FIR4N60BPG

N-Channel Super Junction Power MOSFET-Y

First Semiconductor

PIN Connection   TO-251

G D S

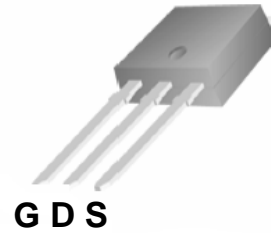## General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

● New technology for high voltage device

● Low on-resistance and low conduction losses

● Small package

● Ultra Low Gate Charge cause lower driving requirements

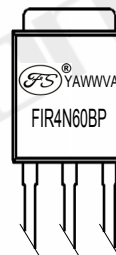● 100% Avalanche Tested

● ROHS compliant

Application

● Power factor correction（PFC）

● Switched mode power supplies(SMPS)

● Uninterruptible Power Supply（UPS）

Schematic diagram

Marking Diagram

YAWWVA
FIR4N60BP
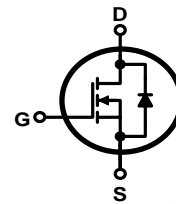
Y	= Year
A	= Assembly Location
WW	= Work Week
VA	= Version & Assembly plant
FIR4N60BP	= Specific Device Code

Table 1.   Absolute Maximum Ratings (T$_C$=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V$_{GS}$=0V）	V$_{DS}$	600	V
Gate-Source Voltage (V$_{DS}$=0V)	V$_{GS}$	±30	V
Continuous Drain Current at Tc=25°C	I$_{D (DC)}$	4	A
Continuous Drain Current at Tc=100°C	I$_{D (DC)}$	2.5	A
Pulsed drain current **(Note 1)**	I$_{DM (pluse)}$	12	A
Maximum Power Dissipation(Tc=25℃)	P$_D$	77	W
Derate above 25°C		0.62	W/°C
Single pulse avalanche energy **(Note2)**	E$_{AS}$	130	mJ
Avalanche current**(Note 1)**	I$_{AR}$	2	A
Repetitive Avalanche energy ， t$_{AR}$ limited by T$_{jmax}$ **(Note 1)**	E$_{AR}$	0.2	mJ

Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150	°C

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	1.62	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	110	°C /W

Table 3. Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=250\mu A$	600			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$			1	µA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$			50	µA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm30V, V_{DS}=0V$			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V$, $I_D=2.5A$		2.2	2.4	Ω
Dynamic Characteristics						
Input Capacitance	C_{Iss}	$V_{DS}=50V, V_{GS}=0V$, F=1.0MHz		300		PF
Output Capacitance	C_{oss}			28		PF
Reverse Transfer Capacitance	C_{rss}			2.3		PF
Total Gate Charge	Q_g	$V_{DS}=480V, I_D=4A$, $V_{GS}=10V$		6.5	10	nC
Gate-Source Charge	Q_{gs}			1.3		nC
Gate-Drain Charge	Q_{gd}			2.5		nC

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switching times						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=380V, I_D=2.5A$, $R_G=20Ω, V_{GS}=10V$		6		nS
Turn-on Rise Time	t_r			3		nS
Turn-Off Delay Time	$t_{d(off)}$			48	60	nS
Turn-Off Fall Time	t_f			8	15	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	$T_C=25°C$		4		A
Pulsed Source-drain current(Body Diode)	I_{SDM}			12		A
Forward On Voltage	V_{SD}	$Tj=25°C, I_{SD}=4A, V_{GS}=0V$		1.4		V
Reverse Recovery Time	t_{rr}	$Tj=25°C, I_F=4A, di/dt=100A/\mu s$		150		nS
Reverse Recovery Charge	Q_{rr}			0.85		uC
Peak reverse recovery current	I_{rrm}			11		A

Notes: 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

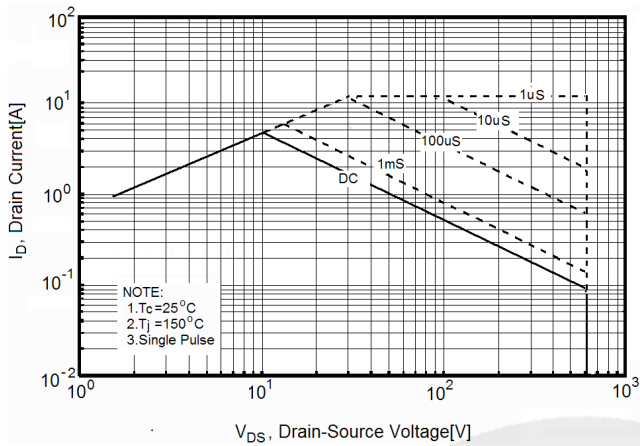**Figure1. Safe operating area**

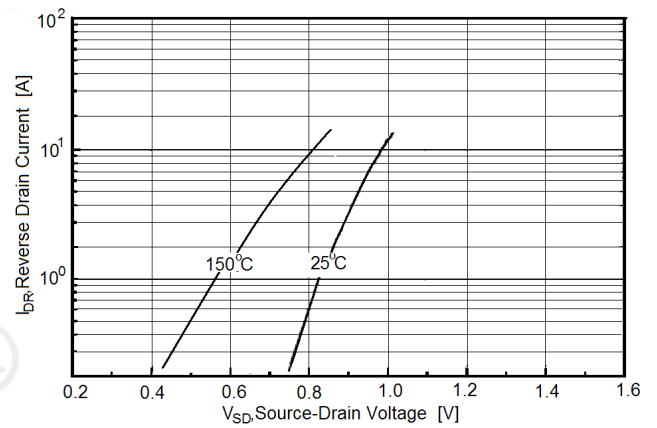**Figure2. Source-Drain Diode Forward Voltage**

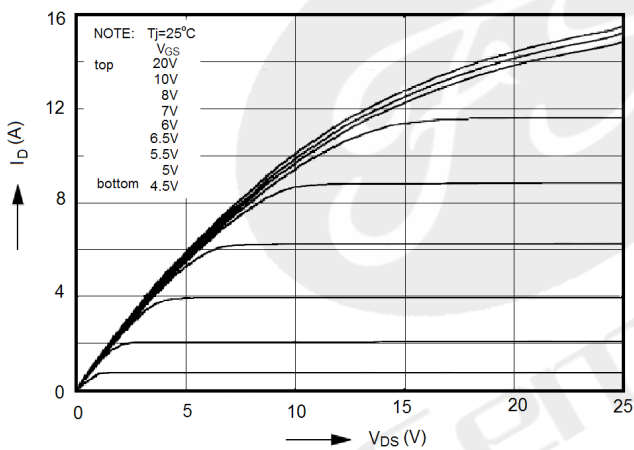**Figure3. Output characteristics**

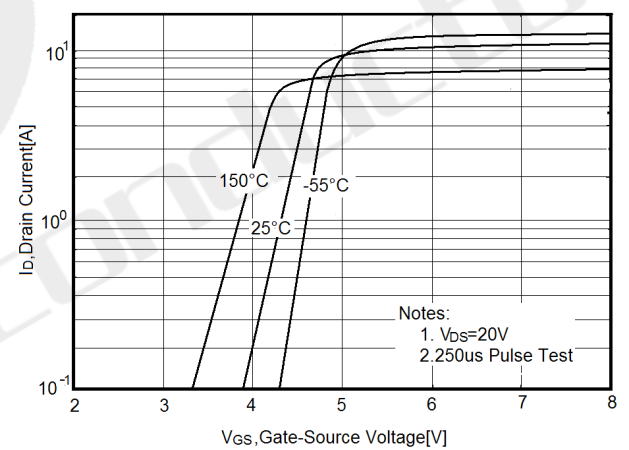**Figure4. Transfer characteristics**

Figure5. Static drain-source on resistance
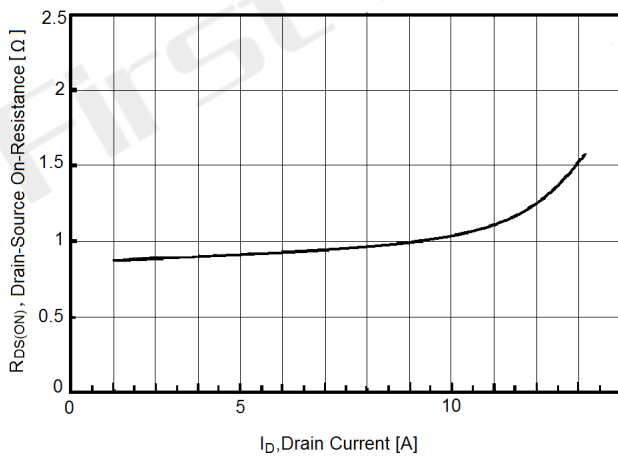
Figure6. $R_{DS(ON)}$ vs Junction Temperature

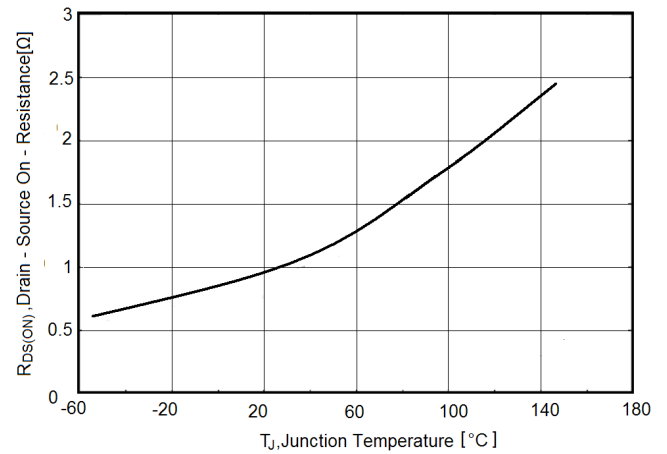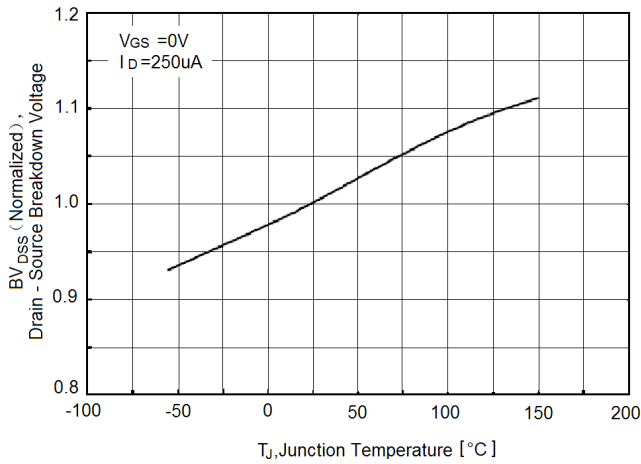## Figure7. BV$_{DSS}$ vs Junction Temperature

$V_{GS} = 0V$
$I_D = 250uA$

BV$_{DSS}$ (Normalized), Drain - Source Breakdown Voltage

T$_J$, Junction Temperature [°C]

Figure8. Maximum I$_D$ vs Junction Temperature

I$_D$, Drain Current [A]

T$_c$, Case Temperature[°C]
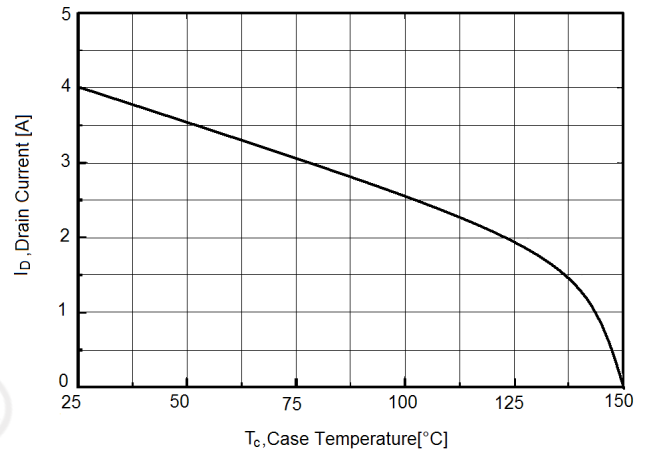
Figure9. Gate charge waveforms

0.2V$_{DS}$ max

0.8V$_{DS}$ max

Note: I$_D$=4A

V$_{GS}$, Gate - Source Voltage [V]

Q$_G$, Total Gate Charge [nC]

Figure10. Capacitance

Ciss=Cgs+Cgd(Cds=shorted)
Coss=Cds+Cgd
Crss=Cgd

Ciss
Coss
Crss

Notes:
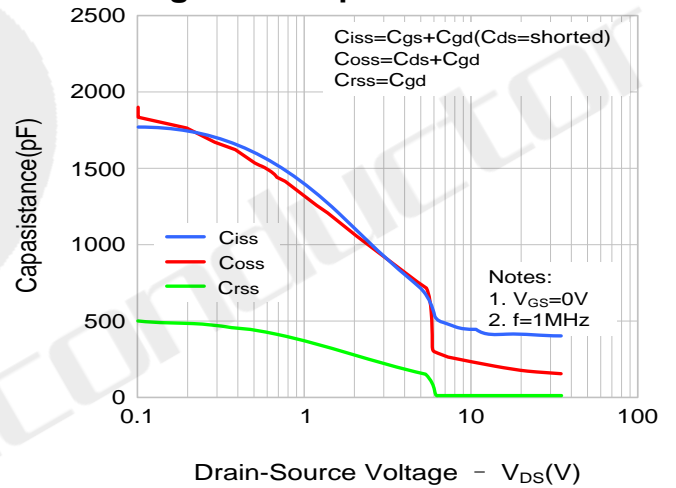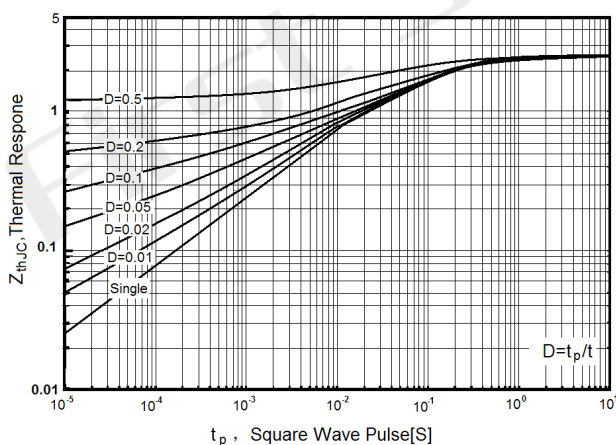1. V$_{GS}$=0V
2. f=1MHz

Capasistance(pF)

Drain-Source Voltage － V$_{DS}$(V)
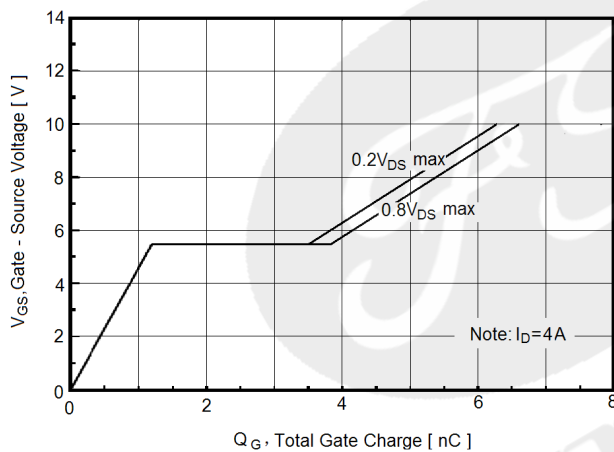
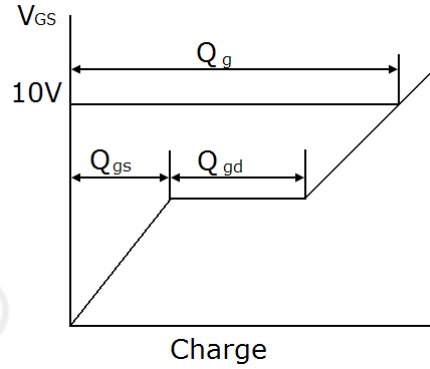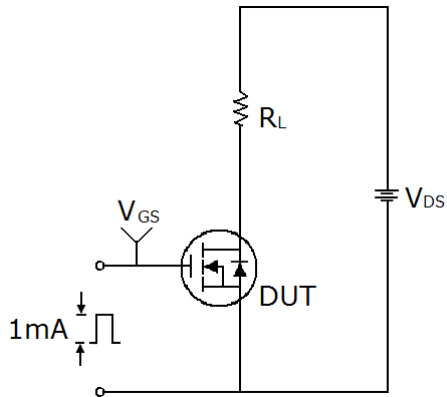## Figure11. Transient Thermal Impedance

D=0.5
D=0.2
D=0.1
D=0.05
D=0.02
D=0.01
Single

D=t$_p$/t

Z$_{thJC}$, Thermal Respone
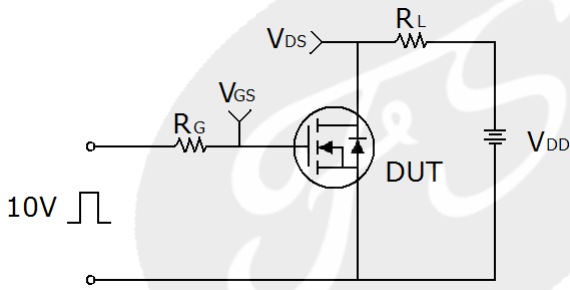
t$_p$, Square Wave Pulse[S]
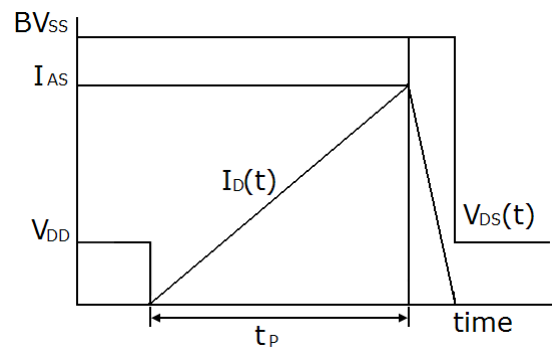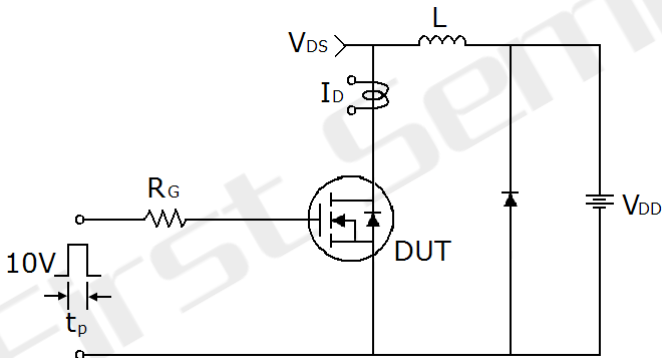
Test circuit

1）Gate charge test circuit & Waveform

2）Switch Time Test Circuit：
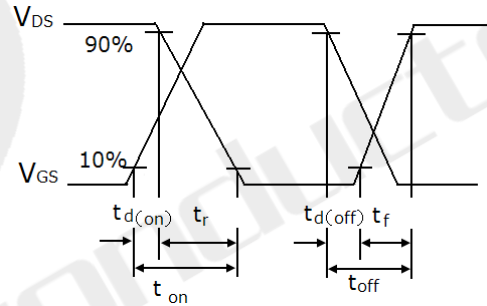
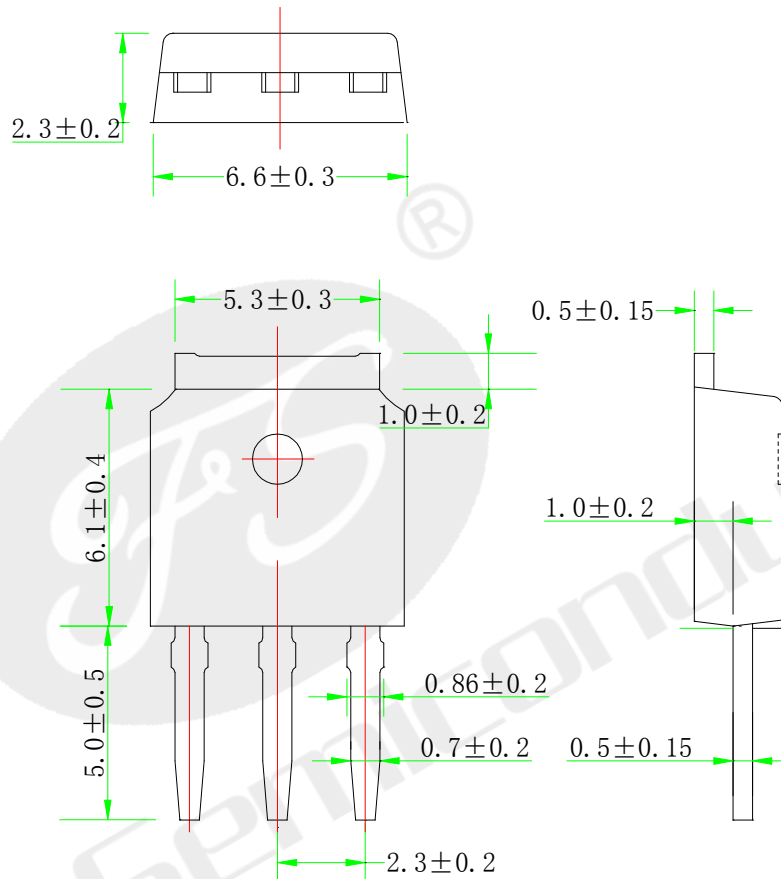### 3）Unclamped Inductive Switching Test Circuit & Waveforms

Package Information

TO-251

Units：mm

2.3±0.2

6.6±0.3

5.3±0.3

1.0±0.2

0.5±0.15

6.1±0.4

1.0±0.2

5.0±0.5

0.86±0.2

0.7±0.2

0.5±0.15

2.3±0.2

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ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	

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