

Parameters Subject to Change Without Notice

DESCRIPTION

The JW[®]5062T is a monolithic buck switching regulator based on I²[™] architecture for fast transient response. Operating with an input range of 4V~18V, JW5062T delivers 4A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples.

JW5062T guarantees robustness with output short protection, thermal protection, current run-away protection, input under voltage lockout, and FB short protection.

JW5062T is available in TSOT23-6 and TSOT23-8 package, which provide a compact solution with minimal external components.

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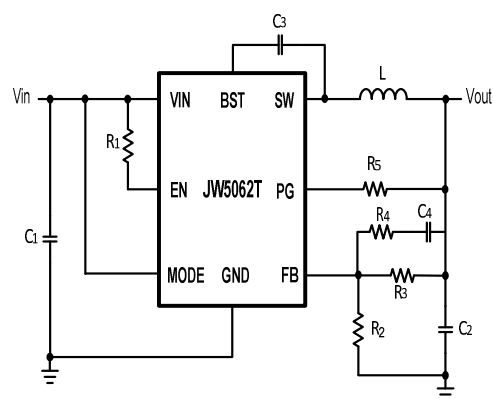
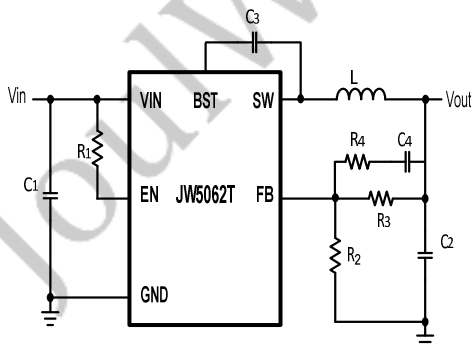
FEATURES

- 4V to 18V operating input range
- 4A output current
- Up to 95% efficiency
- High efficiency (>85%) at light load
- 600kHz switching frequency
- Internal soft-start
- Input under voltage lockout
- Feedback short protection
- Current run-away protection
- Output short protection
- Thermal protection
- Available in TSOT23-6 and TSOT23-8 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION



ORDER INFORMATION

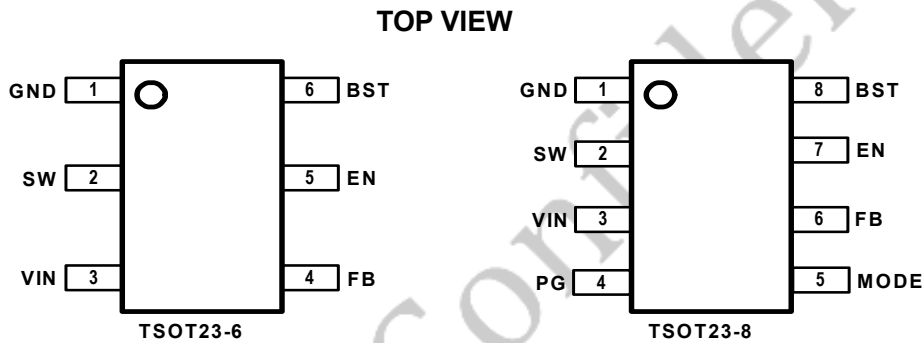
DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW5062TTSOTB#TRPBF	TSOT23-6	J2CX
JW5062TTSOTC#TRPBF	TSOT23-8	J2DX

Notes:

1) JW #TRPBF
Part No. Package Code PB Free Tape and Reel (If "TR" is not shown, it means tube)

2) The first three of top marking mean Part No., and the last letter of top marking means Date Code.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

VIN, EN, SW, MODE Pin	-0.3V to 25V
BST Pin	SW-0.3V to SW+5V
All other Pins	-0.3V to 6V
Junction Temp. ^{2) 3)}	150°C
Lead Temperature	260°C
ESD Susceptibility (Human Body Model)	2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN	4V to 18V
Output Voltage Vout	0.765V to VIN-3V

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
TSOT23-6.....	110	55°C/W
TSOT23-8.....	110	55°C/W

Note:

- 1) Exceeding these ratings may damage the device.
- 2) The JW5062T guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 3) The JW5062T includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

<i>V_{IN}=12V, T_A=25 °C, Unless otherwise stated.</i>						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V _{IN} Under Voltage Lock-out Threshold	V _{IN_MIN}	V _{IN} rising	3.3	3.6	3.8	V
V _{IN} Under voltage Lockout Hysteresis ⁵⁾	V _{IN_MIN_HYST}			200		mV
Shutdown Supply Current	I _{SD}	V _{EN} =0V			1	μA
Supply Current	I _Q	V _{EN} =5V, V _{FB} =1.2V		220		μA
Feedback Voltage	V _{FB}	4.7V<V _{IN} <18V	753	765	777	mV
Top Switch Resistance ⁵⁾	R _{DS(ON)T}			49		mΩ
Bottom Switch Resistance ⁵⁾	R _{DS(ON)B}			20		mΩ
Top Switch Leakage Current	I _{LEAK_TOP}	V _{IN} =18V, V _{EN} =0V, V _{SW} =0V			1	μA
Bottom Switch Leakage Current	I _{LEAK_BOT}	V _{IN} =18, V _{EN} =0V, V _{SW} =18V			1	μA
Top Switch Current Limit	I _{LIM_TOP}			6.5		A
Bottom Switch Current Limit	I _{LIM_BOT}		4	4.5	5	A
Minimum On Time ⁵⁾	T _{ON_MIN}			100		ns
Minimum Off Time ⁵⁾	T _{OFF_MIN}	V _{FB} =0.4V		100		ns
EN Rising threshold ⁵⁾	V _{EN_H}	V _{EN} rising	1.9	2.05	2.2	V
EN Hysteresis ⁵⁾	V _{EN_HYS}	V _{EN} Hysteresis		150		mV
Soft-Start Period	t _{SS}			1.6		ms
Power good lower threshold	PGD_LTH	FB falling		94%		
Power good upper threshold	PGD_UTH	FB rising		106%		
Power good delay ⁵⁾	PGD_DLY	PG from low to high		1		ms
Thermal Shutdown ⁵⁾	T _{TSD}			170		°C
Thermal Shutdown hysteresis ⁵⁾	T _{TSD_HYST}			20		°C

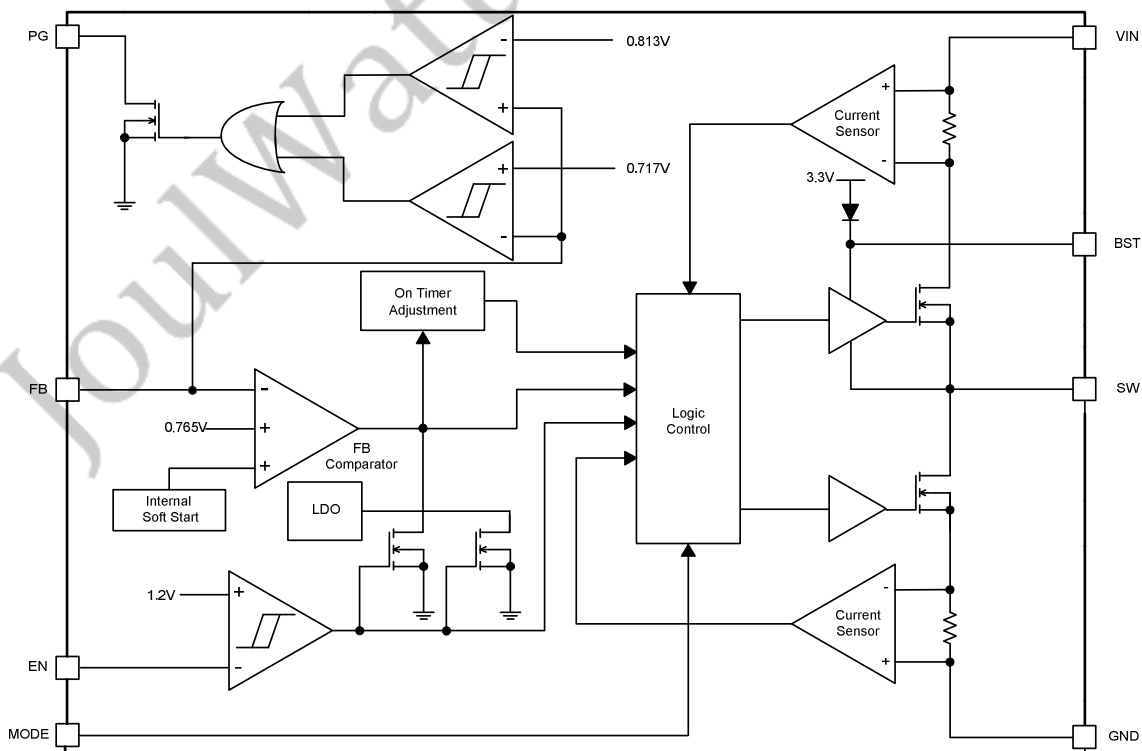
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Pin		Name	Description
TSOT23-6	TSOT23-8		
1	1	GND	Ground pin.
2	2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	6	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.765V. Connect a resistive divider at FB.
5	7	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	8	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
	4	PG	Power good monitor output. This is an open-drain output so a resistor should be connected at this pin to the VCC pin.
	5	MODE	Pull MODE pin low to VIN to achieve PFM operation. Pull MODE up to GND or floating to achieve FCC operation.

BLOCK DIAGRAM

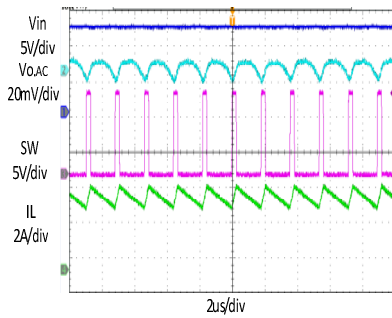


TYPICAL PERFORMANCE CHARACTERISTICS

Vin =12V, Vout = 1.5V, L = 2.2μH, Cout = 44μF, TA = +25°C, unless otherwise noted

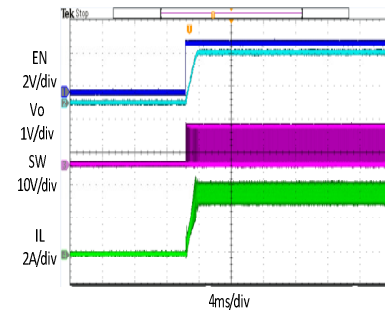
Steady State Test

VIN=12V, Vout=1.5V
Iout=4A



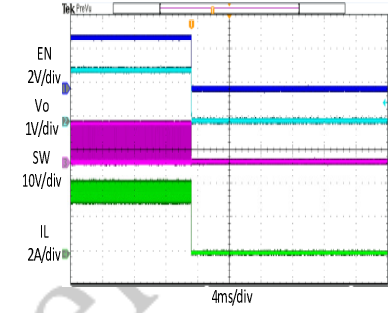
Startup through Enable

VIN=12V, Vout=1.5V
Iout=4A(Resistive load)



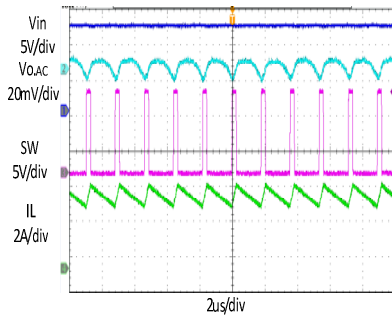
Shutdown through Enable

VIN=12V, Vout=1.5V
Iout=4A (Resistive load)



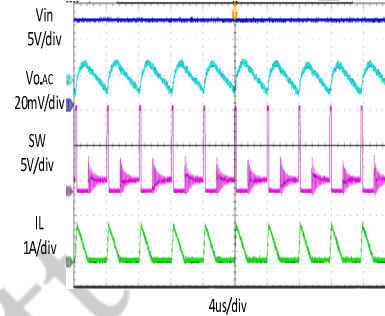
Heavy Load Operation

4A LOAD



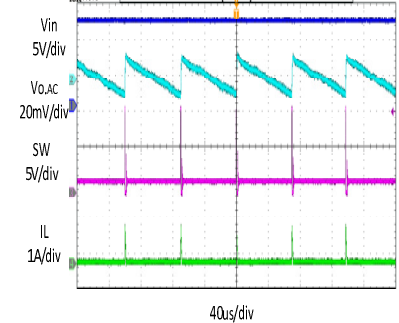
Medium Load Operation

0.2A LOAD



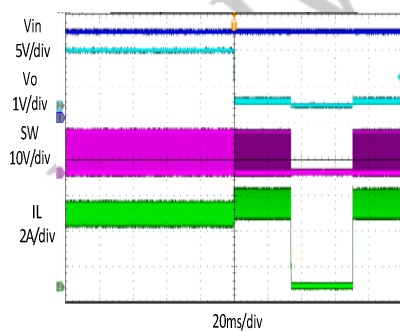
Light Load Operation

0 A LOAD



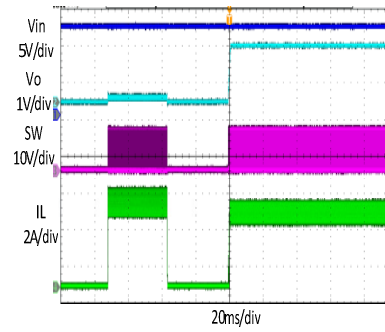
Short Circuit Protection

VIN=12V, Vout=1.5V
Iout=4A- Short



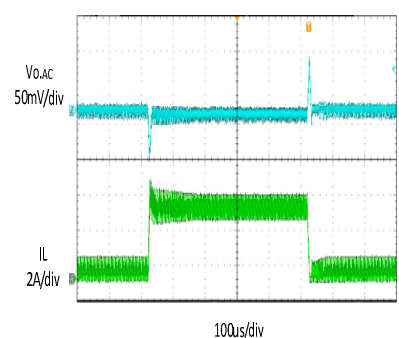
Short Circuit Recovery

VIN=12V, Vout=1.5V
Iout= Short-4A



Load Transient

0.4A LOAD → 4A LOAD → 0.4A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS

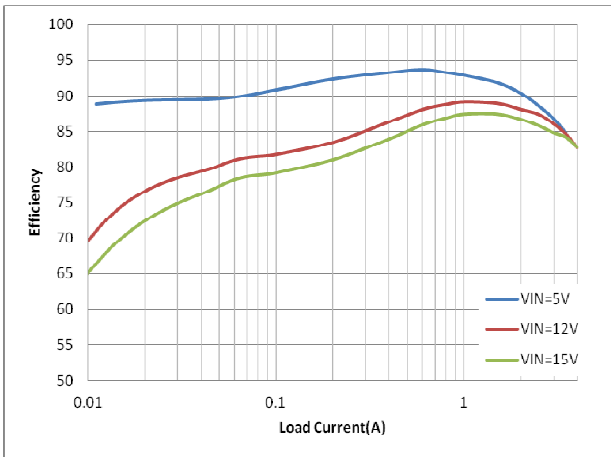


Figure 1. Efficiency vs Load Current
(Vout=1.5V, L=2.2uH)

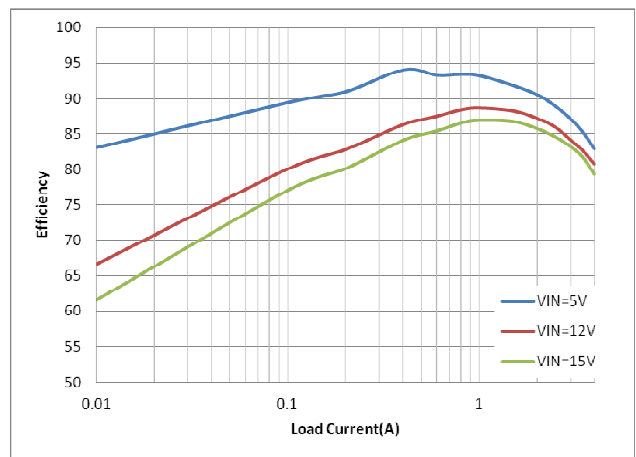


Figure 2. Efficiency vs Load Current
(Vout=1.8V, L=2.2uH)

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FUNCTIONAL DESCRIPTION

JW5062T is a synchronous step-down regulator based on I²™ control architecture. It regulates input voltages from 4V to 18V down to an output voltage as low as 0.765V, and is capable of supplying up to 4A of load current.

Shut-Down Mode

JW5062T shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by JW5062T drops below 1µA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5062T to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 2V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current. A valley current limit is designed in JW5062T so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 1024 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 1024 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 2048 cycles. After the 2048 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 1024 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Thermal Protection

When the temperature of the JW5062T rises above 140°C, it is forced into thermal shut-down. Only when core temperature drops below 125°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{out} \cdot \frac{R_2}{R_2 + R_3}$$

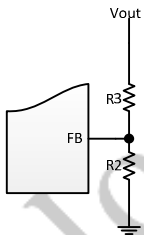
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_2 around 15kΩ, and then R_3 can be calculated by:

$$R_3 = R_2 \cdot \left(\frac{V_{out}}{0.765} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

V _{OUT} (V)	R ₂ (kΩ)	R ₃ (kΩ)
1	13.3	4.02
1.2	28	16
1.5	16	15.4
2.5	20.5	46.4
3.3	16	53.1
5	16	88.7



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_1 is the input capacitance value, f_s is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2} \right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a

22uF~66uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

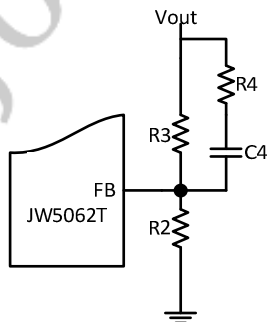
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

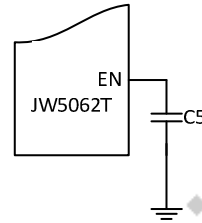
Feedforward Capacitor

In order to minimize the ripple of output voltage at light load, a feedforward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_4 around 1kΩ and C_4 around 50pF.



Start up through EN

If JW5062T start up through EN, a 10nF or larger capacitor should be connected between EN pin and GND to eliminate noise.



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5062T (V_{IN} pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

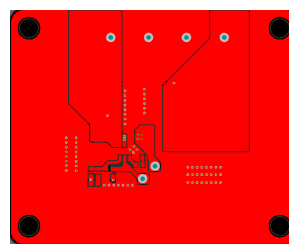


Figure 1. Top Layer

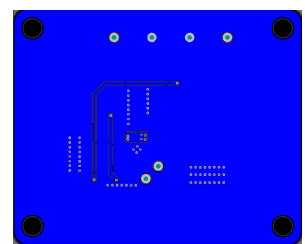


Figure 2. Bottom Layer

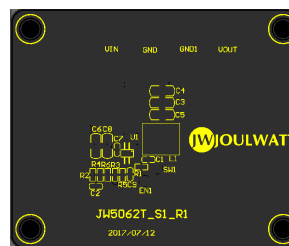
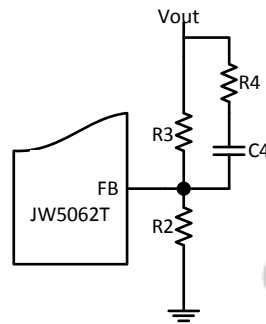


Figure 3. Silk Layer

External Components Suggestion:

V _{OUT} (V)	R ₂ (kΩ)	R ₃ (kΩ)	R ₄ (kΩ)	C ₄ (pF)	L (uH)	C _{out} (uF)
1	13.3	4.02	1	180	2.2	54~66
1.2	28	16	1	180	2.2	54~66
1.5	12	11.2	1	180	2.2	44~66
2.5	20.5	46.4	1	180	2.2	22~66
3.3	16	53.1	1	180	2.2	22~66
5	16	88.7	1	180	3.3~4.7	22~66



REFERENCE DESIGN

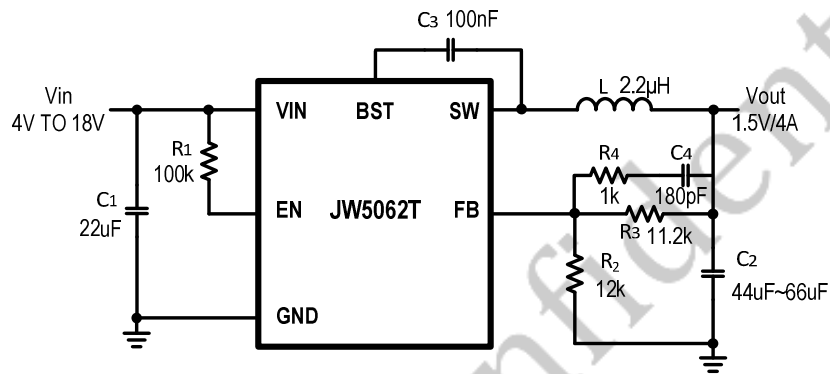
Reference 1:

Vin : 4V~18V

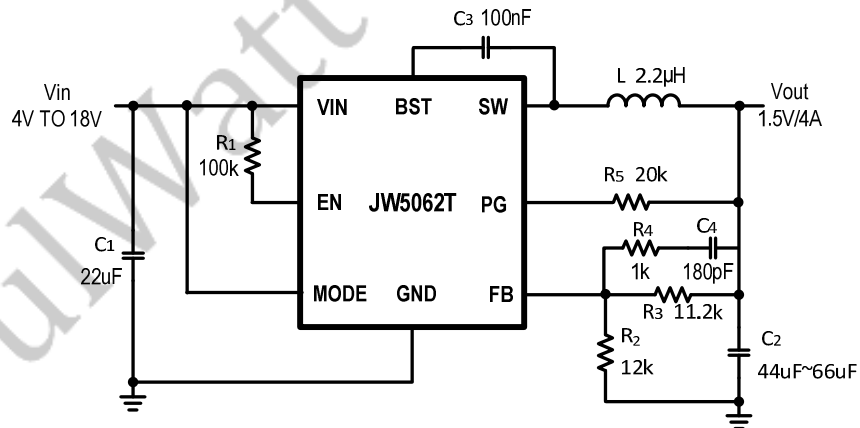
Vout: 1.5V

Iout : 0~4A

TSOT23-6:



TSOT23-8:



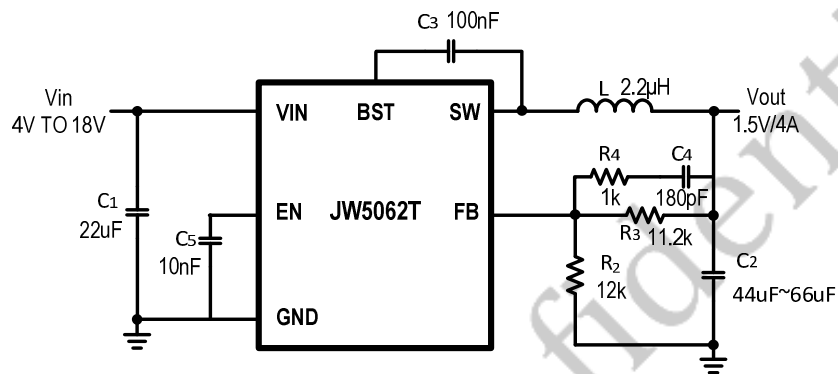
Start up Through EN

Vin : 4V~18V

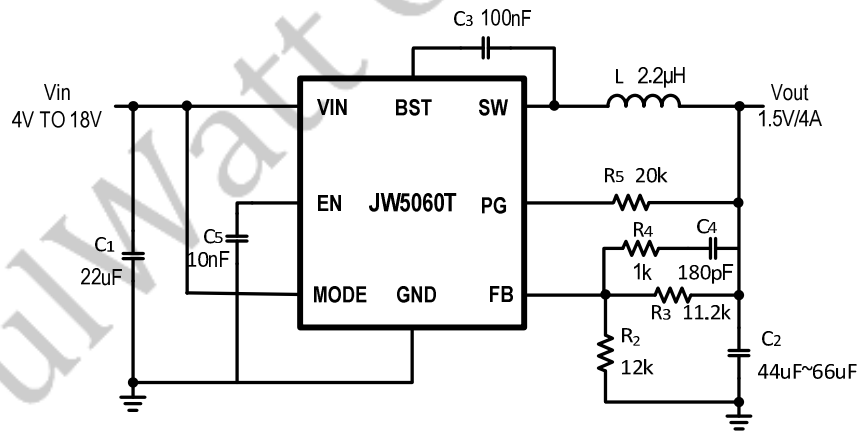
Vout: 1.5V

Iout : 0~4A

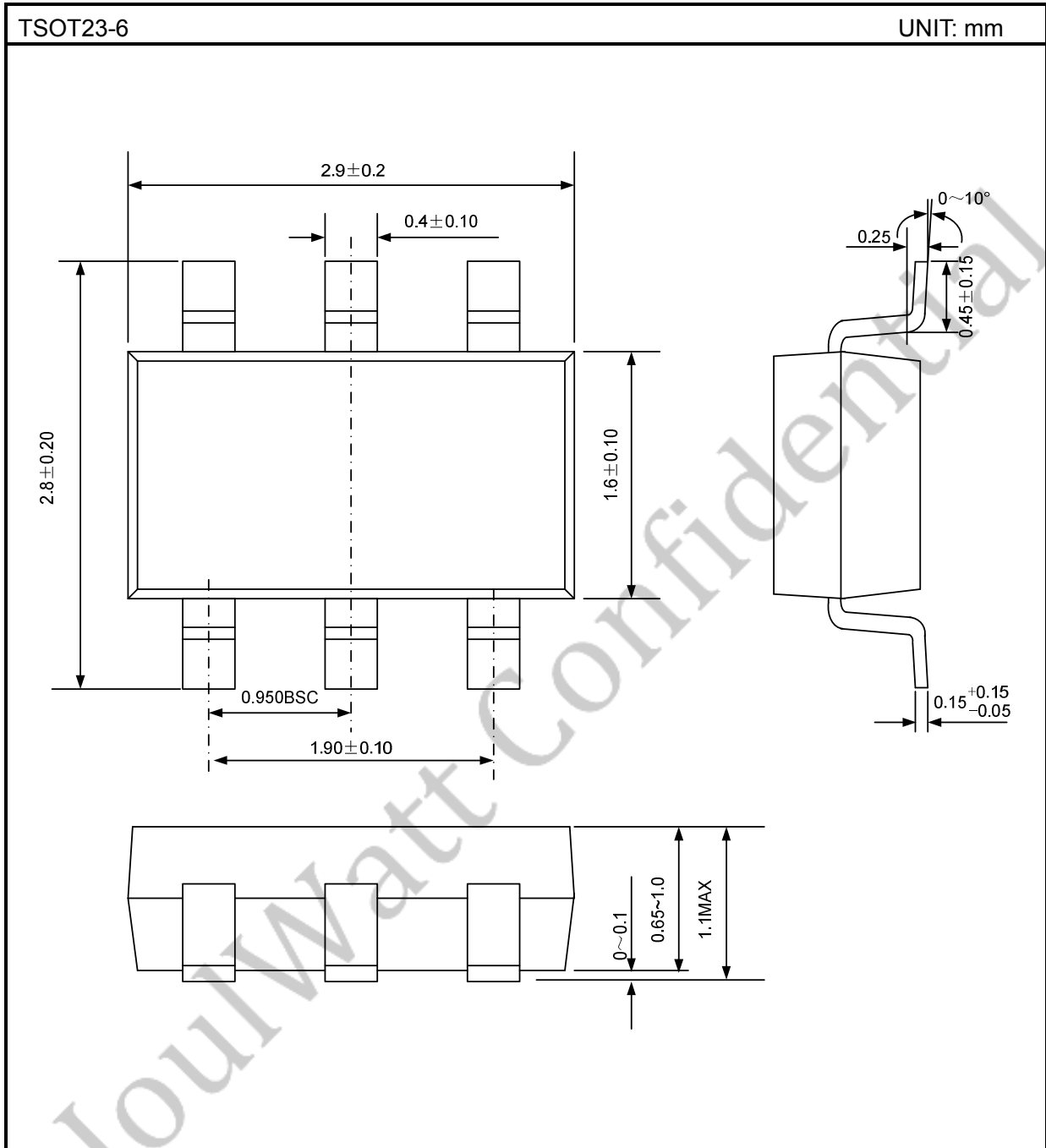
TSOT23-6:



TSOT23-8:

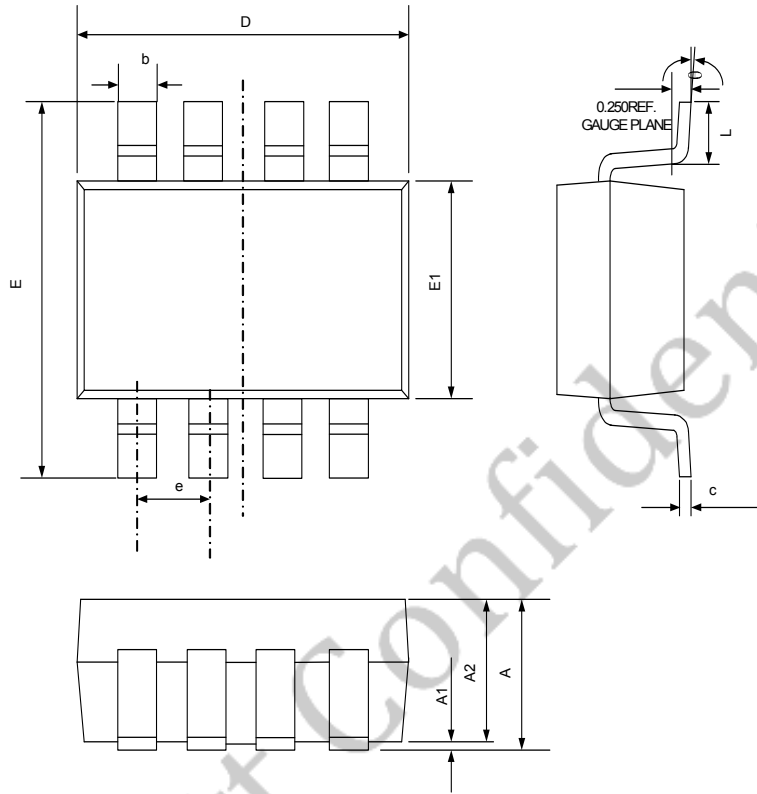


PACKAGE OUTLINE



TSOT23-8

UNIT: mm



Symbol	Dimensions In Millimeters	
	Min	Max
A	---	1.100
A1	0.000	0.100
A2	0.700	1.000
D	2.850	2.950
E	2.650	2.950
E1	1.550	1.650
b	0.200	0.400
c	0.080	0.200
e	0.650(BSC)	
L	0.300	0.600
θ	0°	8°

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