

## 3A, Synchronous Step-Down Converter

### DESCRIPTION

The EUP3226 is a 1 MHz fixed frequency synchronous, current-mode, step-down dc-dc converter capable of providing up to 3A output current. The EUP3226 operates from an input range of 2.7V to 5.5V and provides a regulated output voltage from 0.6V to 5V. The internal synchronous power switch improves efficiency and eliminates the need for an external Schottky diode. The EUP3226 can be externally set for either forced PWM continuous mode or pulse skipping mode. Forced PWM operation provides very low output ripple voltage for noise sensitive applications while pulse skipping operation improves light load efficiency by reducing switching loss.

The EUP3226 features short circuit and thermal protection circuits to improve system reliability. Internally soft-start avoids input inrush current during startup. The EUP3226 is available in TDFN 3mm×3mm 10-pin package with the exposed pad and SOP-8 package with the exposed pad.

### FEATURES

- 2.7V to 5.5V Input Voltage Range
- High Efficiency up to 96%
- 3A Available Load Current
- 57/35mΩ Integrated PFET/NFET Switches
- 1MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- Short Circuit and Thermal Protection
- Integrated UVLO and Power Good
- Excellent Line and Load Transient Response
- Available in 10-Pin 3mm×3mm TDFN and SOP-8 (EP) Packages
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

### APPLICATIONS

- High Performance DSPs, FPGAs, ASICs and Microprocessors
- Base Station, Telecom, and Networking Equipment Power Supplies
- ePC and NetPCs

### Typical Application Circuit

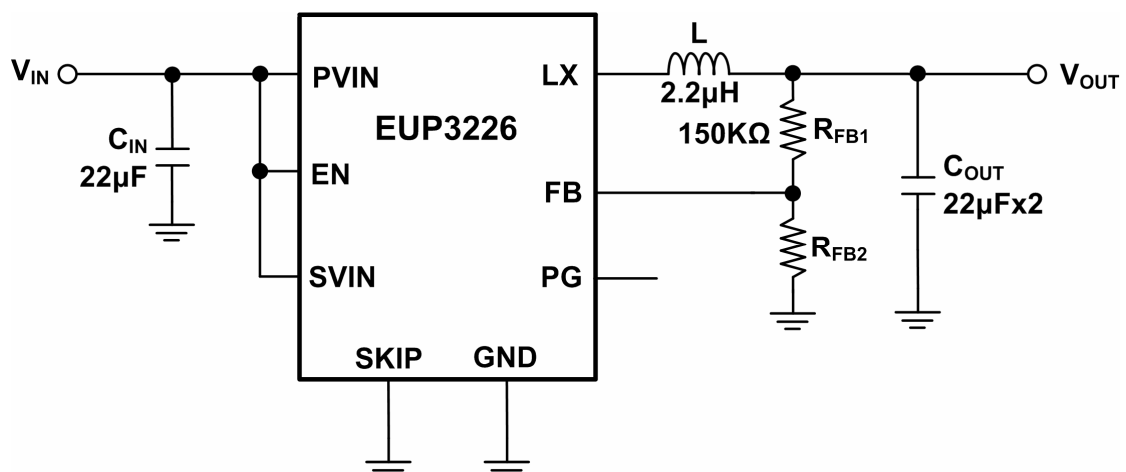


Figure1. TDFN-10 Typical Application Circuit

## Typical Application Circuit (continued)

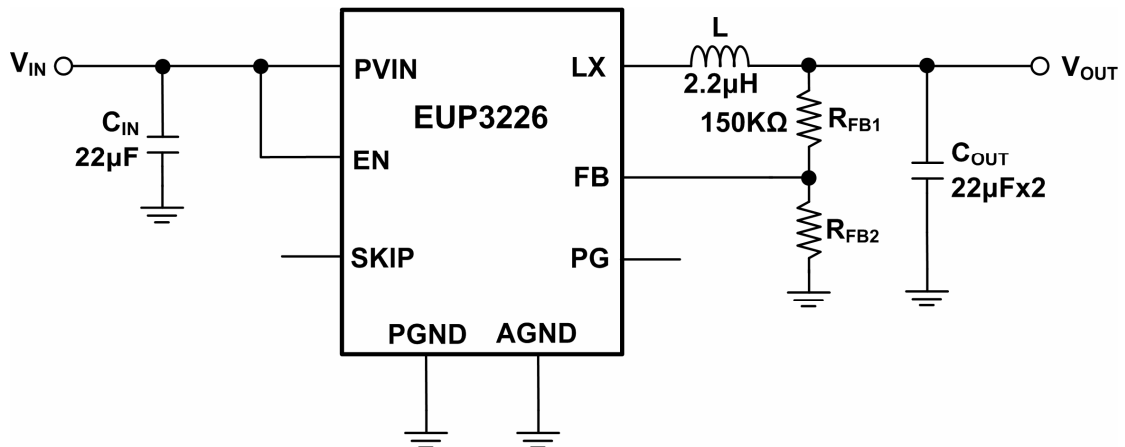


Figure2. SOP-8 (EP) Typical Application Circuit

## Pin Configurations

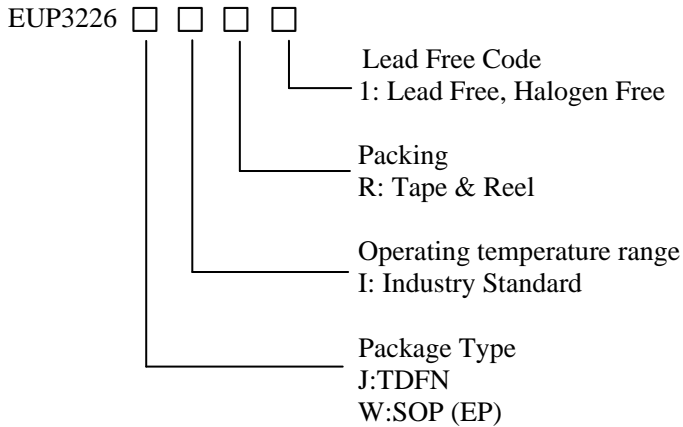
Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-10	<p>(TOP VIEW)</p>	SOP-8 (EP)	<p>(TOP VIEW)</p>

## Pin Description

PIN	TDFN-10	SOP-8 (EP)	DESCRIPTION
NC	1	-	No connection.
LX	2,3	1	Switch node connected to inductor. This pin is connected to the drains of the internal main and synchronous power MOSFET switches.
PG	4	4	Power good output signal. Logic high when regulator output is within $\pm 10\%$ of target output voltage. A pull-up resistor of 10k $\Omega$ to 100k $\Omega$ is recommended for most applications.
EN	5	3	Chip enable pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V or floating it shut down the device. An internal 600k $\Omega$ resistor pull it down to ground.
FB	6	6	Feedback pin. Connect it to an external resistor divider to set output voltage.
SKIP	7	2	Operation Mode Select Input. Logic high selects pulse skipping mode, and logic low or floating chooses forced PWM mode. An internal 7 $\mu$ A current pull it down to ground.
SVIN	8	-	Analog input supply which is connected to PVIN through a low pass RC filter.
PVIN	9,10	7	Input voltage to the power switches.
AGND	-	5	Analog ground.
PGND	-	8	Power ground.
Thermal Pad	-	-	Ground.( Thermal pad is used as the ground of whole chip.)

## Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3226JIR1	TDFN-10	XXXXX P3226 1A	-40 °C to +85°C
EUP3226WIR1	SOP-8 (EP)	XXXXX P3226 1A	-40 °C to +85°C



## Block Diagram

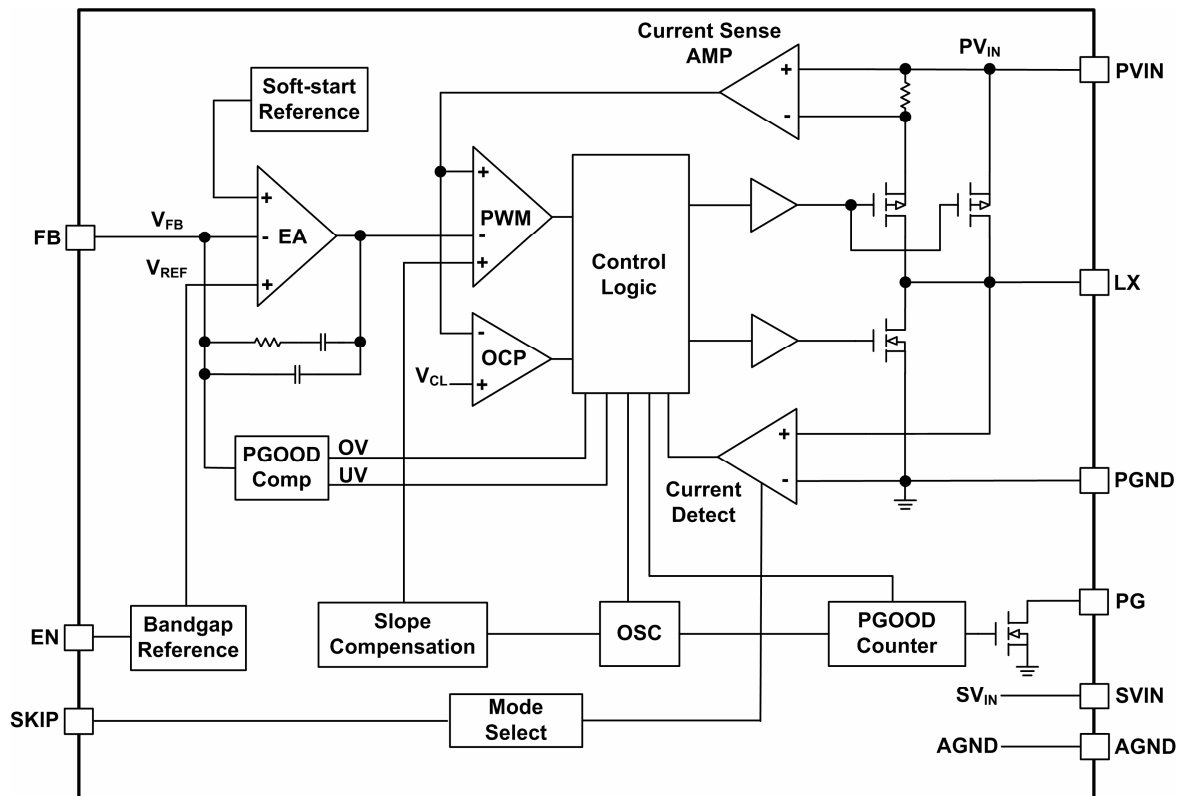


Figure3. Block Diagram

## Absolute Maximum Ratings (1)

■	Input Supply Voltage(SVIN, PVIN) -----	-0.3V to 6V
■	EN, FB, SKIP -----	-0.3V to 6V
■	PG -----	0V to 6V
■	LX Voltage -----	-0.3V to $V_{PVIN}+0.3V$
■	Junction Temperature -----	150°C
■	Package Thermal Resistance	
	TDFN-10, $\theta_{JA}$ -----	69°C/W
	SOP-8 (EP), $\theta_{JA}$ -----	60°C/W
■	Storage Temperature -----	-65°C to 150°C
■	Lead Temp (Soldering, 10sec) -----	260°C
■	Minimum ESD Rating -----	±2kV

## Recommended Operating Conditions (2)

■	Supply Voltage -----	2.7V to 5.5V
■	Operating Temperature Range -----	-40°C to 85°C

Note(1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note(2): The device is not guaranteed to function outside the recommended operating conditions.

## Electrical Characteristics

$V_{PVIN}=V_{SVIN}=V_{VEN}=5V$ ,  $T_A=+25^\circ C$ , unless otherwise specified. The ● indicates specifications which apply over the full operating range -40°C to +85°C. The EUP3226 is 100% production tested at 25°C. Typical and temperature specifications are guaranteed by design and statistical characterizations.

Symbol	Parameter	Conditions	EUP3226			Unit
			Min.	Typ.	Max.	
$V_{IN}$	Input Voltage Range	$-40^\circ C \leq T_A \leq +85^\circ C$	● 2.7		5.5	V
UVLO	Input Undervoltage Lockout	Rising, $-40^\circ C \leq T_A \leq +85^\circ C$	● 2.25	2.45	2.65	V
UVLO_Hys	UVLO Hysteresis			200		mV
$I_{FB}$	Feedback Current	$V_{FB}=0.6V$	-50	0	+50	nA
$V_{FB}$	Regulated Feedback Voltage	$T_A=+25^\circ C$	0.594	0.600	0.606	V
		$-40^\circ C \leq T_A \leq +85^\circ C$	● 0.588	0.600	0.612	
$\Delta V_{OUT}$	Output Voltage Line Regulation	$V_{IN}=3V$ to 5V		0.15		%/V
$V_{LOADREG}$	Output Voltage Load Regulation	$I_{LOAD}=100mA$ to 3A		0.1		%/A
$V_{PGH}$	Power Good High Threshold	With Respect To $V_{FB}$	+7	+10	+13	%
$V_{PGL}$	Power Good Low Threshold	With Respect To $V_{FB}$	-13	-10	-7	%
$T_{PG}$	Power Good Delay Time			32		Cycles
$V_{LPG}$	Power Good Low Voltage	$I_{SINK}=1mA$		0.1	0.3	V
$I_{PG}$	Power Good Leakage Current	High Impedance, $V_{PG}=5V$			1	μA
$V_{ENL}$	EN Input Low Voltage				0.3	V
$V_{ENH}$	EN Input High Voltage		1.5			V
$R_{EN}$	EN Pull Down Resistor			600		KΩ
$V_{SKIPL}$	SKIP Input Low Voltage				0.3	V
$V_{SKIPH}$	SKIP Input High Voltage		1.5			V
$I_{SKIP}$	SKIP Pull Down Current		3	7	10	μA
$I_Q$	Quiescent Current	$V_{FB}=0.65V$ , $V_{SKIP}=5V$ or 0V		0.5	0.8	mA
$I_{SHDN}$	Shutdown Current	$V_{EN}=0V$			3	μA

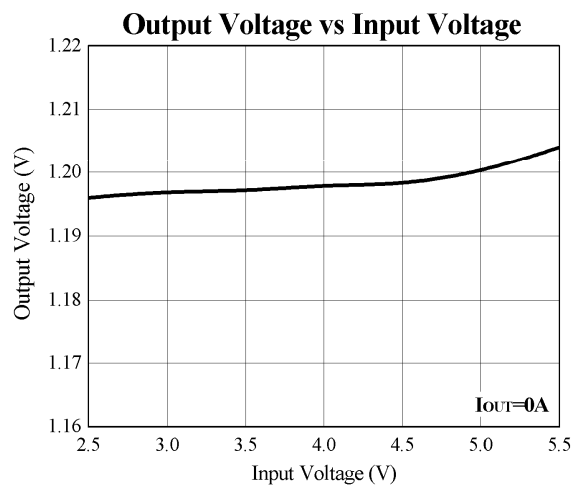
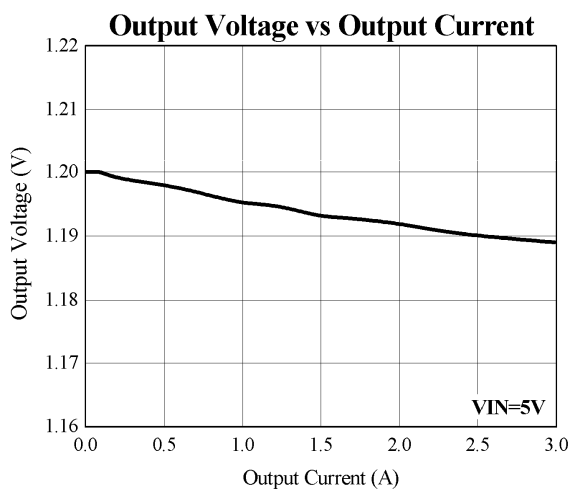
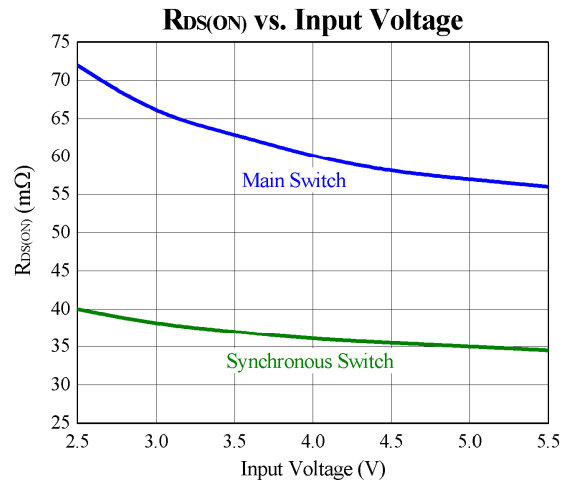
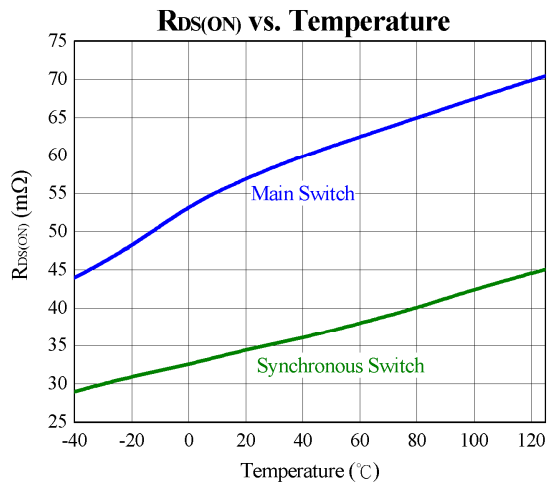
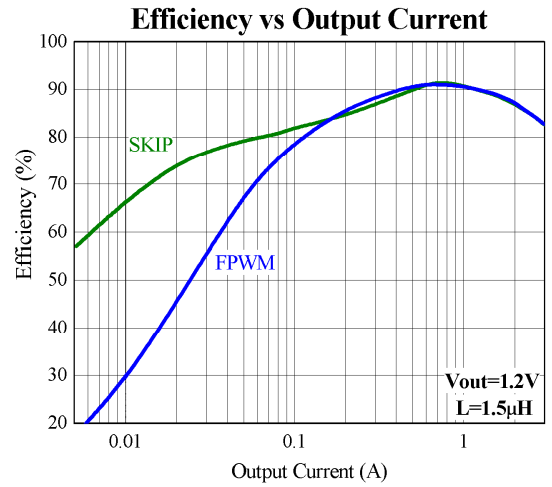
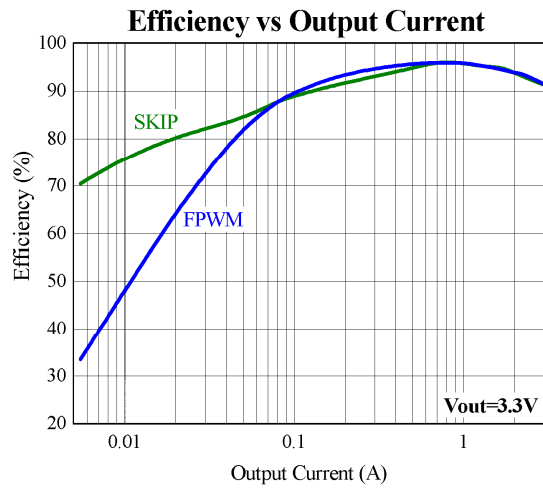
**Electrical Characteristics (continued)**

PVIN=SVIN=VEN=5V, T<sub>A</sub>=+25°C, unless otherwise specified. The • indicates specifications which apply over the full operating range -40°C to +85°C. The EUP3226 is 100% production tested at 25°C. Typical and temperature specifications are guaranteed by design and statistical characterizations.

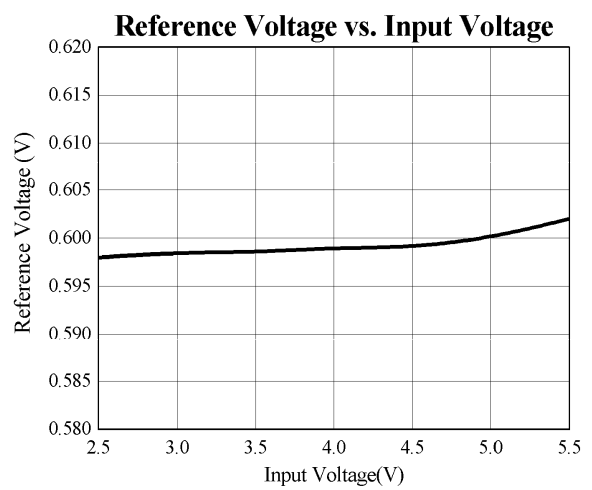
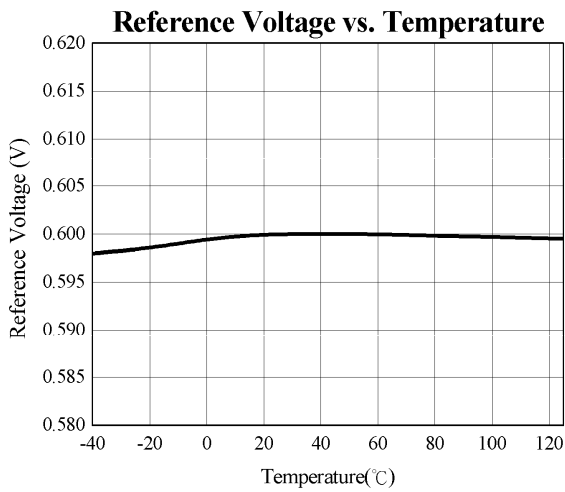
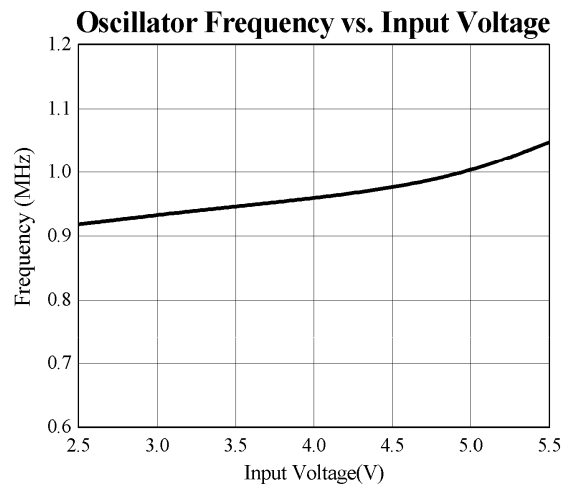
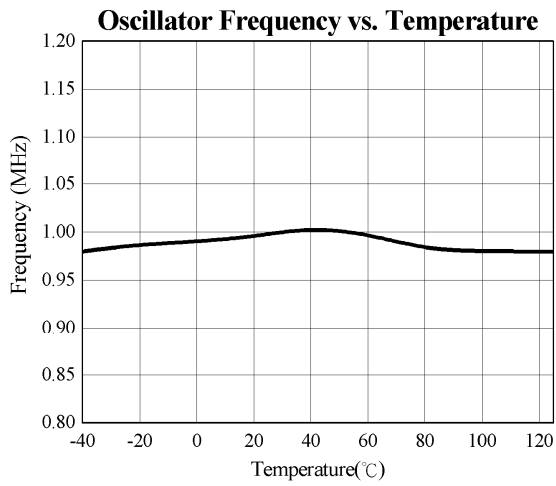
Symbol	Parameter	Conditions	EUP3226			Unit
			Min.	Typ.	Max.	
f <sub>OSC</sub>	Oscillator Frequency	V <sub>FB</sub> =0.55V, -40°C ≤ T <sub>A</sub> ≤ +85°C •	0.8	1	1.2	MHz
		V <sub>FB</sub> =0V		380		KHz
D <sub>MAX</sub>	Maximum Duty Cycle			100		%
T <sub>ON(Min)</sub>	Minimum On Time			100		ns
I <sub>PEAK</sub>	Hside PCH Switch Peak Current	V <sub>FB</sub> =0.55V		5		A
I <sub>NEG</sub>	Lside NCH Negative Current Limit	V <sub>SKIP</sub> =0V, FPWM Mode		-1		A
R <sub>LX</sub>	LX Pull Down Resistor	V <sub>EN</sub> =0V		1.25		KΩ
R <sub>PFET</sub>	R <sub>DS(ON)</sub> of P-Channel FET	I <sub>LX</sub> =0.5A		57	70	mΩ
R <sub>NFET</sub>	R <sub>DS(ON)</sub> of N-Channel FET	I <sub>LX</sub> =0.5A		35	50	mΩ
T <sub>SD</sub>	Thermal Shutdown			160		°C

## Typical Operating Characteristics

$C_{IN}=22\mu\text{F}$ ,  $C_{OUT}=22\mu\text{F}\times 2$ ,  $L=2.2\mu\text{H}$ ,  $V_{IN}=5\text{V}$ ,  $V_{OUT}=1.2\text{V}$ , See Figure 1,  $T_A=25^\circ\text{C}$ , unless otherwise noted.

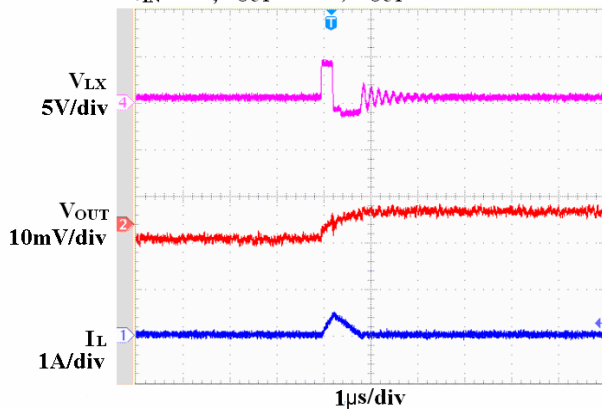


## Typical Operating Characteristics (continued)



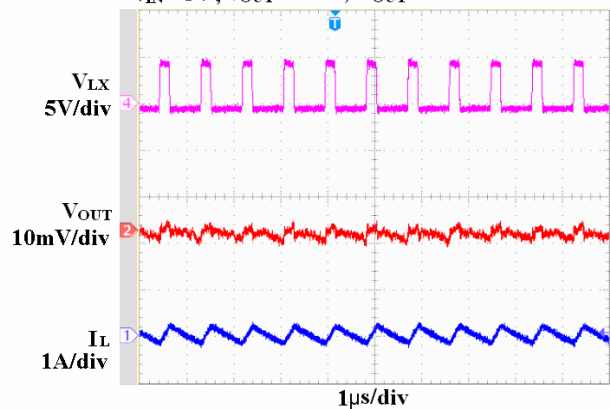
### Skip Mode Operation

$V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A$



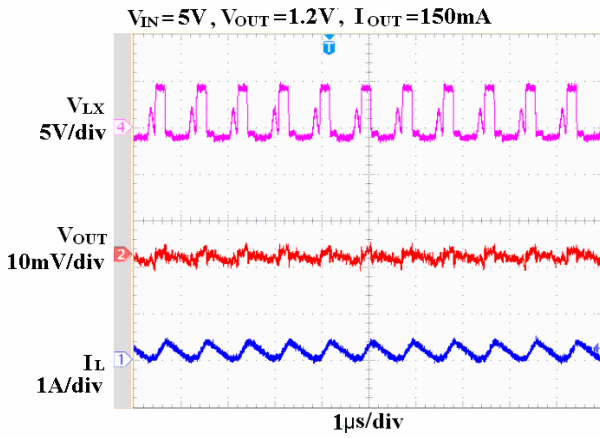
### FPWM Mode Operation

$V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A$

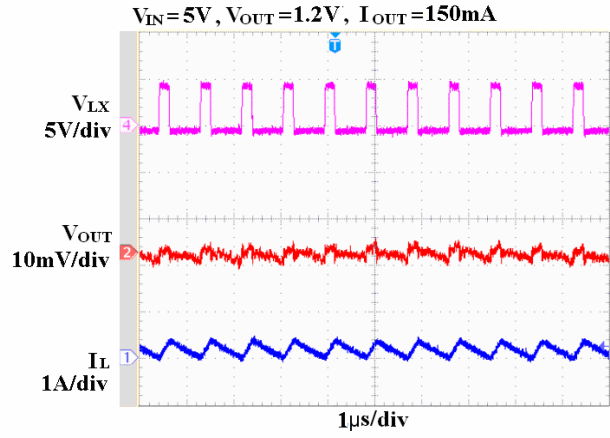


**Typical Operating Characteristics (continued)**

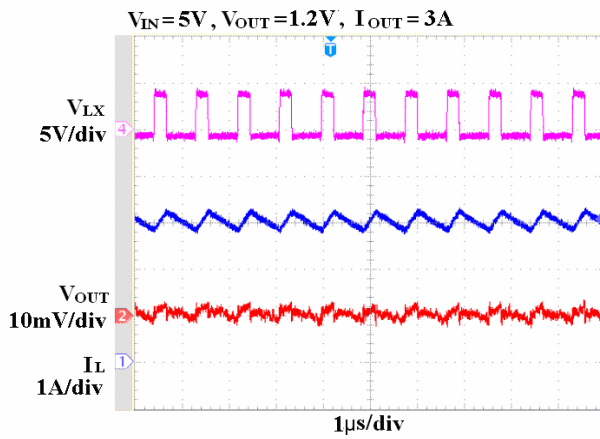
**Skip Mode Operation**



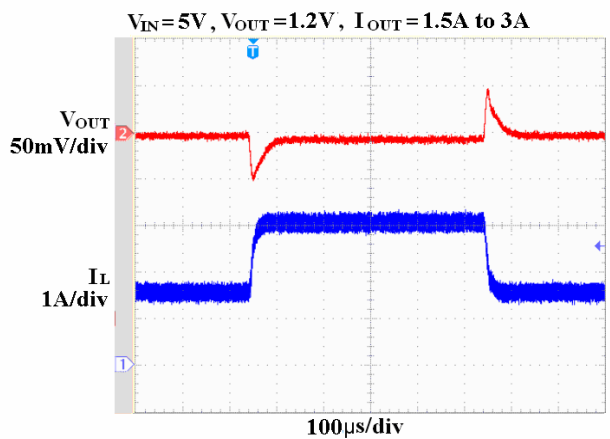
**FPWM Mode Operation**



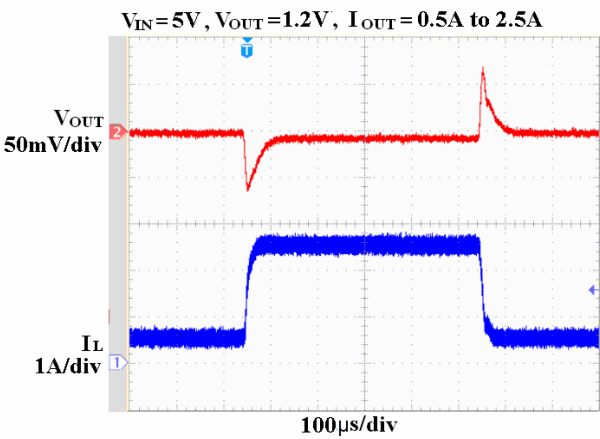
**FPWM Mode Operation**



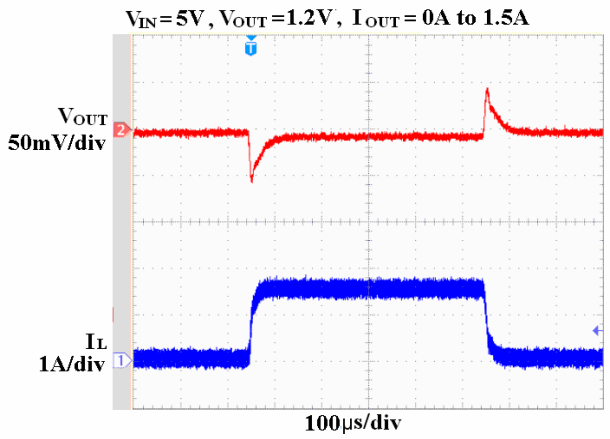
**Load Step**



**Load Step**



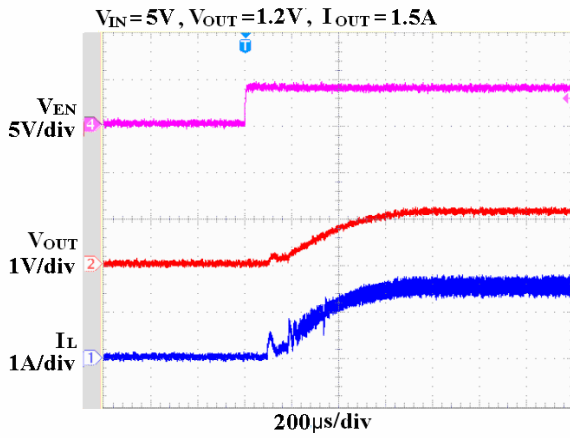
**Load Step (FPWM Mode)**



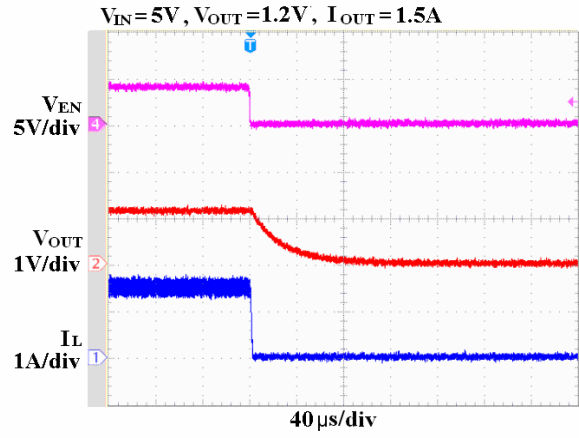


## Typical Operating Characteristics (continued)

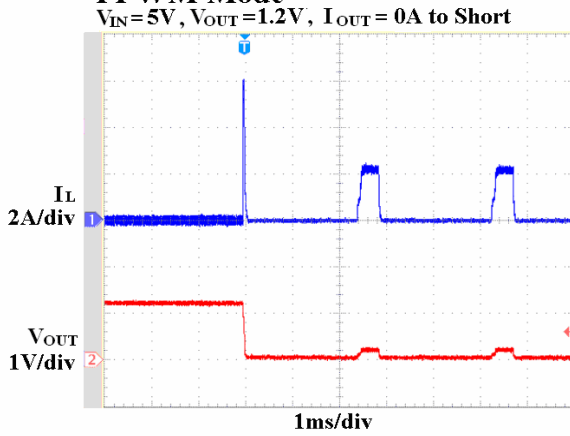
### Start Up



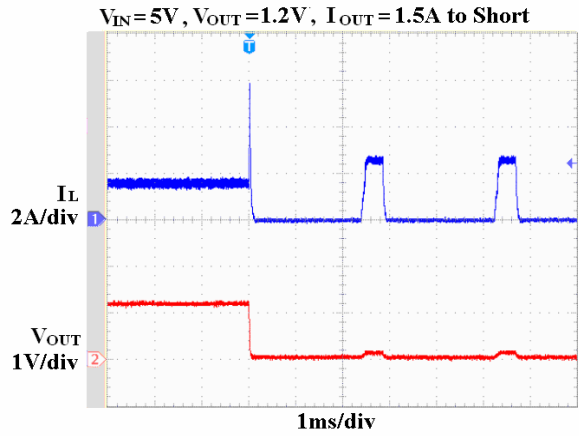
### Shut Down



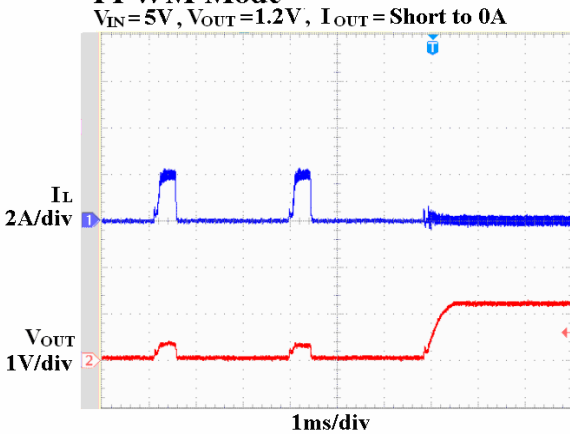
### Short Circuit FPWM Mode



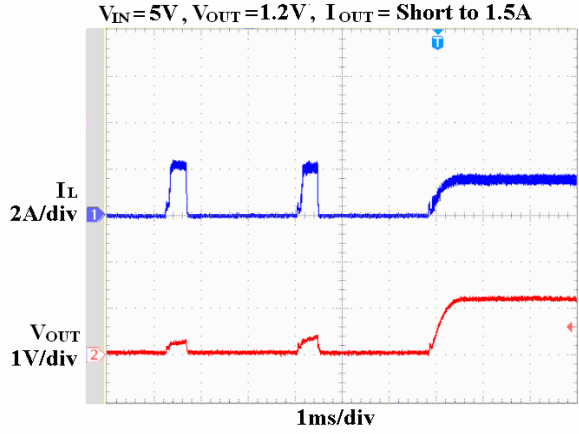
### Short Circuit



### Short Circuit Recovery FPWM Mode



### Short Circuit Recovery



## Application Information

The EUP3226 uses a slope-compensated constant frequency, current mode architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the EUP3226 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by three weighted differential signals: the output of error amplifier, the main switch sense voltage and the slope-compensation ramp. It modulates output power by adjusting the inductor peak-current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle. When the inductor current starts to reverse in pulse skipping mode operation or when the PWM reaches the end of the oscillator period in forced PWM operation, the synchronous switch turns off.

### Soft-Start

The EUP3226 has an internal soft-start circuit to limit the inrush current and output voltage overshoot during startup. The soft-start time is about 800 $\mu$ S.

### Short-Circuit Protection

As soon as the output voltage drops below 50% of the nominal output voltage, the converter switching frequency and the current limit are reduced.

### Output Overvoltage Protection

The output voltage is monitored by a comparator through FB pin. It guards against transient overshoots >10% by turning the main switch off.

### Input Undervoltage Lockout

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the main and synchronous switches under undervoltage state.

### Thermal Protection and Lockout

The internal thermal protection and lockout circuit prevents device in the event that the maximum junction temperature is exceeded. If the device temperature is higher than 160 $^{\circ}$ C (typical), it will be shut down. Only if the power is reprovided or the EN pin is reactivated can the device rework.

### Inductor Selection

The EUP3226 typically uses a 2.2 $\mu$ H output inductor. The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  influence the ripple current as shown in equation.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation.

The DC-resistance of the inductor directly influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

### $C_{IN}$ and $C_{OUT}$ Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3226. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical value is around 22 $\mu$ F.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The output capacitor  $C_{OUT}$  has a strong effect on loop stability.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR).

ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

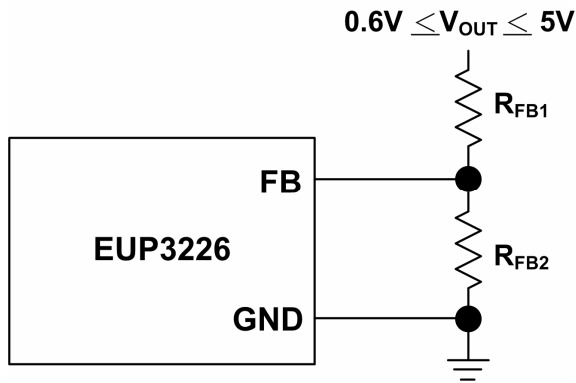
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula, where  $R_{FB1}$  value is kept 150K $\Omega$ :

$$R_{FB2} = R_{FB1} \left( \frac{0.6}{V_{OUT} - 0.6} \right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown below.



### Thermal Considerations

To avoid the EUP3226 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

Where  $P_D = I_{LOAD}^2 \times R_{DS(ON)}$  is the power dissipated by the regulator ;  $\theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature,  $T_J$ , is given by:

$$T_J = T_A + T_R$$

Where  $T_A$  is the ambient temperature.

$T_J$  should be below the maximum junction temperature of 150°C.

### PC Board Layout Checklist

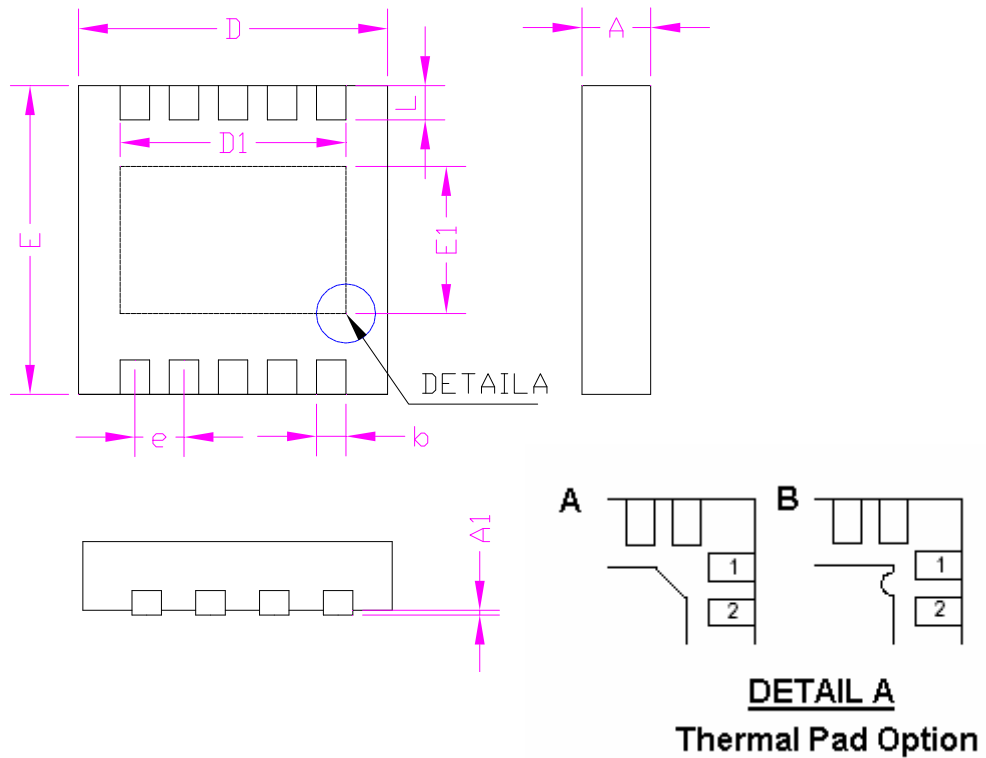
For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3226.

1. The input capacitor  $C_{IN}$  should connect to PVIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the LX trace and the VIN trace should be kept short, direct and wide.
3. The FB pin should connect directly to the feedback resistors. The resistive divider  $R_{FB1}/R_{FB2}$  must be connected between the  $C_{OUT}$  and ground.
4. Keep the switching node, LX, away from the sensitive FB node.

## Packaging Information

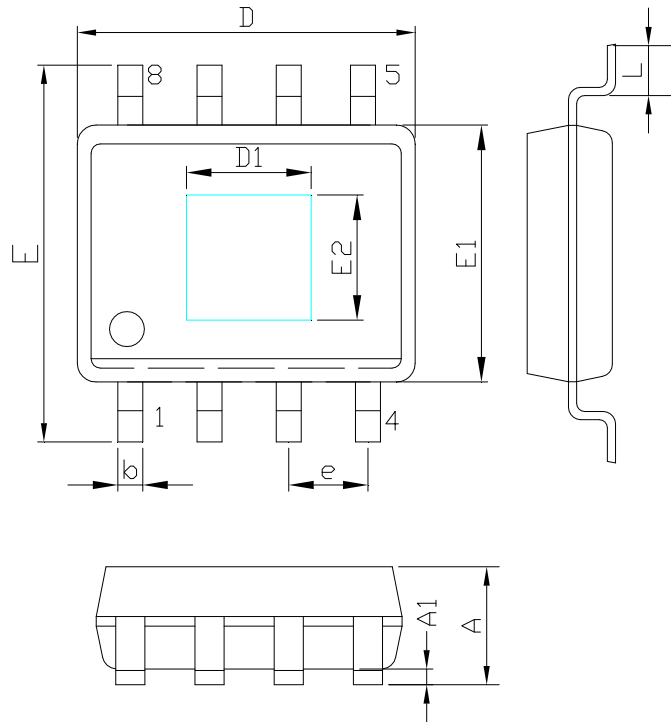
### TDFN-10



Remark: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.60	2.65	0.091	0.102	0.104
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.50	1.65	1.75	0.059	0.065	0.069
L	0.30	0.40	0.50	0.012	0.016	0.020
b	0.18	-	0.30	0.007	-	0.012
e	0.50 REF			0.020 REF		

**SOP-8 (EP)**



Remark: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	1.35	-	1.75	0.053	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.70	3.90	4.00	0.146	0.154	0.157
D1	2.67	2.97	3.50	0.105	0.117	0.138
E2	1.78	2.18	2.60	0.070	0.086	0.102
E	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	-	1.27	0.016	-	0.050
b	0.31	-	0.51	0.012	-	0.020
e	1.27 REF			0.050 REF		

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