5V to 12V Synchronous Buck Controller

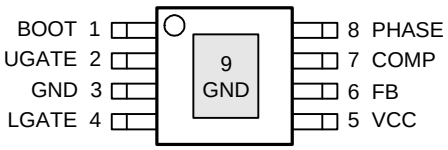
Features

- **Wide Operation Supply Voltage from 5V to 12V**
- **Power-On-Reset Monitoring on VCC**
- **Excellent Reference Voltage Regulations**
  - **0.6V Internal Reference**
  - **±1% Over Temperature Range**
- **Integrated Soft-Start**
- **Automatic PSM/PWM Modes**
- **Voltage Mode PWM Operation with 90% (Max.) Duty Cycle**
- **Under-Voltage Protection**
- **Adjustable Over-Current Protection Threshold**
  - **Sensing the $R_{DS(ON)}$ of Low-Side MOSFET**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **Simple SOP-8P Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Graphic Cards**
- **DSL, Switch HUB**
- **Wireless Lan**
- **Notebook Computer**
- **Mother Board**
- **LCD Monitor/TV**

Pin Configuration



SOP-8P
(Top View)

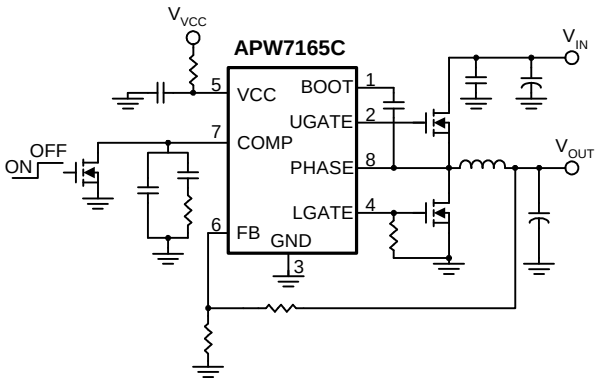
General Description

The APW7165Cis a voltage mode, fixed 300kHz-switching frequency, and synchronous buck controller. The APW7165C allows wide input voltage that is either a single 5~12V or two supply voltage(s) for various applications. A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. A built-in digital soft-start circuit prevents the output voltages from overshoot as well as limits the input current. An internal 0.6V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The APW7165C provides excellent output voltage regulations against load current variation.

The controller's over-current protection monitors the output current by using the voltage drops across the $R_{DS(ON)}$ of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. The APW7165C also integrates over-voltage protection (OVP) and under-voltage protection circuit which monitors the FB voltage to prevent the PWM output from over and under voltage.

The APW7165C is available in a simple SOP-8P package.

Simplified Application Circuit



Ordering and Marking Information

APW7165C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-8P Operating Ambient Temperature Range E : -20 to 70°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7165C KA: APW7165C XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	VCC Supply Voltage (VCC to GND)		-0.3 ~ 16	V
V_{BOOT}	BOOT to PHASE Voltage		-0.3 ~ 16	V
V_{UGATE}	UGATE to PHASE Voltage	> 400ns	-0.3 ~ V_{BOOT}+0.3	V
		< 400ns	-5 ~ V_{BOOT}+5	V
V_{LGATE}	LGATE to GND Voltage	> 400ns	-0.3 ~ V_{VCC}+0.3	V
		< 400ns	-5 ~ V_{VCC}+5	V
V_{PHASE}	PHASE to GND Voltage	> 200ns	-0.3 ~ 16	V
		< 200ns	-10 ~ 30	V
	FB and COMP to GND (< V_{VCC} + 0.3V)		-0.3 ~ 7	V
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2)	SOP-8P	80	°C/W
θ_{JC}	Thermal Resistance -Junction to Case	SOP-8P	20	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	VCC Supply Voltage (VCC to GND)	4.5 ~ 13.2	V
V_{OUT}	Converter Output Voltage	0.9 ~ 5	V
V_{IN}	Converter Input Voltage	2.9 ~ V_{VCC}	V
I_{OUT}	Converter Output Current	0 ~ 20	A
T_A	Ambient Temperature	-20 ~ 70	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 3: Refer to the application circuit for further information.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7165C			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY VOLTAGE AND CURRENT						
I_{VCC}	VCC Supply Current (Shutdown Mode)	UGATE and LGATE open; COMP=GND	-	4	6	mA
	VCC Supply Current	UGATE and LGATE open	-	16	24	
POWER-ON-RESET (POR)						
	Rising VCC POR Threshold		3.7	4.1	4.4	V
	VCC POR Hysteresis		0.3	0.45	0.6	V
OSCILLATOR						
F_{OSC}	Oscillator Frequency		270	300	330	kHz
ΔV_{OSC}	Oscillator Sawtooth Amplitude (Note 4)		-	1.5	-	V
D_{MAX}	Maximum Duty Cycle		85	-	90	%
ERROR AMPLIFIER						
V_{REF}	Reference Voltage	T_A = -20 ~ 70°C	0.594	0.6	0.606	V
	Converter Load Regulation (Note 4)	I_{OUT} = 2 ~ 12A	-	-	0.2	%
gm	Transconductance		-	667	-	µA/V
	FB Input Leakage Current	V_{FB} = 0.6V	-	0.1	1	µA
	COMP High Voltage	R_L = 10kΩ to GND	-	2.5	-	V
	COMP Low Voltage	R_L = 10kΩ to GND	-	1	-	
	Maximum COMP Source Current	V_{COMP} = 2V	-	200	-	µA
	Maximum COMP Sink Current	V_{COMP} = 2V	-	200	-	
GATE DRIVERS						
	High-Side Gate Driver Source Current	V_{BOOT}= 12V, $V_{UGATE-PHASE}$ = 2V	-	1.8	-	A
	High-Side Gate Driver Sink Impedance	BOOT=12V, I_{UGATE} = 0.1A	-	2.3	-	Ω
	Low-Side Gate Driver Source Current	V_{VCC} = 12V, V_{LGATE} = 2V	-	1.8	-	A
	Low-Side Gate Driver Sink Impedance	V_{VCC} =12V, I_{UGATE} = 0.1A	-	1.3	-	Ω
T_D	Dead-Time (Note 4)		-	30	-	ns

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C, unless otherwise noted. Typical values are at T_A = 25°C.

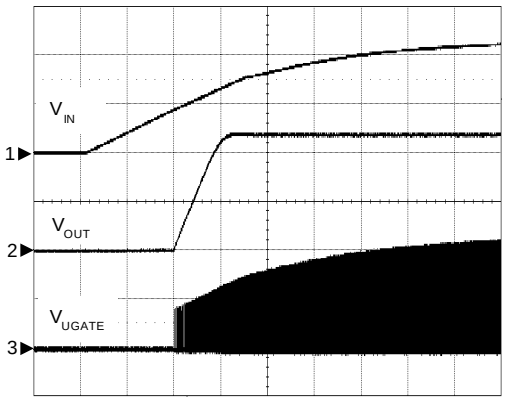
Symbol	Parameter	Test Conditions	APW7165C			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
V_{FB_UV}	FB Under-Voltage Protection Trip Point	Percentage of V_{REF}	45	50	55	%
V_{FB_OV}	FB Over-Voltage Protection Trip Point	V_{FB} rising	115	120	125	%
	FB Over-Voltage Protection Hysteresis		-	5	-	%
V_{OCP_MAX}	Built-in Maximum OCP Voltage		300	-	-	mV
I_{OCSET}	OCSET Current Source		19.5	21.5	23.5	µA
SOFT-START						
$V_{DISABLE}$	Shutdown Threshold of V_{COMP}		-	-	0.6	V
T_{SS}	Internal Soft-Start Interval (Note 4)		-	1.7	-	ms

Note 4: Guaranteed by design, not production tested.

Operating Waveforms

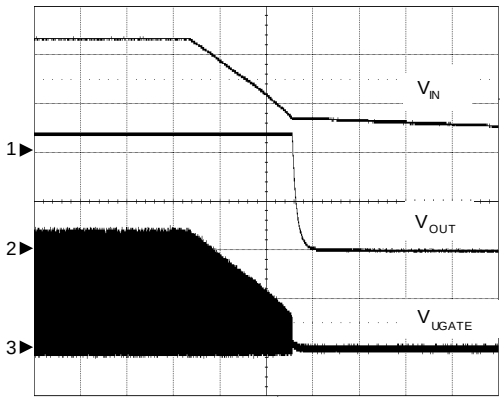
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On



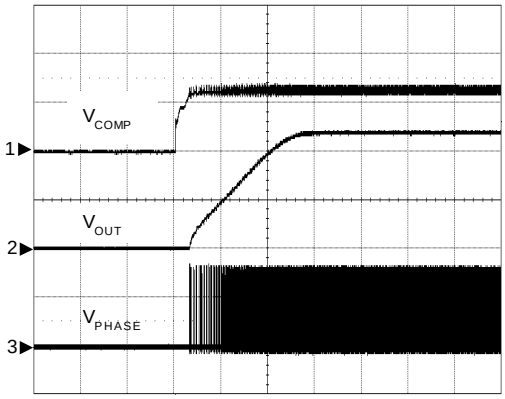
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{UGATE}, 10V/Div
Time: 1ms/Div

Power Off



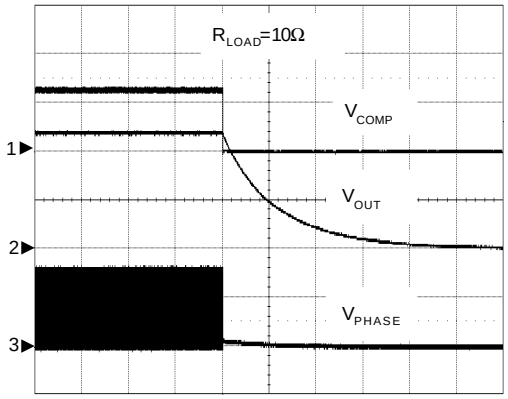
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{UGATE}, 10V/Div
Time: 200ms/Div

Enable



CH1: V_{COMP}, 1V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{PHASE}, 10V/Div
Time: 500µs/Div

Shutdown

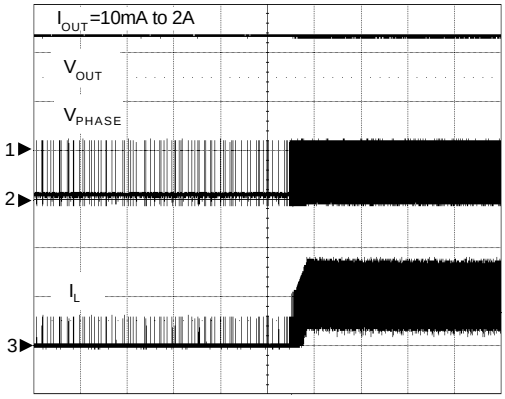


CH1: V_{COMP}, 1V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{PHASE}, 10V/Div
Time: 1ms/Div

Operating Waveforms (Cont.)

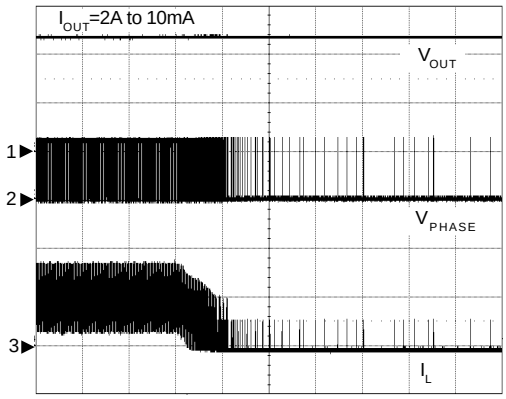
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

PSM to PWM



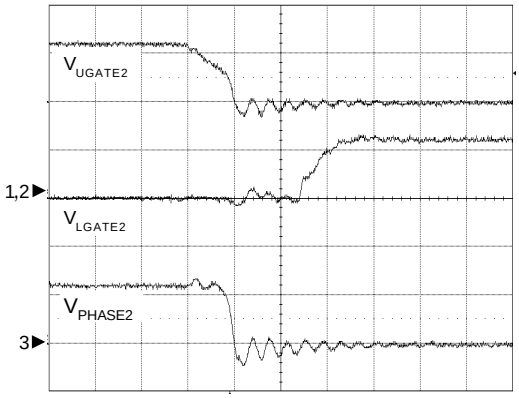
CH1: V_{OUT}, 1V/Div
CH2: V_{PHASE}, 10V/Div
CH3: I_L, 2A/Div
Time: 500µs/Div

PWM to PSM



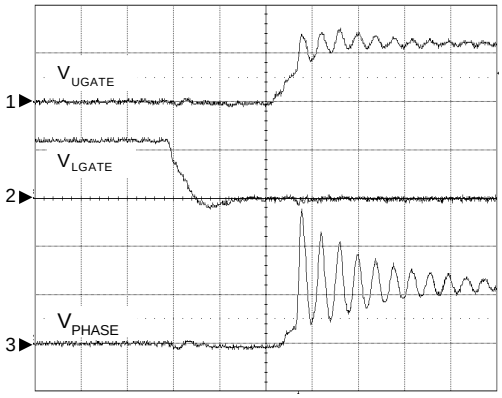
CH1: V_{OUT}, 500mV/Div
CH2: V_{PHASE}, 10V/Div
CH3: I_L, 2A/Div
Time: 500µs/Div

UGATE Falling



CH1: V_{UGATE}, 20V/Div
CH2: V_{LGATE}, 10V/Div
CH3: V_{PHASE}, 10V/Div
Time: 20ns/Div

UGATE Rising

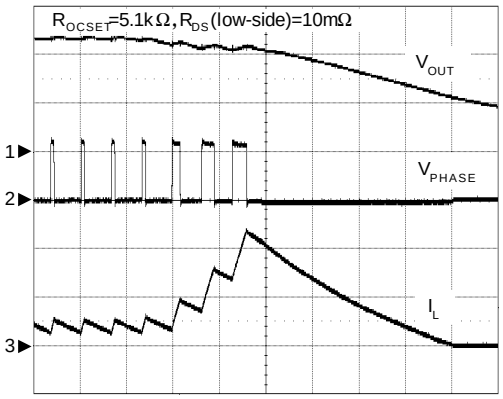


CH1: V_{UGATE}, 20V/Div
CH2: V_{LGATE}, 10V/Div
CH3: V_{PHASE}, 10V/Div
Time: 20ns/Div

Operating Waveforms (Cont.)

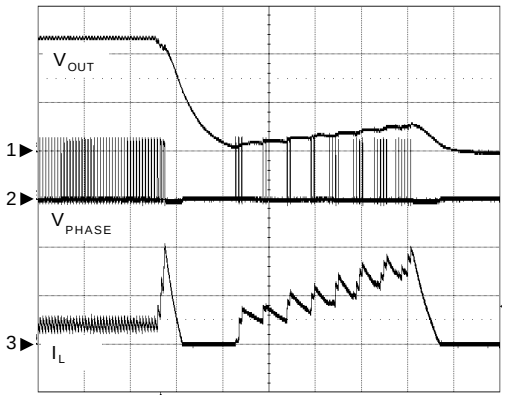
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Over-Current Protection



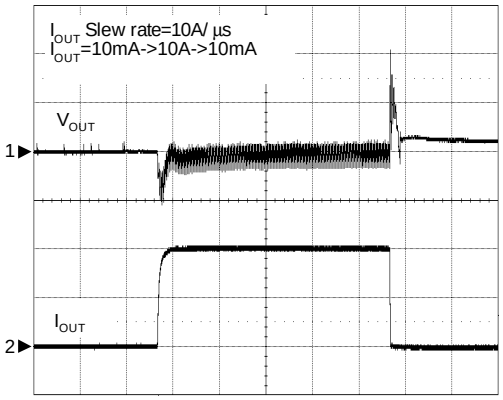
CH1: V_{OUT}, 500mV/Div
CH2: V_{PHASE}, 20A/Div
CH3: I_L, 10A/Div
Time: 5µs/Div

Over-Current Protection



CH1: V_{OUT}, 500mV/Div
CH2: V_{PHASE}, 20A/Div
CH3: I_L, 10A/Div
Time: 50µs/Div

Load Transient Response

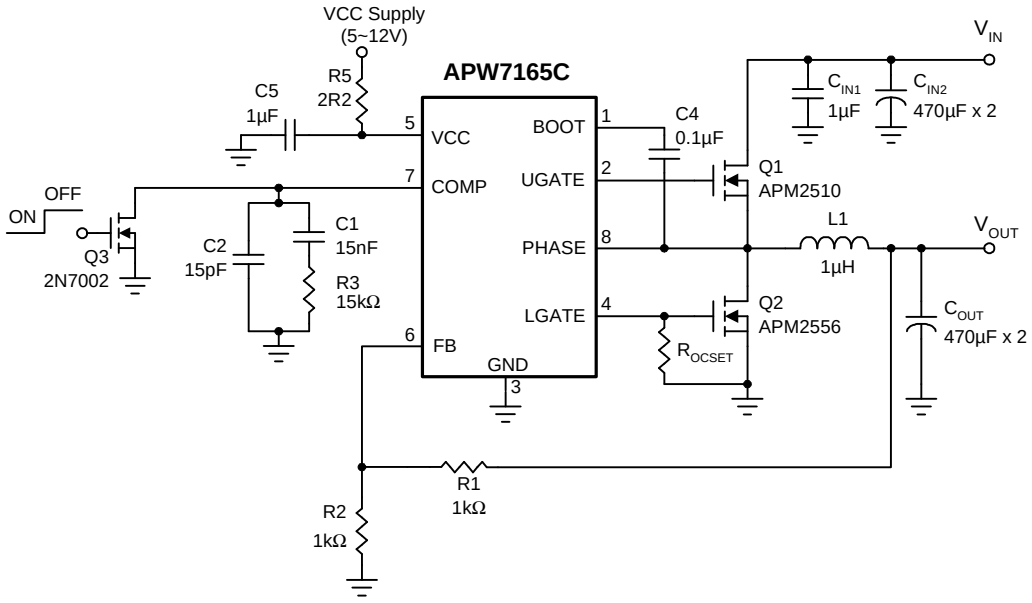


CH1: V_{OUT}, 50mV/Div
CH2: I_{OUT}, 5A/Div
Time: 100µs/Div

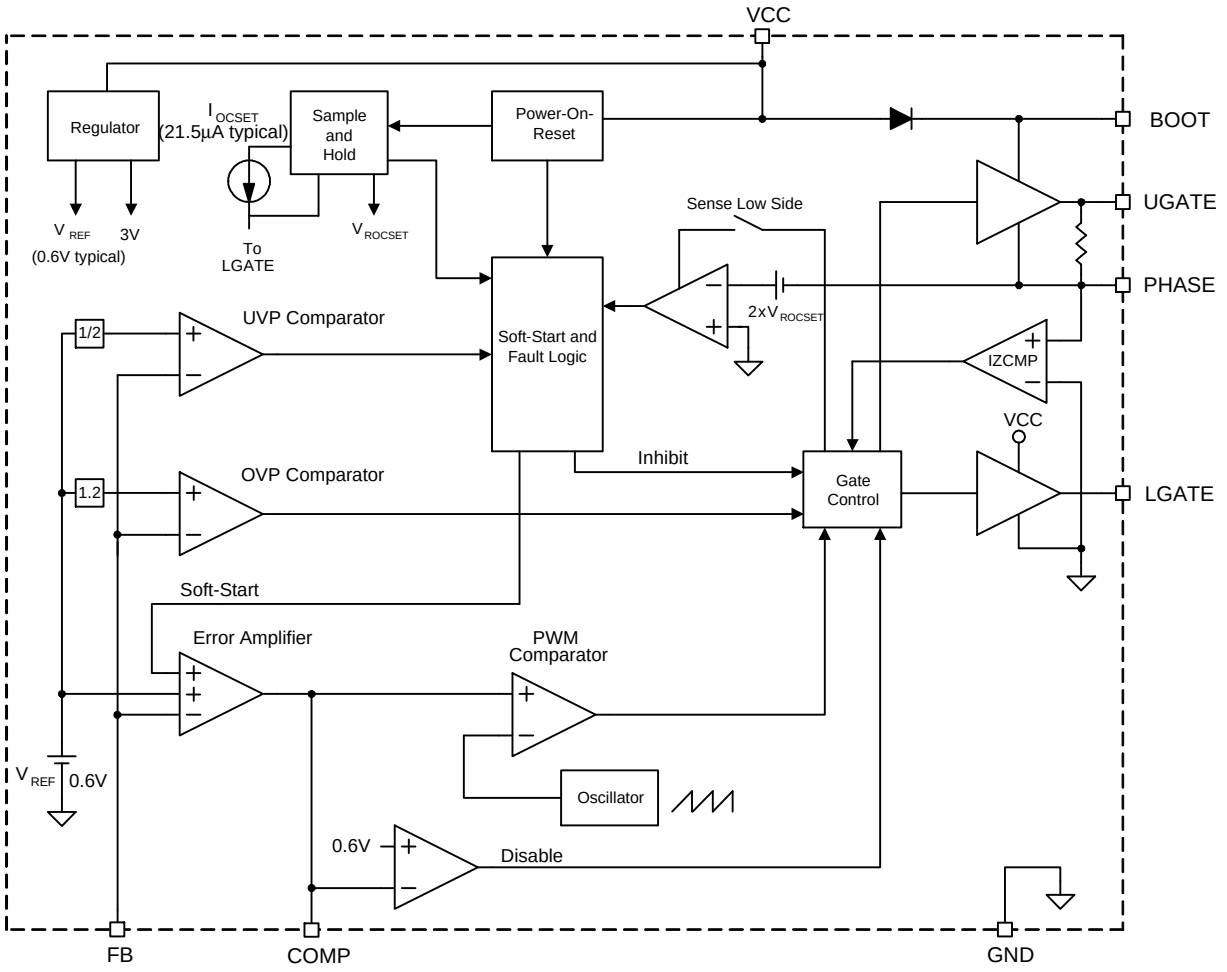
Pin Description

PIN		FUNCTION
NO.	NAME	
1	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, and the power supply voltage VCC, generates the bootstrap voltage for the high-side gate driver (UGATE).
2	UGATE	High-side Gate Driver Output. This pin is the gate driver for high-side MOSFET.
3	GND	Signal and Power ground. Connecting this pin to system ground.
4	LGATE	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It also used to set the maximum inductor current. Refer to the section in “Function Description” for detail.
5	VCC	Power Supply Input for Control Circuitry. Connect a nominal 5V to 12V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10μF) be connected to GND for noise decoupling.
6	FB	Feedback Input of Converter. The converter senses feedback voltage via FB and regulates the FB voltage at 0.6V. Connecting FB with a resistor-divider from the output sets the output voltage of the converter.
7	COMP	This is a multiplexed pin. During the soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin. Pulling COMP low ($V_{DISABLE}$ = 0.6V typical) will shut down the controller. When the pull-down device is released, the COMP pin will start to rise. When the COMP pin rises above the $V_{DISABLE}$ trip point, the APW7165C will begin a new initialization and soft-start cycle.
8	PHASE	This pin is the return path for the high-side gate driver. Connecting this pin to the high-side MOSFET source and connecting a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the low-side MOSFET for over-current protection.
9 (Exposed Pad)	GND	Thermal Pad. Connect this pad to the system ground plan for good thermal conductivity.

Typical Application Circuit



Block Diagram



Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7165C continually monitors the input supply voltage (VCC) and ensures that the IC has sufficient supply voltage and can work well. The POR function initiates a soft-start process while the VCC voltage exceeds the POR threshold; the POR function also inhibits the operations of the IC while the VCC voltage falls below the POR threshold.

Soft-Start

The APW7165C builds in a 40-steps digital soft-start to control the output voltage rise as well as limit the current surge at the start-up. During soft-start, the internal step voltage connected to the one of the positive inputs of the error amplifier replaces the reference voltage (0.6V typical) until the step voltage reaches the reference voltage. The digital soft-start circuit interval (shown as figure 1) depends on the switching frequency.

$$T_{SS} = (t_3 - t_2) = \frac{1}{F_{OSC}} \cdot 512$$

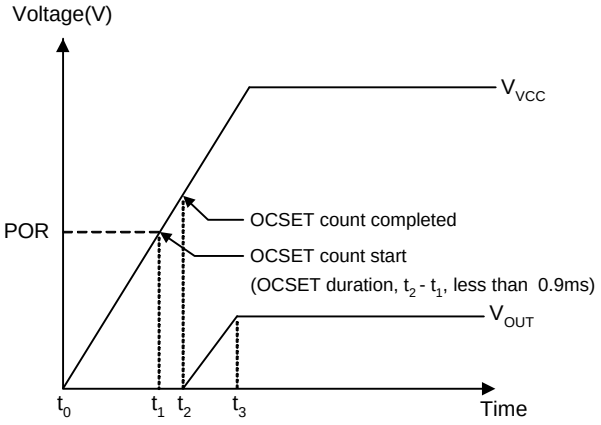


Figure 1. Soft-Start Interval

Over-Current Protection

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during on-state.

A resistor (R_{OCSET}), connected from the LGATE to the GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (21.5μA typical), flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET}. During the normal operation, the device holds V_{ROCSET} and stops the current source, I_{OCSET}. When the voltage across the low-side MOSFET exceeds the double V_{ROCSET} (2 x V_{ROCSET}), the IC shuts off the converter and then initiates a new soft-start process. After 2 over-current events are counted, the device is shut down and all the gate drivers (UGATE, LGATE, and DRIVE) are off. Both the output of the PWM converter and linear controller are latched to be floating.

The APW7165C has an internal OCP voltage, V_{OCP_MAX}, and the value is 0.3V minimum. When the R_{OCSET} x I_{OCSET} exceeds 0.3V or the R_{OCSET} is floating or not connected, the V_{ROCSET} will be the default value 0.3V. The over current threshold would be 0.7V across low-side MOSFET. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low-side)}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

- The $R_{DS(ON)}$ of low-side MOSFET is varied by temperature and gates to source voltage. Users should determine the maximum $R_{DS(ON)}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (19.5μA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the low-side MOSFET; I_{LIMIT} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ripple current

- The overshoot and transient peak current also should be considered.

Function Description (Cont.)

Under-Voltage Protection

The under-voltage function monitors the voltage on FB (V_{FB}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (50% V_{REF}), a fault signal is internally generated and the device turns off high-side and low-side MOSFETs. The converter is shut-down and the output is latched to be floating.

Over-Voltage Protection (OVP)

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 120% of the nominal output voltage, the APW7165C turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling OVP threshold, regulating the output voltage around the OVP threshold.

Shutdown and Enable

The APW7165C can be shut down or enabled by pulling low the voltage on COMP. The COMP is a dual-function pin. During normal operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin.
Pulling the COMP low ($V_{DISABLE}$ = 0.6V typical) places the controller into shutdown mode which UGATE and LGATE are pulled to PHASE and GND respectively.
When the pull-down device is released, the COMP voltage will start to rise. When the COMP voltage rises above the $V_{DISABLE}$ threshold, the APW7165C will begin a new initialization and soft-start process.

Pulse Skipping Mode (PSM)

At light loads, the inductor current may reach zero or reverse on each pulse. The low-side MOSFET is turned off by the current reversal comparator, IZCMP, to block the negative inductor current. In this condition, the converter enters discontinuous current mode operation.
At very light loads, the APW7165C will automatically skip pulses in pulse skipping mode operation to reduce switching losses as well as maintain output regulation for efficient applications.

Adaptive Shoot-Through Protection

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.
During turn-off of the low-side MOSFET, the LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay.
During turn-off of the high-side OCSFET, the UGATE-to-PHASE voltage is also monitored until it is below 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.6V. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right)$$

Where R1 is the resistor connected from V_{OUT} to FB and R2 is the resistor connected from FB to the GND.

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$ where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1µF to 1µF can connect between VCC and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

A tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP pin and ground should be added. The simplest loop compensation network is shown in Figure 5.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The FLC is the double poles of the LC filter, and FESR is the zero introduced by the ESR of the output capacitor.

Application Information (Cont.)

Compensation (Cont.)

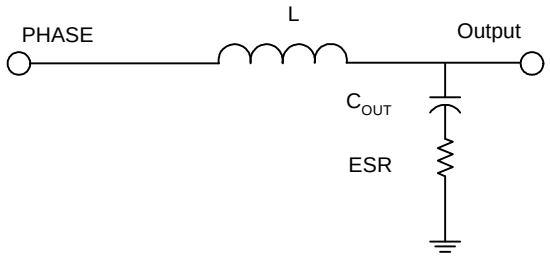


Figure 2. The Output LC Filter

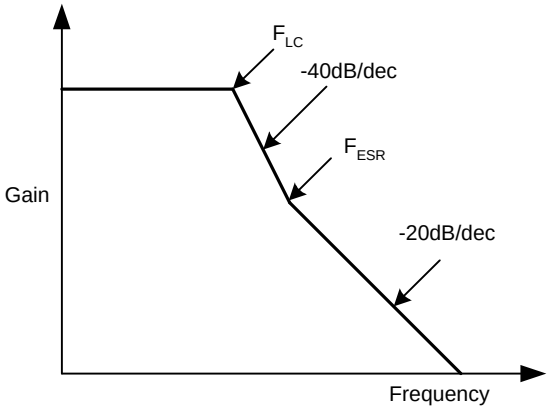


Figure 3. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

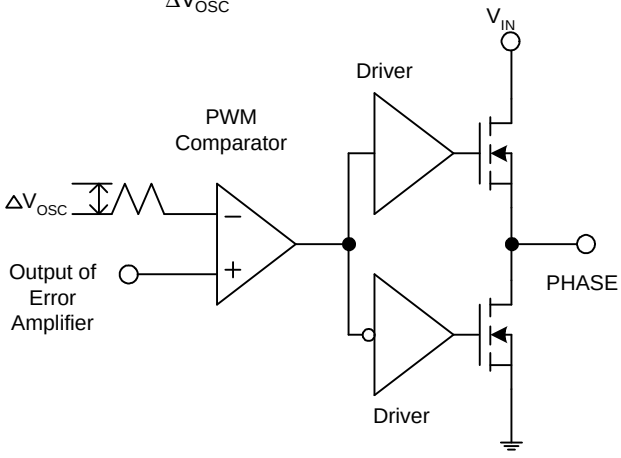


Figure 4. The PWM Modulator

The compensation circuit is shown in Figure 5. R3 and C1 introduce a zero and C2 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Z_O = gm \times \left[\left(R3 + \frac{1}{sC1}\right) // \frac{1}{sC2}\right]$$

$$= gm \times \frac{\left(s + \frac{1}{R3 \times C1}\right)}{s \times \left(s + \frac{C1 + C2}{R3 \times C1 \times C2}\right) \times C2}$$

The pole and zero of the compensation network are:

$$F_P \frac{1}{2 \times \pi \times R3 \times \frac{C1 \times C2}{C1 + C2}}$$

$$F_Z = \frac{1}{2 \times \pi \times R3 \times C1}$$

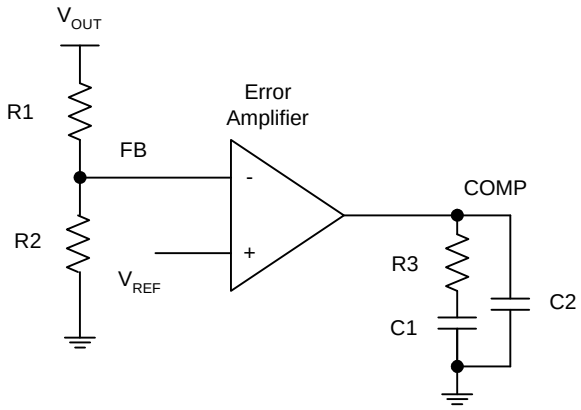


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R2}{R1 + R2} \times GAIN_{AMP}$$

Figure 6 shows the converter gain and the following guidelines will help to design the compensation network.

1.Select the desired zero crossover frequency F_O:

$(1/5 \sim 1/10) \times F_{SW} > F_O > F_Z$

Use the following equation to calculate R3:

$$R3 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R1 + R2}{R2} \times \frac{F_O}{gm}$$

Where:

gm = 667μA/V

Application Information (Cont.)

Compensation (Cont.)

2. Place the zero F_Z before the LC filter double poles F_{LC}:

$F_Z = 0.75 \times F_{LC}$

Calculate the C1 by the equation:

$$C1 = \frac{1}{2 \times \pi \times R1 \times 0.75 \times F_{LC}}$$

3. Set the pole at the half the switching frequency:

$F_P = 0.5 \times F_{SW}$

Calculate the C2 by the equation:

$$C2 = \frac{C1}{\pi \times R3 \times C1 \times F_{SW} - 1}$$

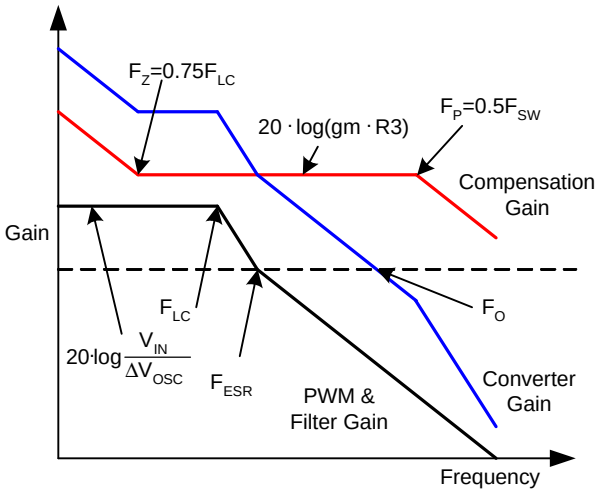


Figure 6. Converter Gain & Frequency

MOSFET Selection

The selection of the N-channel power MOSFETs is determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}), and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$P_{UPPER} = I_{OUT}^2 (1+ TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_{SW}$

$P_{LOWER} = I_{OUT}^2 (1+ TC)(R_{DS(ON)})(1-D)$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching internal, t_{sw}, is the function of the reverse transfer capacitance C_{RSS}. Figure 7 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

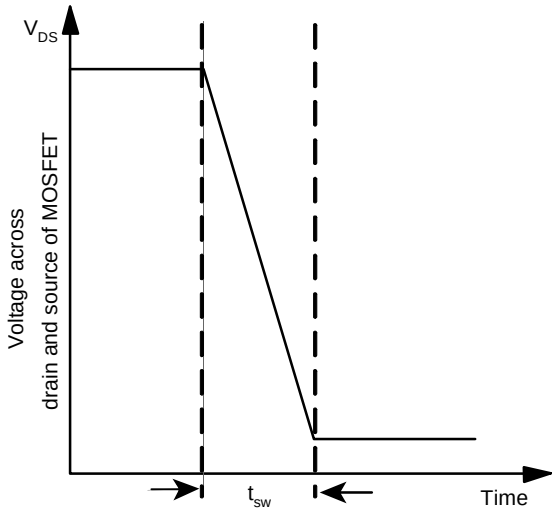


Figure 7. Switching waveform across MOSFET

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300kHz,the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting imped-

Application Information (Cont.)

Layout Consideration (Cont.)

ances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG and LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.

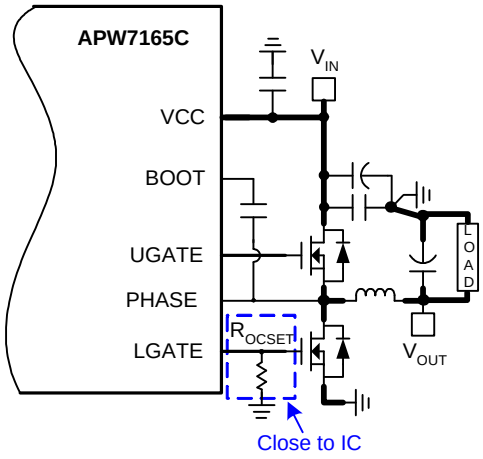
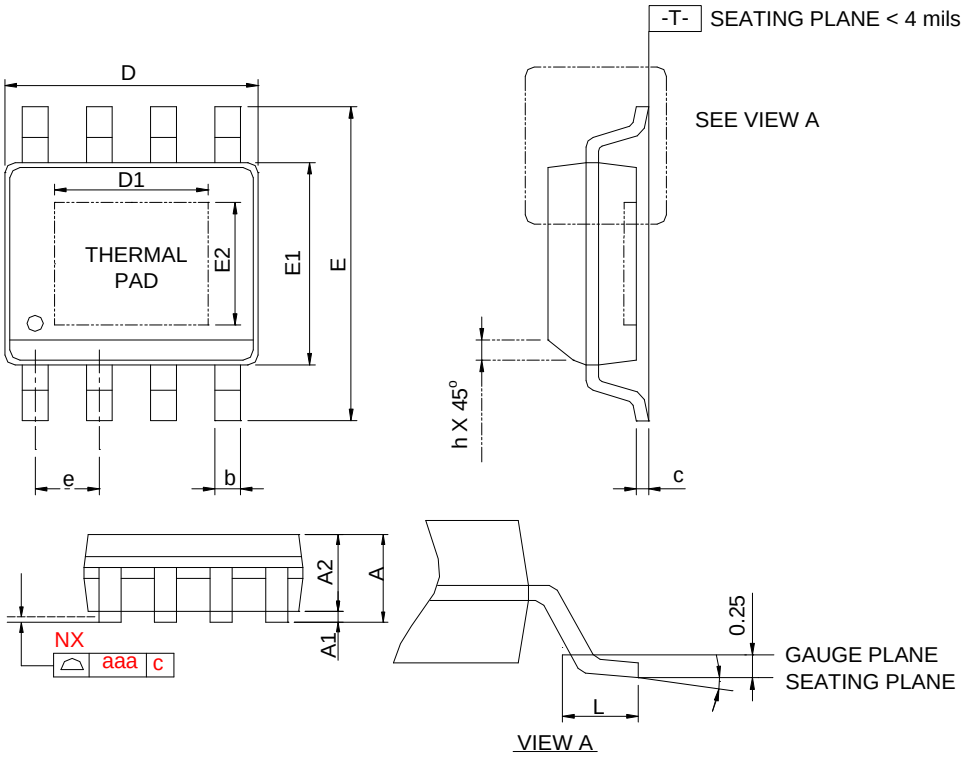


Figure 8. Layout Guidelines

Package Information

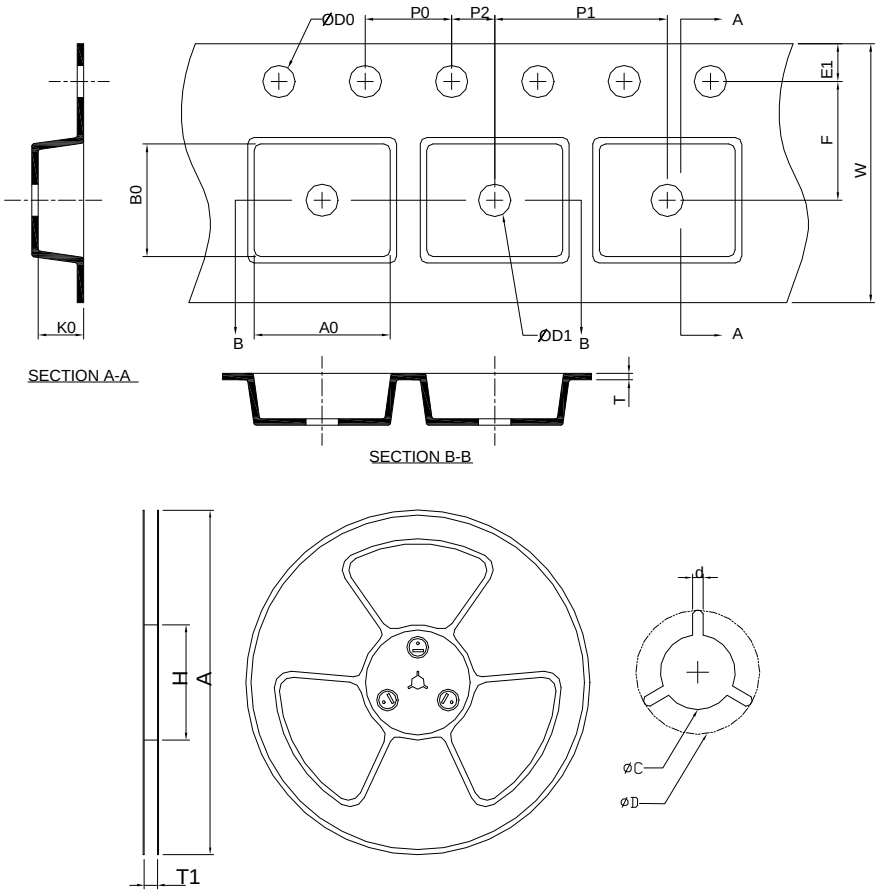
SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
°	0°C	8°C	0°C	8°C
aaa	0.10		0.004	

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

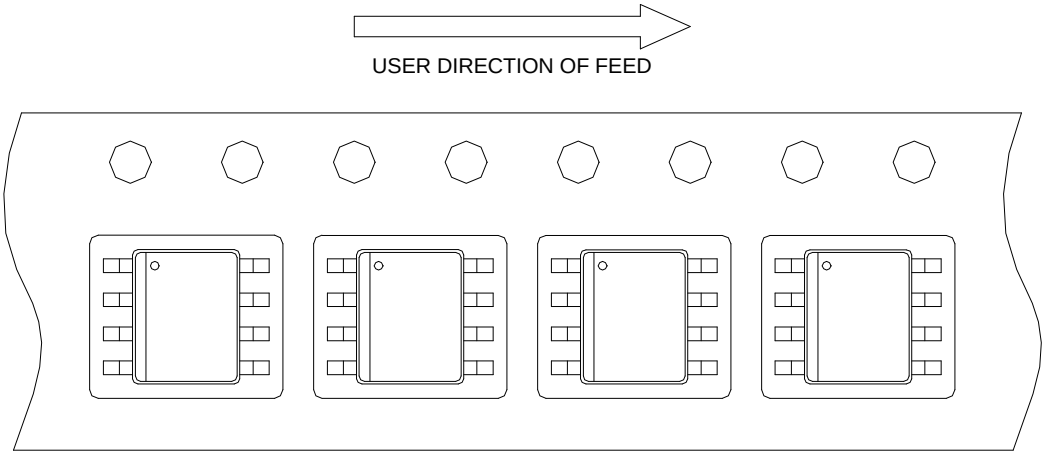
(mm)

Devices Per Unit

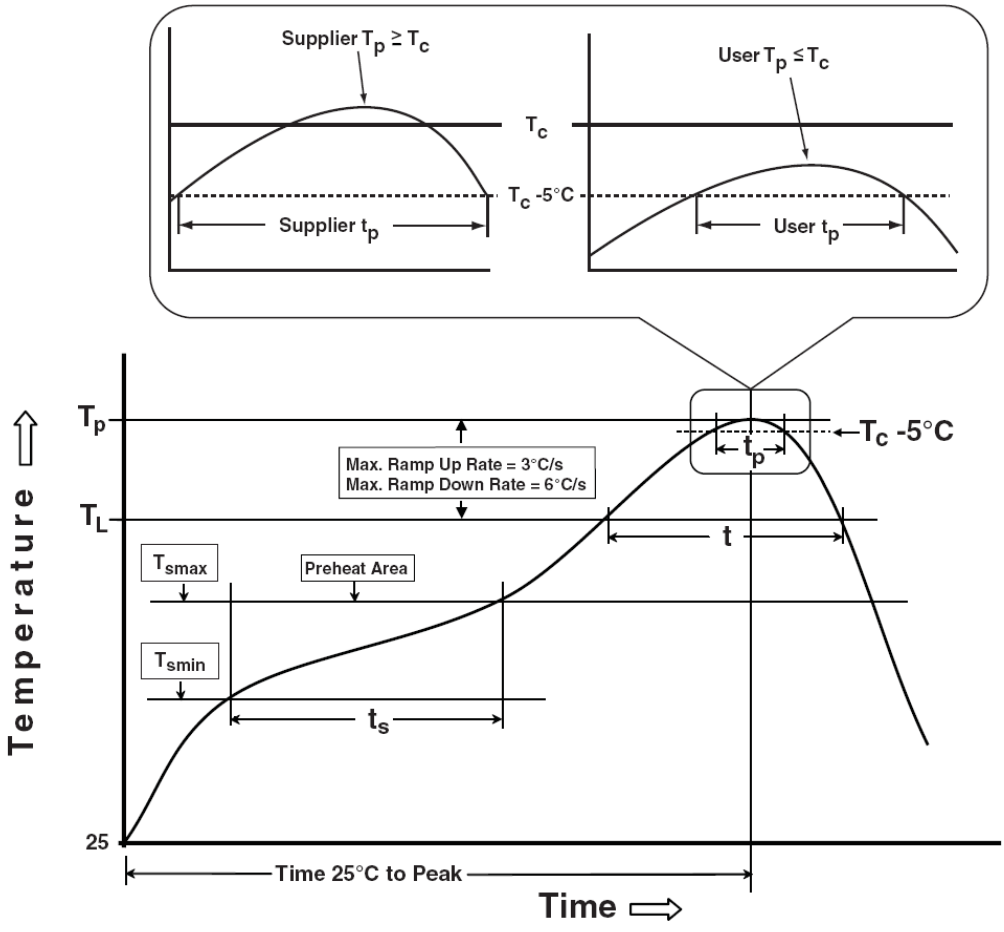
Package Type	Unit	Quantity
SOP-8P	Tape & Reel	2500

Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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