3A, Ultra Low Dropout (0.19V Typical) Linear Regulator

Features

- Ultra Low Dropout
  - 0.19V (Typical) at 3A Output Current
- Low ESR output Capasitor (Milti-layer Chip Capasitors (MLCC)) Applicable
- 0.8V Reference Voltage
- High Output Accuracy
- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and Short Current-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30㎂)
- Built in Shutdown/Enable Control with floating high/low Function
- Simple SOP-8P and TDFN3x3-10 Packages with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Motherboards, VGA Cards
- Notebook PCs
- Add-in Cards

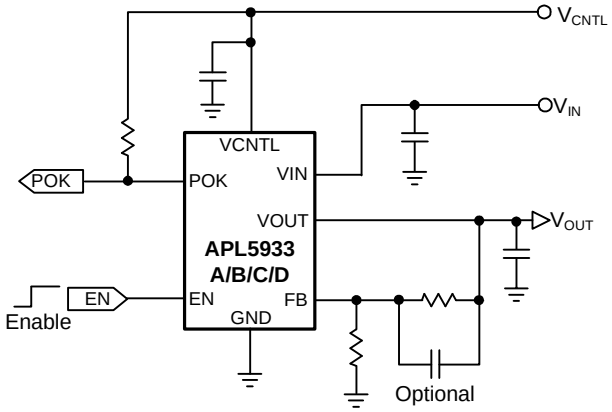
General Description

The APL5933A/B/C/D is a 3A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (V_{CNTL}) for the control circuitry, the other is a main supply Voltage(V_{IN}) for power conversion, to reduce power dissipation and provide extremely low dropout voltage.

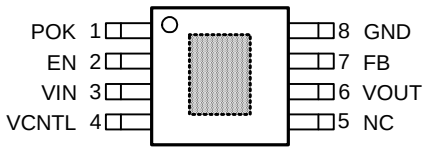
The APL5933A/B/C/D integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages on V_{CNTL} and V_{IN} pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. APL5933A/B/C/D can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V or ENB above 1.2V will shuts off the output.

The APL5933A/B/C/D is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

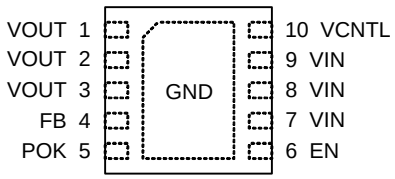
Simplified Application Circuit



Pin Configuration



APL5933A/B/C/D
SOP-8P
(Top View)



APL5933A/B/C/D
TDFN3x3-10
(Top View)

= Exposed Pad
(connected to ground plane for better heat dissipation)

= Exposed Pad
(connected to ground plane for better heat dissipation)

Ordering and Marking Information

APL5933 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- Enable Function / Turn On Delay

Turn On Delay Time
A : Initial High/2.7ms B : Initial High/0.5ms
C : Initial Low/2.7ms D : Initial Low/0.5ms
Package Code
KA : SOP-8P QB : TDFN3x3-10
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL5933A KA :	APL5933A XXXXX	XXXXX - Date Code
APL5933B KA :	APL5933B XXXXX	XXXXX - Date Code
APL5933C KA :	APL5933C XXXXX	XXXXX - Date Code
APL5933D KA :	APL5933D XXXXX	XXXXX - Date Code
APL5933A QB :	APL 5933A XXXXX	XXXXX - Date Code
APL5933B QB :	APL 5933B XXXXX	XXXXX - Date Code
APL5933C QB :	APL 5933C XXXXX	XXXXX - Date Code
APL5933D QB :	APL 5933D XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 6	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ V_{IN}+0.3	V
	POK to GND Voltage	-0.3 ~ 6	V
	EN, FB to GND Voltage	-0.3 ~ V_{CNTL}+0.3	V
$P_{D(MAX)}$	Maximum Power Dissipation, T_A=25°C SOP-8P TDFN3x3-10	 2.5 2	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-8P TDFN3x3-10	 50 60	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air SOP-8P TDFN3x3-10	 7 8	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P/TDFN3x3-10 is soldered directly on the PCB.

Recommended Operating Conditions (Note3)

Symbol	Parameter		Range	Unit
V_{CNTL}	VCNTL Supply Voltage		3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage		1.2 ~ 5.5	V
V_{OUT}	VOUT Output Voltage (when V_{CNTL}-V_{OUT}>2.1V)		0.8 ~ V_{IN} – V_{DROP}	V
I_{OUT}	VOUT Output Current		0 ~ 3	A
C_{OUT}	VOUT Output Capacitance	I_{OUT} = 0 to 3A at 25% nominal V_{OUT}	8 ~ 250	µF
ESR_{COUT}	ESR of VOUT Output Capacitor		0 ~ 200	mΩ
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified. These specifications apply over V_{CNTL}=5V, V_{IN}=1.8V, V_{OUT}=1.2V, and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_J=25°C.

Symbol	Parameter	Test Conditions			APL5933A/B/C/D			Unit
					Min.	Typ.	Max.	
SUPPLY CURRENT								
I_{VCNTL}	VCNTL Supply Current	EN=VCNTL, I_{OUT}=0A			-	1.0	1.5	mA
I_{SD}	VCNTL Supply Current at Shutdown	EN=GND or ENB=VCNTL			-	20	30	μA
	VIN Supply Current at Shutdown	V_{IN}=5.5V, EN=GND or ENB=VCNTL			-	-	1	μA
POWER-ON-RESET (POR)								
	Rising VCNTL POR Threshold				2.5	2.7	2.9	V
	VCNTL POR Hysteresis				-	0.4	-	V
	Rising VIN POR Threshold				0.8	0.9	1.0	V
	VIN POR Hysteresis				-	0.5	-	V
OUTPUT VOLTAGE								
V_{REF}	Reference Voltage	FB=VOUT			0.792	0.8	0.808	V
	Output Voltage Accuracy	V_{CNTL} =3.0~5.5V, I_{OUT}= 0~3A, T_J= -40~125 °C			-1.5	-	+1.5	%
	Load Regulation	I_{OUT}=0A ~3A			-	0.06	0.25	%
	Line Regulation	I_{OUT}=10mA, V_{CNTL}=3.0 ~ 5.5V			-0.15	-	+0.15	%/V
	VOUT Pull-Low Resistance	V_{CNTL}=5V, V_{EN}=0V or V_{ENB}=5V, V_{OUT}<0.8V			-	80	-	Ω
	FB Input Current	V_{FB}=0.8V			-100	-	100	nA
DROPOUT VOLTAGES								
V_{DROP}	VIN-to-VOUT Dropout Voltage	V_{CNTL}=5.0V, I_{OUT}=3A	V_{OUT}=2.5V	T_J=25°C	-	0.24	0.29	V
				T_J=-40~125°C	-	-	0.39	
			V_{OUT}=1.8V	T_J=25°C	-	0.22	0.26	
				T_J=-40~125°C	-	-	0.35	
			V_{OUT}=1.2V	T_J=25°C	-	0.21	0.25	
				T_J=-40~125°C	-	-	0.34	
PROTECTIONS								
I_{LIM}	Current-Limit Level	T_J=25°C			3.6	4.0	4.6	A
		T_J= -40 ~ 125°C			3.2	-	-	
I_{SHORT}	Short Current-Limit Level	V_{FB}<0.2V			-	0.9	-	A
	Short Current-Limit Blanking Time	From beginning of soft-start			1.5	3.4	-	ms
T_{SD}	Thermal Shutdown Temperature	T_J rising			-	150	-	°C
	Thermal Shutdown Hysteresis				-	50	-	°C

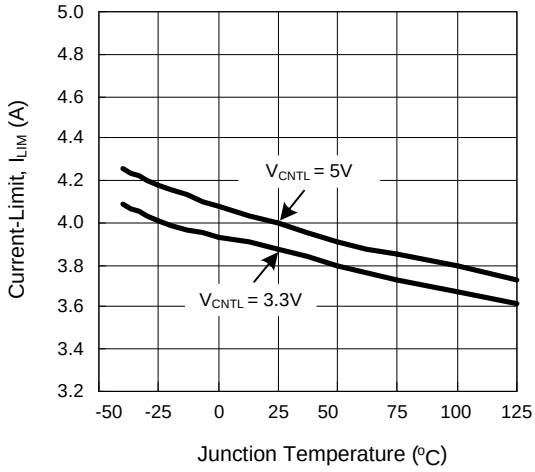
Electrical Characteristics (Cont.)

Unless otherwise specified. These specifications apply over V_{CNTL}=5V, V_{IN}=1.8V, V_{OUT}=1.2V, and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_J=25°C.

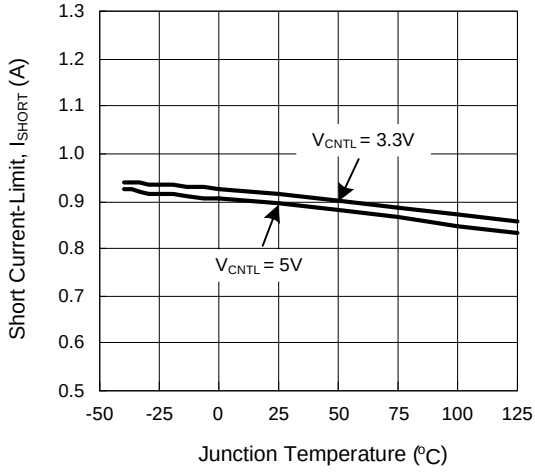
Symbol	Parameter	Test Conditions	APL5933A/B/C/D			Unit
			Min.	Typ.	Max.	
ENABLE AND SOFT-START						
V_{EN}	EN Logic Input Threshold	V_{CNTL} = 3V to 5.5V	0.5	0.8	1.1	V
	EN Hysteresis		-	0.1	-	V
I_{EN}	EN Pull-High Current	EN = GND (AL5933A/B)	-	3	-	µA
	EN Pull-Low Current	V_{EN} = 5V(APL5933C/D)	-	3	-	µA
t_{SS}	Soft-Start Interval	V_{OUT} = 10% to 90%	1	2	4	ms
$t_{D(ON)}$	Turn On Delay	APL5933A/C, from being enabled to V_{OUT} rising 10%, T_J=25°C	1.5	2.7	4	ms
		APL5933B/D, from being enabled to V_{OUT} rising 10%, T_J=25°C	0.3	0.5	0.7	ms
POWER-OK AND DELAY						
V_{THPOK}	Rising POK Threshold Voltage	V_{FB} rising	90	92	94	%
	POK Threshold Hysteresis		-	8	-	%
	POK Pull-Low Voltage	POK sinks 5mA	-	0.25	0.4	V
	POK Denounce Interval	V_{FB}<falling POK voltage threshold	-	10	-	µs
	POK Delay Time	From V_{FB} =V_{THPOK} to rising edge of the V_{POK}	1	2	4	ms

Typical Operating Characteristics

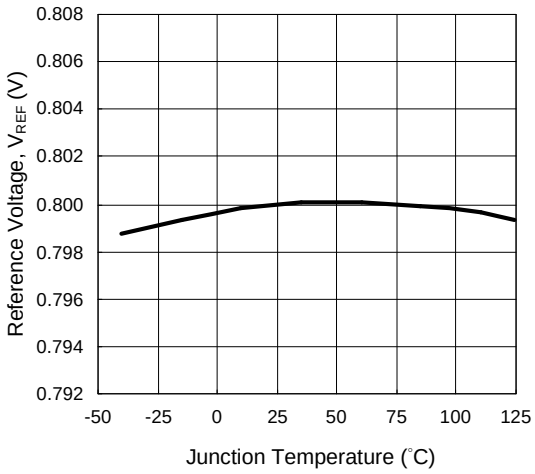
Current-Limit vs. Junction Temperature



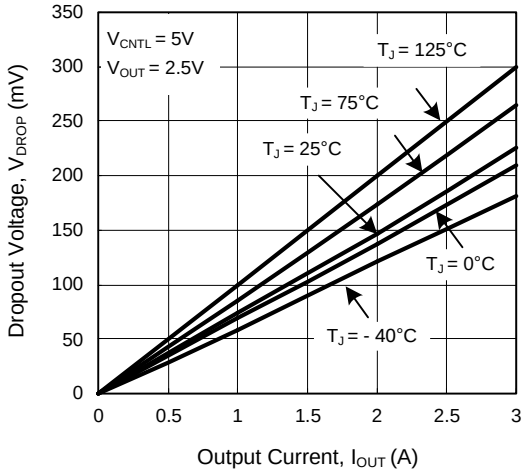
Short Current-Limit vs. Junction Temperature



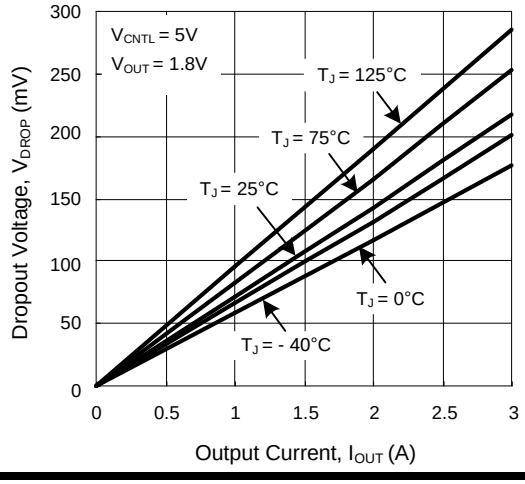
Reference Voltage vs. Junction Temperature



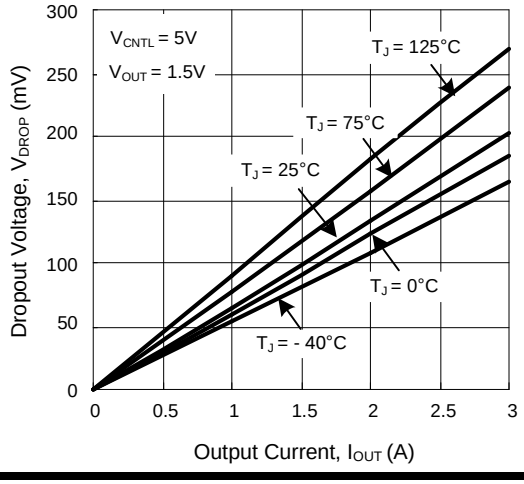
Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current

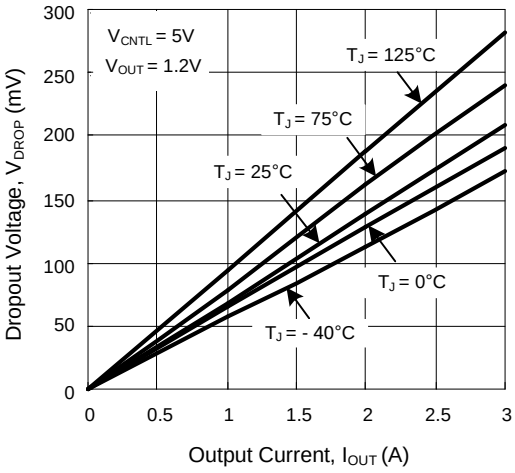


Dropout Voltage vs. Output Current

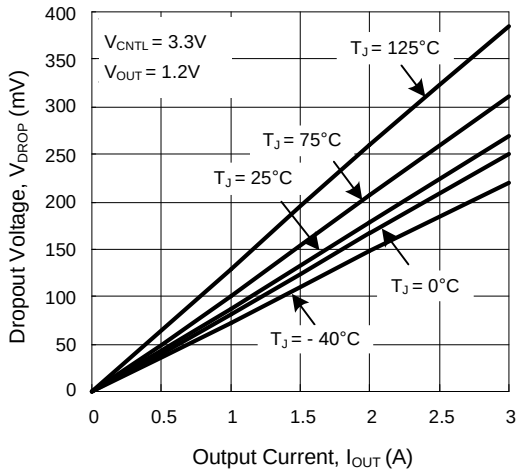


Typical Operating Characteristics

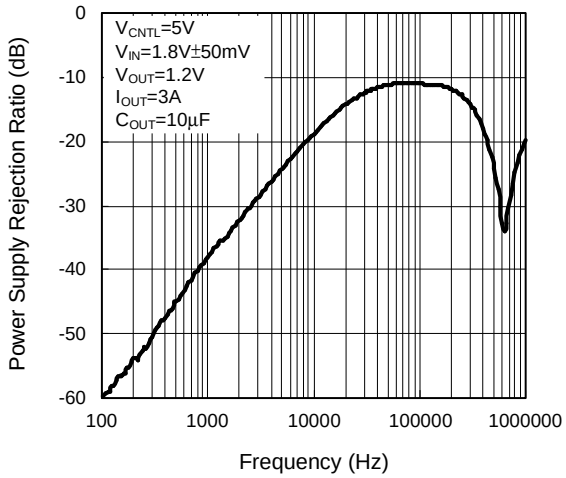
Dropout Voltage vs. Output Current



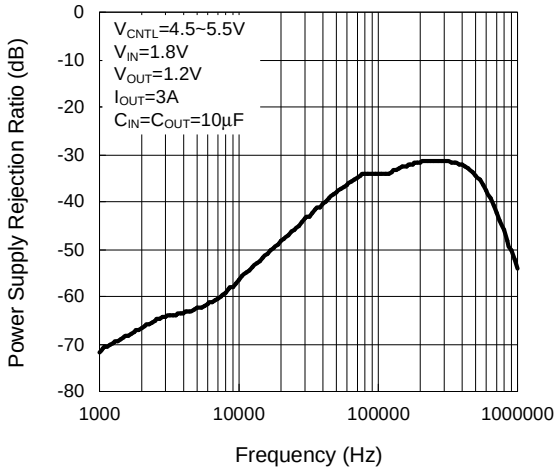
Dropout Voltage vs. Output Current



VIN Power Supply Rejection Ratio (PSRR)



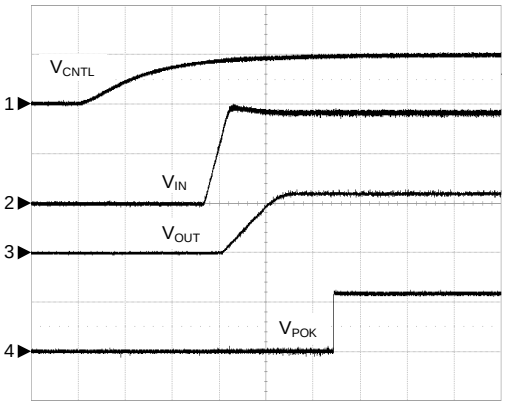
VCNTL Power Supply Rejection Ratio (PSRR)



Operating Waveforms

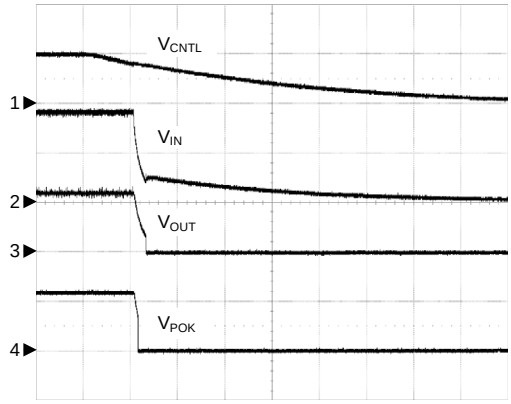
Refer to the typical application circuit. The test condition is V_{IN}=1.8V, V_{CNTL}=5V, V_{OUT}=1.2V, T_A= 25°C unless otherwise specified.

Power On



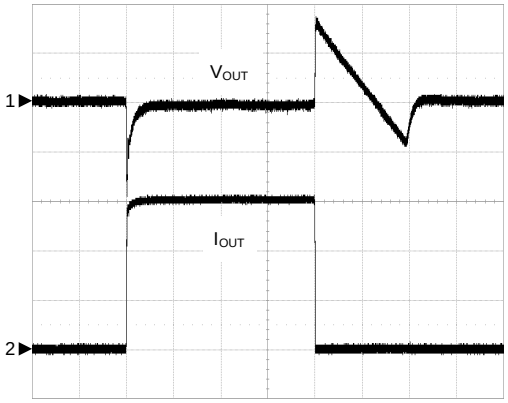
C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{POK}, 1V/Div, DC
TIME: 2ms/Div

Power Off



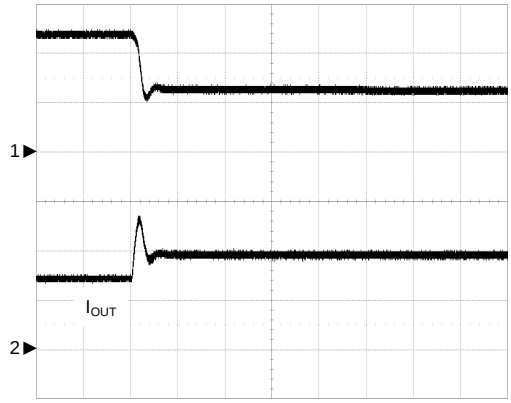
C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{POK}, 1V/Div, DC
TIME: 1ms/Div

Load Transient Response



I_{OUT}=10mA to 3A to 10mA (rise / fall time = 1µs)
C_{OUT}=10µF, C_{IN}=10µF
CH1: V_{OUT}, 50mV/Div, DC offset 1.2V
CH2: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Over Current Protection

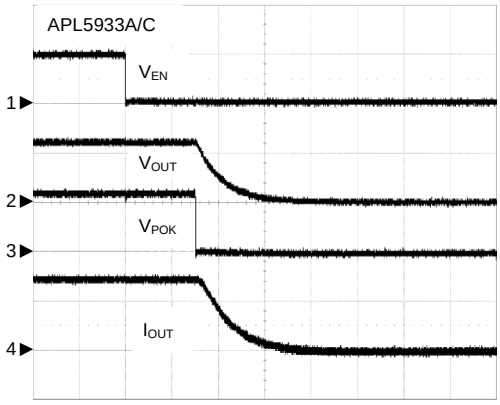


C_{OUT}=10µF, C_{IN}=10µF, R_{OUT}= 0.4Ω to 0.1Ω
CH1: V_{OUT}, 0.5V/Div, DC
CH2: I_{OUT}, 2A/Div, DC
TIME: 50µs/Div

Operating Waveforms

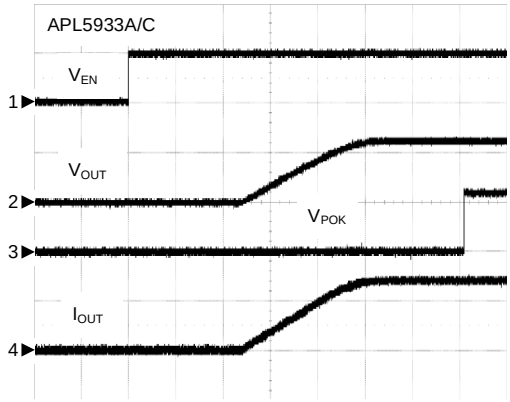
Refer to the typical application circuit. The test condition is V_{IN}=1.8V, V_{CNTL}=5V, V_{OUT}=1.2V, T_A= 25°C unless otherwise specified.

Shutdown



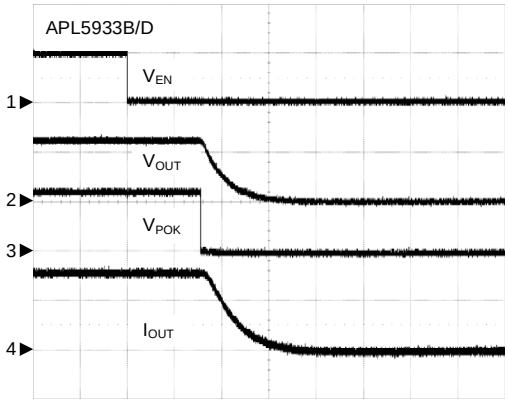
C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 1V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 5µs/Div

Enable



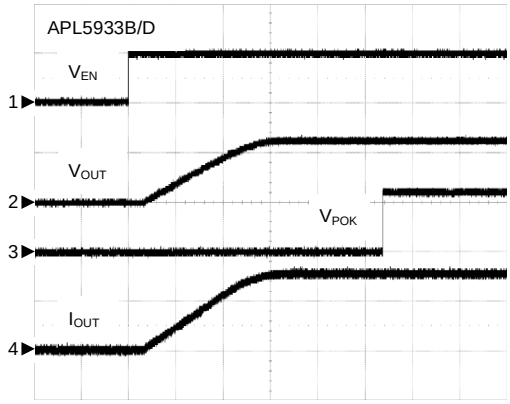
C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 1V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

Shutdown



C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 1V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 5µs/Div

Enable



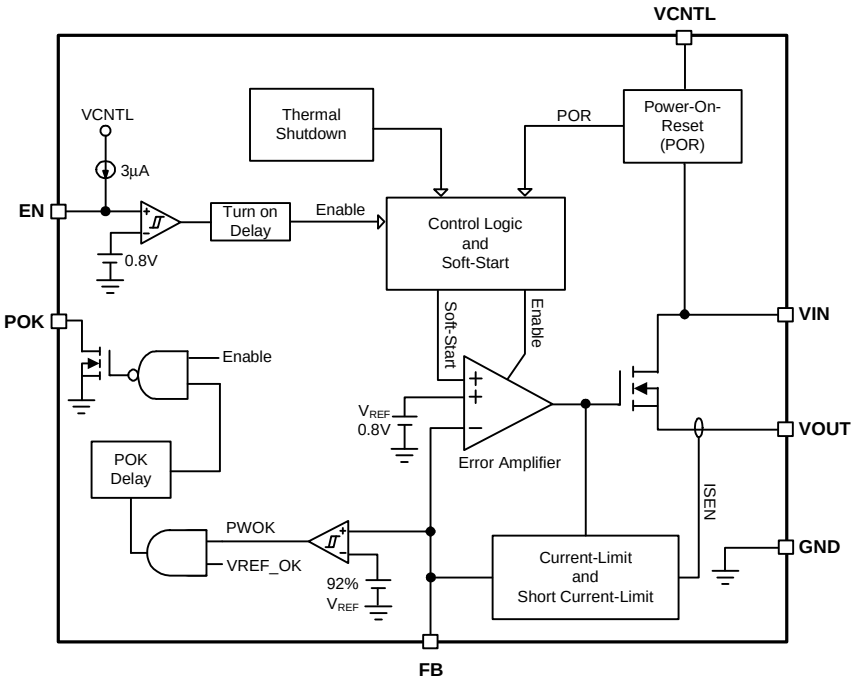
C_{IN}=10µF, C_{OUT}=10µF, R_L=0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 1V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

Pin Description

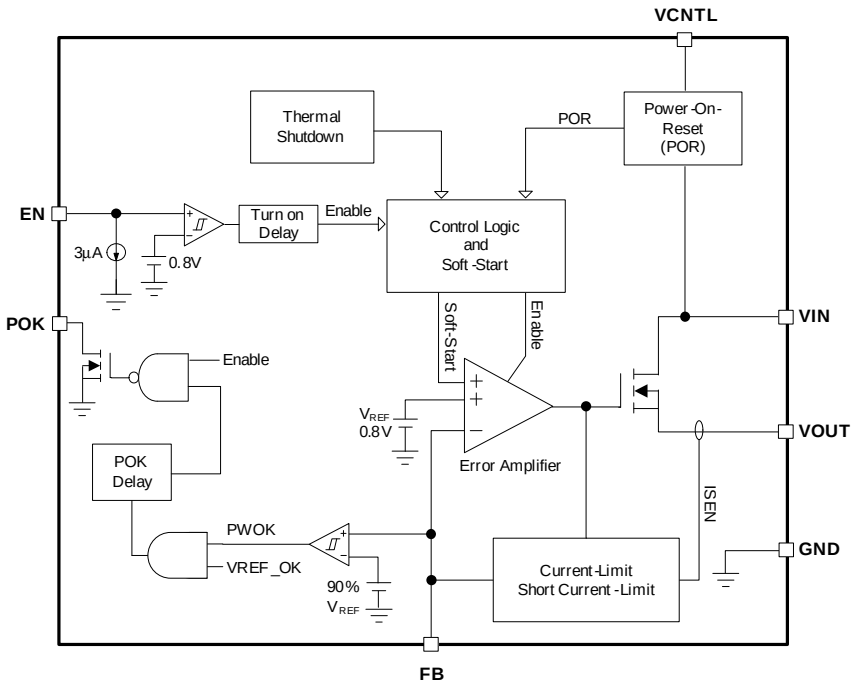
PIN			FUNCTION
NO.		NAME	
SOP-8P	TDFN3x3-10		
1	5	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	6	EN (APL5933A/B)	Active-High enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new turn on delay and soft-start process. When leave this pin open, an internal pull-up current (3μA typical) pulls the EN voltage and enables the regulator.
		EN (APL5933C/D)	Active-High enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new turn on delay and soft-start process. When leave this pin open, an internal pull-low current (3μA typical) pulls the EN voltage and shuts down the regulator.
3	7,8,9	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose
4	10	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
5	-	NC	No Connection.
6	1,2,3	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10μF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 3A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
7	4	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
8	Exposed Pad	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
Exposed Pad	-	-	P-Type Substrate connection of the chip. Connect this pad to system ground plane for good thermal conductivity.

Block Diagram

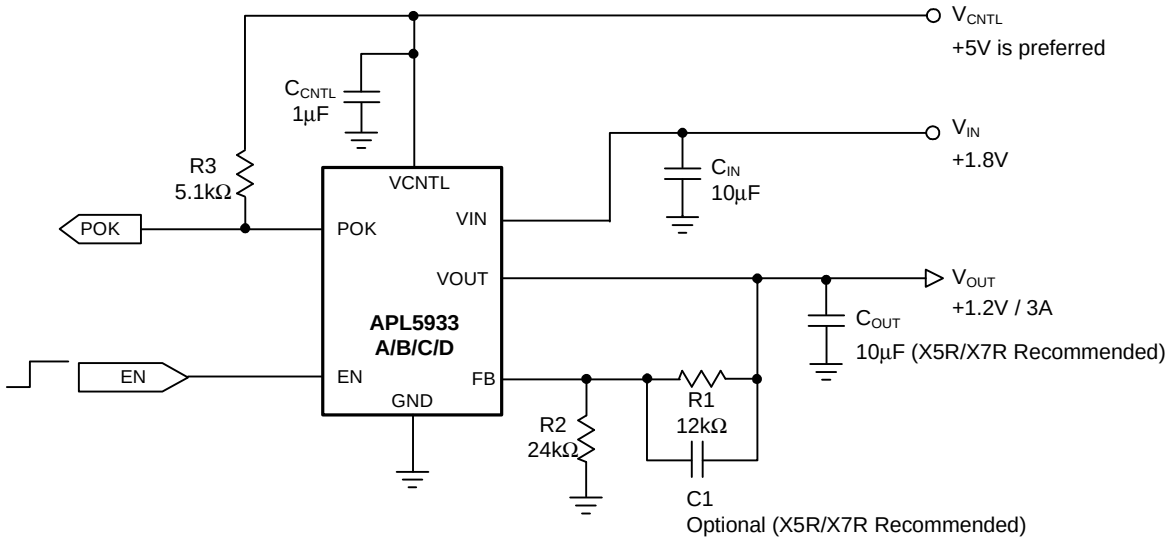
APL5933A/B



APL5933C/D



Typical Application Circuit



Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless of the output status when one of the supply voltages falls below its falling POR voltage threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 2ms.

Output Voltage Regulation

An error amplifier working with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

Current-Limit Protection

The APL5933A/B/C/D monitors the current flowing through the output NMOS and limits the maximum current to prevent load and APL5933A/B/C/D from damages during current overload conditions.

Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 0.9A (typical) when the voltage on FB pin falls below 0.2V (typical) during current overload or short-circuit conditions.
The short current-limit function is disabled for successful start-up during soft-start interval.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5933A/B/C/D. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down.

The regulator regulates the output again through initiation of a new soft-start process after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 50°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, the device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Enable Control (APL5933A/B)

The APL5933A/B has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new turn on delay and soft-start cycle. When left open, this pin is pulled up by an internal current source (3μA typical) to enable normal operation. It's not necessary to use an external transistor to save cost.

Enable Control (APL5933C/D)

The APL5933C/D has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new turn on delay and soft-start cycle. When left open, this pin is pulled low by an internal current sink (3μA typical) to shutdown the regulator.

Power-OK and Delay

The APL5933A/B/C/D indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK voltage threshold (V_{THPOK}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate the output is ok. As the V_{FB} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 10μs typical).

Application Information

Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage.

Output Capacitor

The APL5933A/B/C/D requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as output capacitors.

During load transients, the output capacitors which is depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the APL5933A/B/C/D and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

Input Capacitor

The APL5933A/B/C/D requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10µF at least. However, if the drop of the input voltage is not cared, the input capacitance can be less than 10µF. More capacitance reduces the variations of the supply voltage on VIN pin.

Setting The Output Voltage

The output voltage is programmed by the resistor divider connected to FB pin. The preset output voltage is calculated by the following equation :

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{..... (V)}$$

where R1 is the risistor connected from VOUT to FB with Kelvin sensing connection and R2 is the risistor connected from FB to GND. A bypass capacitor(C1) may be connected with R1 in parallel to improve load transient response and stability.

Operation Region and Power Dissipation

The APL5933 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

Where (T_J-T_A) is the temperature difference between the junction and ambient air. θJA is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = \frac{(150-25)}{50}$$
$$= 2.5(W) \quad \text{.....for SOP-8P package.}$$

$$P_{D(max)} = \frac{(150-25)}{60}$$
$$= 2.08(W) \quad \text{.....for TDFN3x3-10 package.}$$

For normal operation, do not exceed the maximum junction temperature of T_J = 125°C. The calculated power dissipation should less than:

$$P_D = \frac{(125-25)}{50}$$
$$= 2(W) \quad \text{.....for SOP-8P package.}$$

$$P_D = \frac{(125-25)}{60}$$
$$= 1.66(W) \quad \text{.....for TDFN3x3-10 package.}$$

Application Information (Cont.)

Layout Consideration (See Figure 1)

1. Please solder the Exposed Pad on the system ground pad on the top-layer of PCBs. The ground pad must have wide size to conduct heat into the ambient air through the system ground plane and PCB as a heat sink.
2. Please place the input capacitors for VIN and VCNTL pins near the pins as close as possible for decoupling high-frequency ripples.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
4. To place APL5933A/B/C/D and output capacitors near the load reduces parasitic resistance and inductance for excellent load transient response.
5. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
6. Large current paths, shown by bold lines on the figure 1, must have wide tracks.
7. Place the R1, R2, and C1 (option) near the APL5933A/B/C/D as close as to avoid noise coupling.
8. Connect the ground of the R2 to the GND pin by using a dedicated track.
9. Connect the one pin of the R1 to the load for Kelvin sensing.
10. Connect one pin of the C1 (option) to the VOUT pin for reliable feedback compensation.

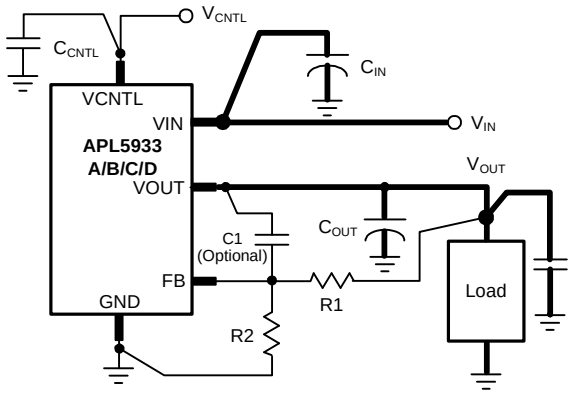


Figure 1.

Thermal Consideration

Refer to the figure 2, the SOP-8P is a cost-effective package featuring a small size like a standard SOP-8 and a bottom exposed pad to minimize the thermal resistance of the package, being applicable to high current applications. The exposed pad must be soldered to the top-layer ground plane. It is recommended to connect the top-layer ground pad to the internal ground plan by using vias. The copper of the ground plane on the top-layer conducts heat into the PCB and ambient air. Please enlarge the area of the top-layer pad and the ground plane to reduce the case-to-ambient resistance (θ_{CA}).

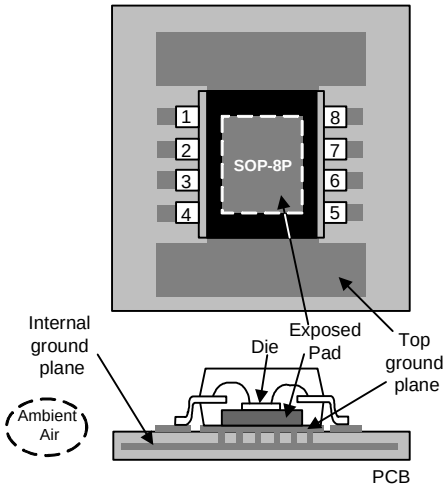
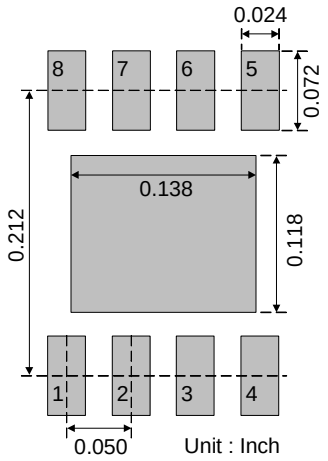


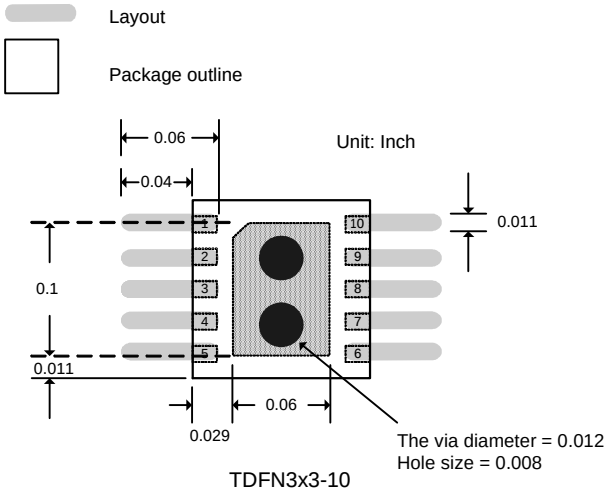
Figure 2.

Application Information (Cont.)

Recommanded Minimum Footprint



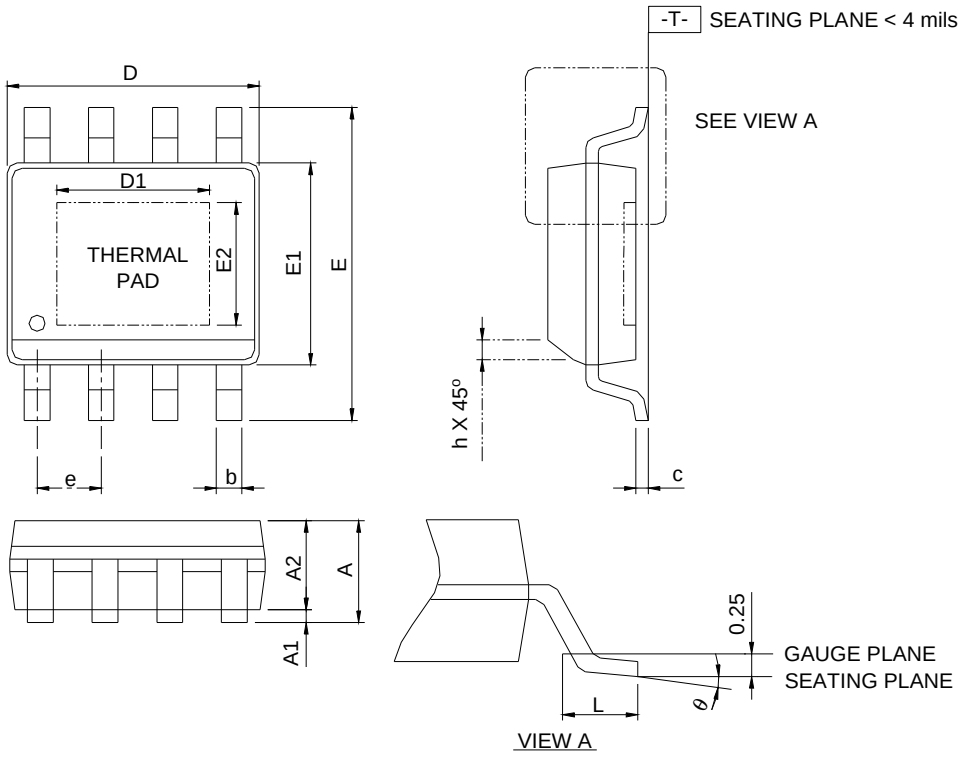
SOP-8P



TDFN3x3-10

Package Information

SOP-8P

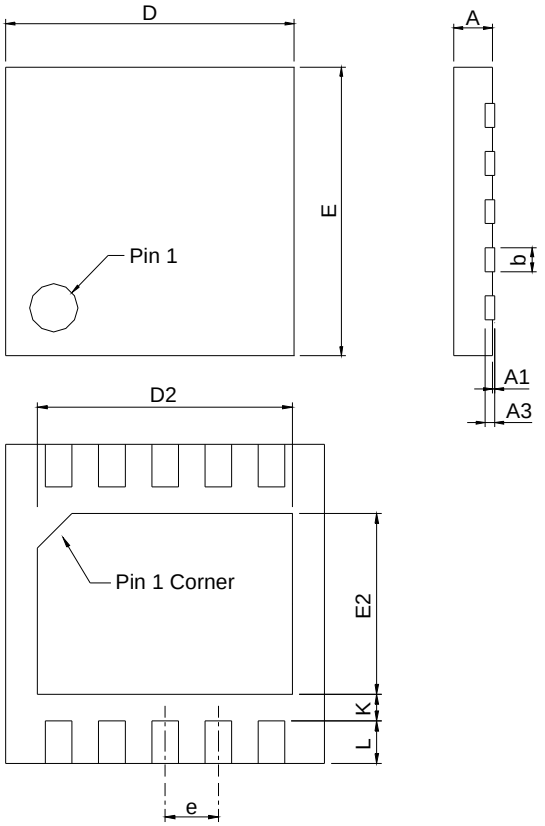


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

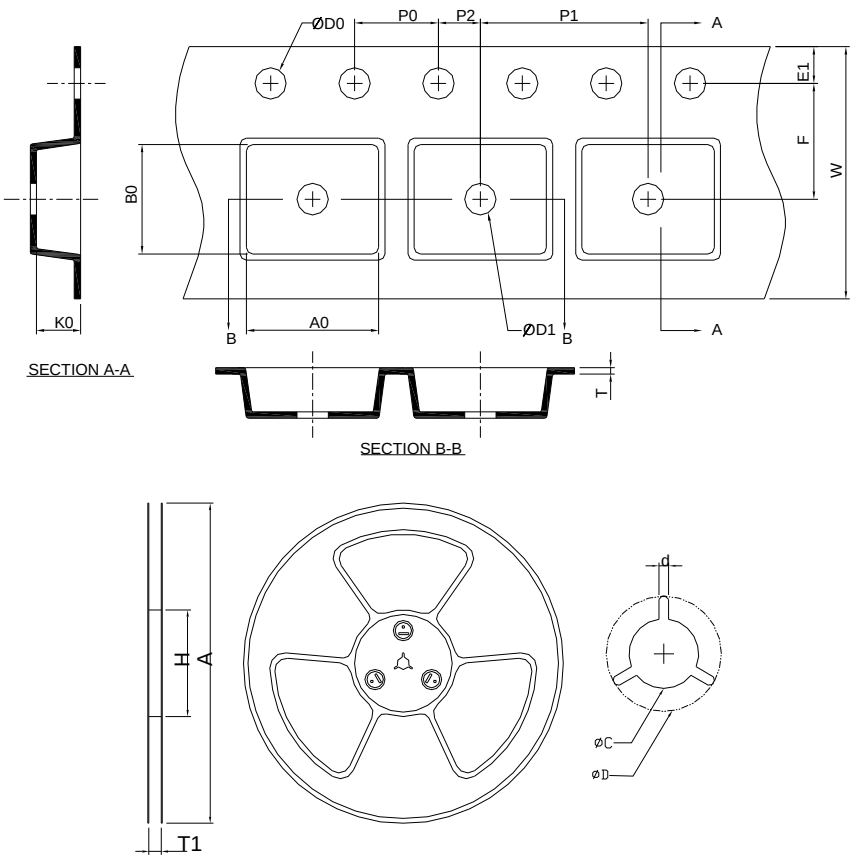
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

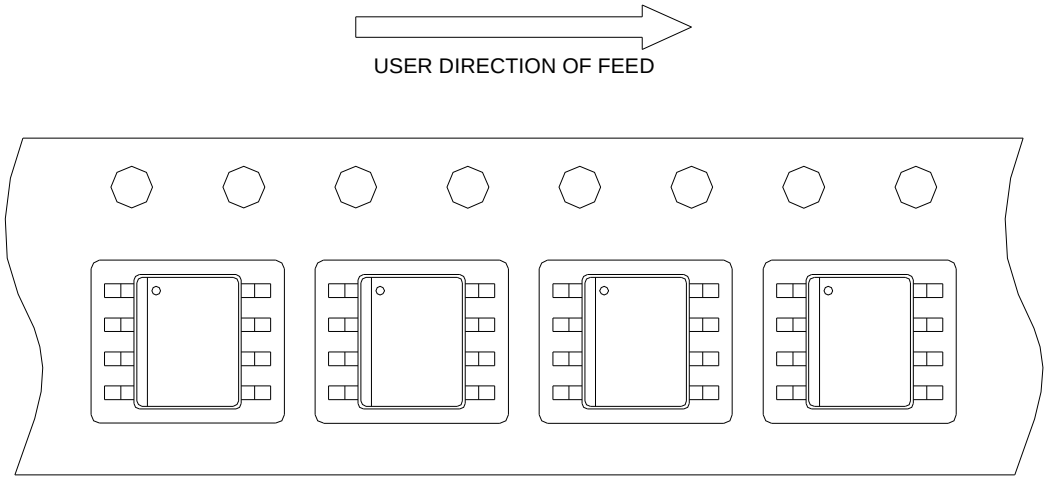
(mm)

Devices Per Unit

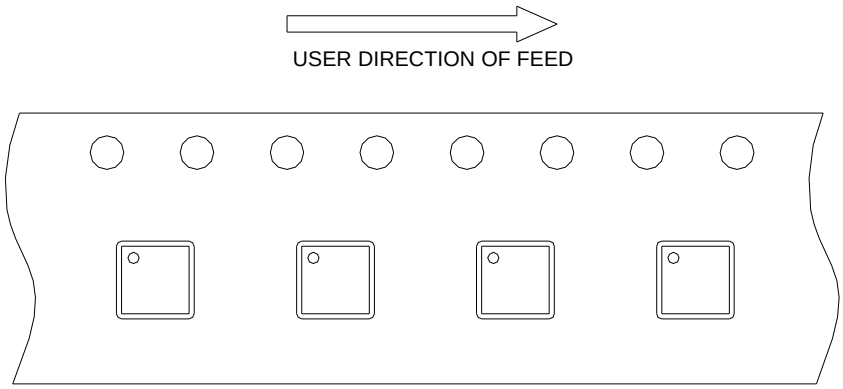
Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500
TDFN-3x3-10	Tape & Reel	3000

Taping Direction Information

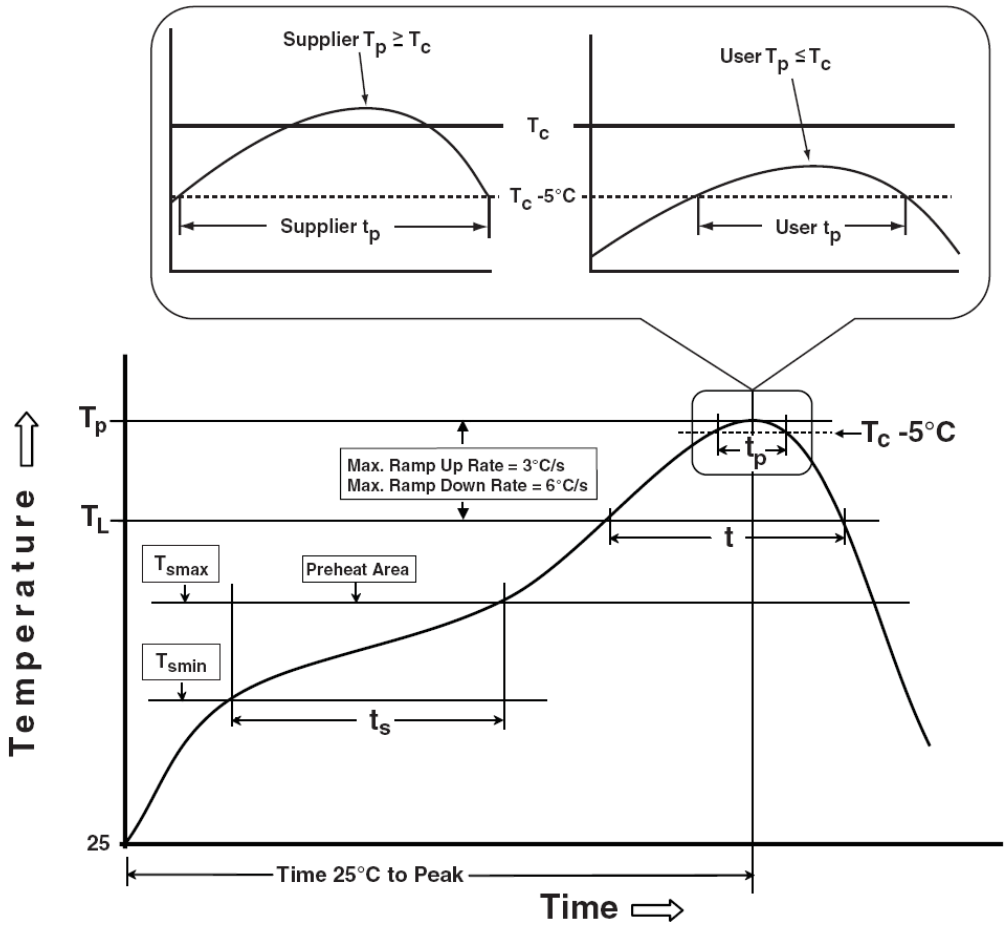
SOP-8P



TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
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