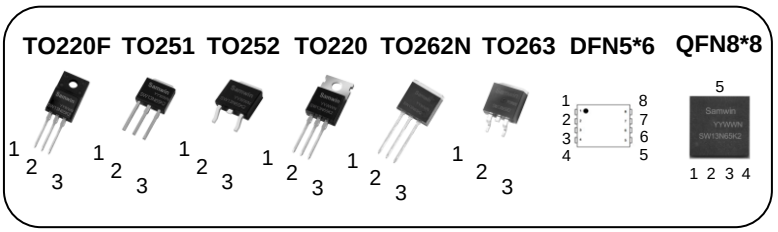
*N-channel Enhanced mode TO-220F/TO-251/TO-252/TO-220/TO-262N/TO-263/ DFN5*6/QFN8*8 MOSFET*

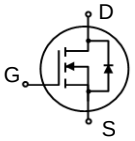
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 0.24Ω) @V_{GS}=10V
- Low Gate Charge (Typ 28nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: LED, Charger, Adaptor



TO220F/TO251/TO252/TO220/TO262N/TO263:1. Gate 2. Drain 3. Source
DFN5*6: 4.Gate 5,6,7,8. Drain 1,2,3 Source
QFN8*8:1. Gate 2,3,4.Source 5.Drain

BV_{DSS} : 650V
I_D : 13A
$R_{DS(ON)}$: 0.24Ω



General Description

This power MOSFET is produced with super junction advanced technology of SAMWIN.
This technology enable the power MOSFET to have better characteristics, Including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

LEAD-FREE RoHS

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW F 13N65K2	SW13N65K2	TO-220F	TUBE
2	SW I 13N65K2	SW13N65K2	TO-251	TUBE
3	SW D 13N65K2	SW13N65K2	TO-252	REEL
4	SW P 13N65K2	SW13N65K2	TO-220	TUBE
5	SW J 13N65K2	SW13N65K2	TO-262N	TUBE
6	SW B 13N65K2	SW13N65K2	TO-263	TUBE
7	SW HA 13N65K2	SW13N65K2	DFN5*6	REEL
8	SW HC 13N65K2	SW13N65K2	QFN8*8	REEL

Absolute maximum ratings

Symbol	Parameter	Value								Unit
		TO220F	TO251	TO252	TO220	TO262N	TO263	DFN5*6	QFN8*8	
V_{DSS}	Drain to source voltage	650								V
I_D	Continuous drain current (@T_C=25°C)	13*								A
	Continuous drain current (@T_C=100°C)	8.2*								A
I_{DM}	Drain current pulsed (note 1)	39								A
V_{GS}	Gate to source voltage	±30								V
E_{AS}	Single pulsed avalanche energy (note 2)	200								mJ
E_{AR}	Repetitive avalanche energy (note 1)	21								mJ
dv/dt	MOSFET dv/dt ruggedness (@VDS=0~400V)	30								V/ns
dv/dt	Peak diode recovery dv/dt (note 3)	20								V/ns
P_D	Total power dissipation (@T_C=25°C)	33.8	143.7	134.4	178.6	168.9	158.2		96	W
	Total power dissipation (@T_a=25°C)							3.7		W
	Derating factor above 25°C	0.27	1.15	1.08	1.4	1.35	1.27	0.03	0.8	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature	-55 ~ + 150								°C
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.	300								°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value								Unit
		TO220F	TO251	TO252	TO220	TO262N	TO263	DFN5*6	QFN8*8	
R_{thjc}	Thermal resistance, Junction to case	3.7	0.87	0.93	0.7	0.74	0.79		1.3	°C/W
R_{thja}	Thermal resistance, Junction to ambient	50	79		54	64		34(Note)		°C/W

Note: R_{thja} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thjc} is guaranteed by design while R_{thca} is determined by the user's board design.

DFN5*6 R_{thja} : 34°C/W on a 1 in^2 pad of 2oz copper.

Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C		0.56		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V			1	uA
		V_{DS}=520V, T_C=125°C			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2		4	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D=6.5A		0.24	0.29	Ω
G_{fs}	Forward transconductance	V_{DS}=30V, I_D=6.5A		13		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=200V, f=1MHz		1092		pF
C_{oss}	Output capacitance			51		
C_{rss}	Reverse transfer capacitance			1.2		
$t_{d(on)}$	Turn on delay time	V_{DS}=325V, I_D=13A, R_G=25Ω, V_{GS}=10V (note 4,5)		17		ns
t_r	Rising time			34		
$t_{d(off)}$	Turn off delay time			97		
t_f	Fall time			40		
Q_g	Total gate charge	V_{DS}=520V, V_{GS}=10V, I_D=13A (note 4,5)		28		nC
Q_{gs}	Gate-source charge			5.5		
Q_{gd}	Gate-drain charge			10.5		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		3		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			13	A
I_{SM}	Pulsed source current				39	A
V_{SD}	Diode forward voltage drop.	I_S=13A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=13A, V_{GS}=0V, dI_F/dt=100A/us		299		ns
Q_{rr}	Reverse recovery charge			3.3		uC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L =32.7mH, I_{AS} =3.5A, V_{DD}=50V, R_G=25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 13A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

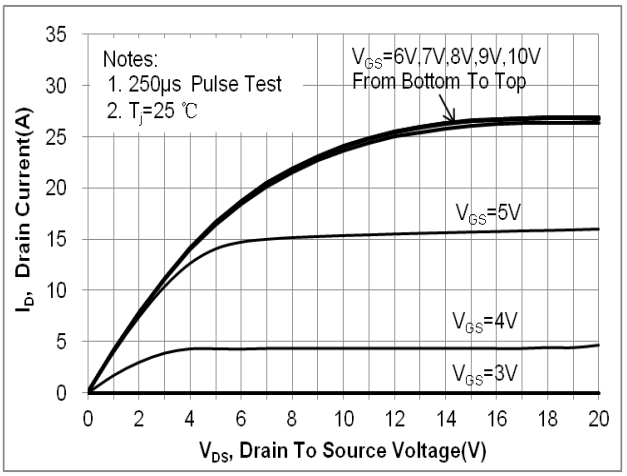


Fig. 2. Transfer characteristics

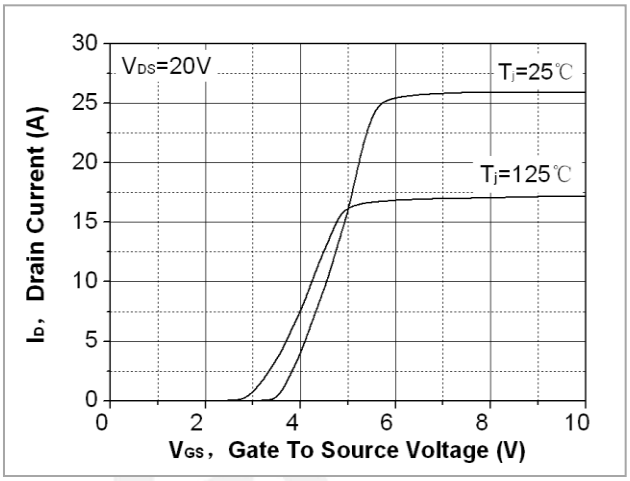


Fig. 3. On-resistance variation vs. drain current and gate voltage

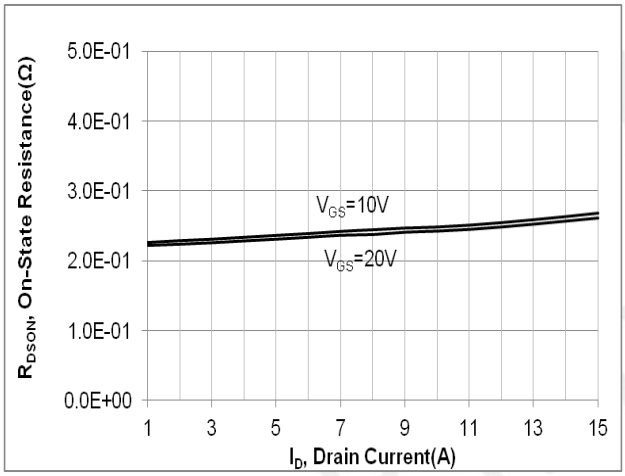


Fig. 4. On-state current vs. diode forward voltage

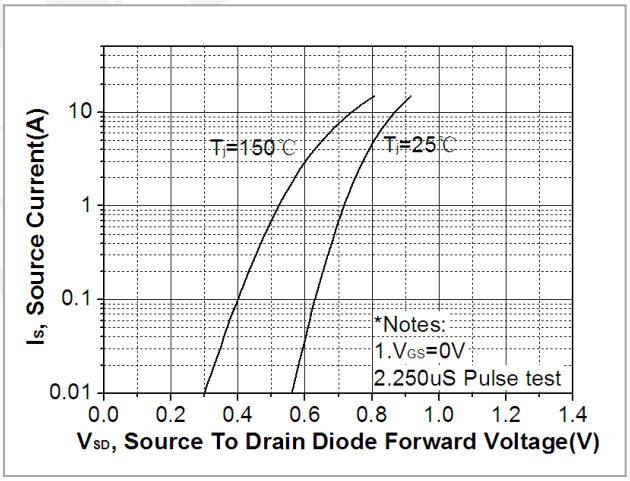


Fig 5. Breakdown voltage variation vs. junction temperature

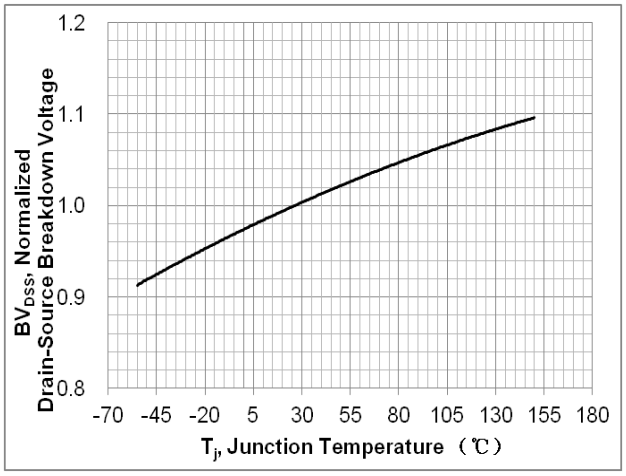


Fig. 6. On-resistance variation vs. junction temperature

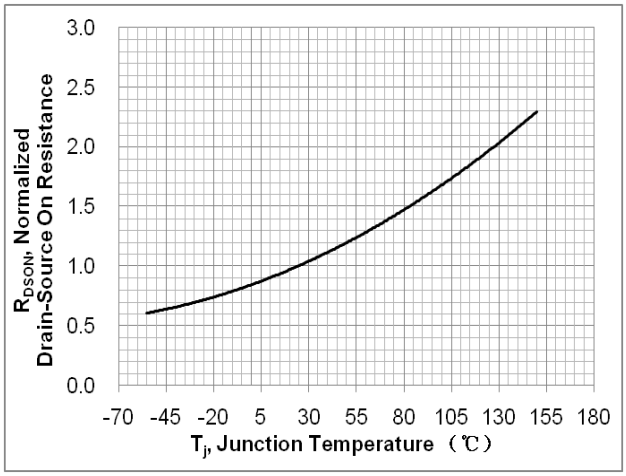


Fig. 7. Gate charge characteristics

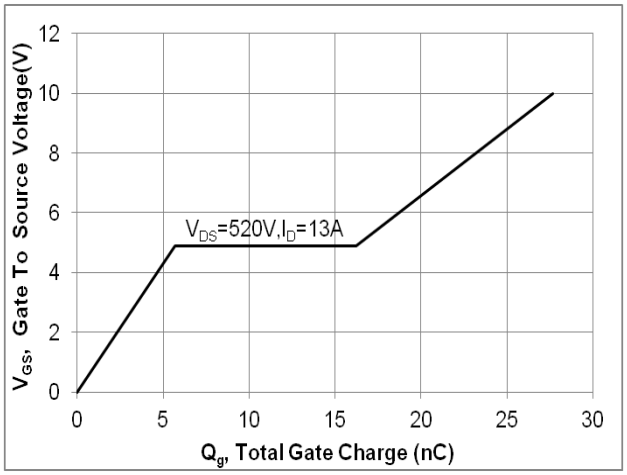


Fig. 8. Capacitance Characteristics

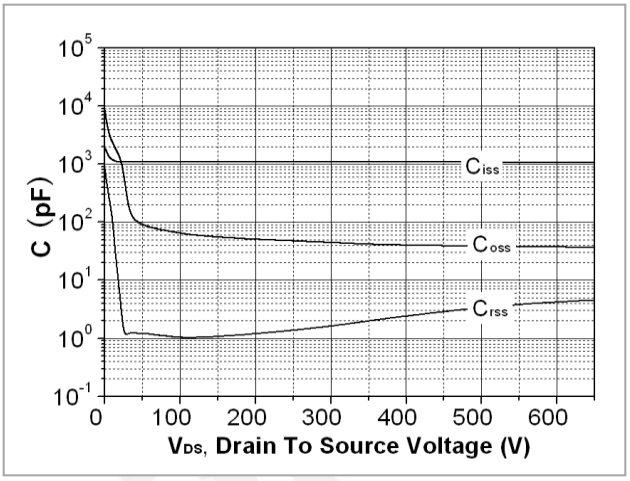


Fig. 9. Maximum safe operating area(TO-220F)

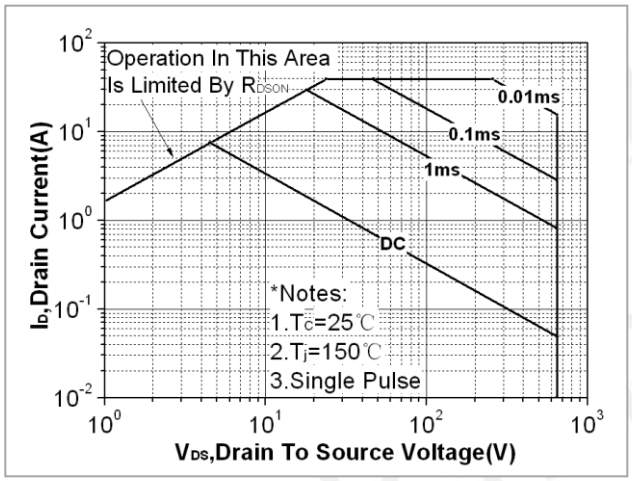


Fig.10. Maximum safe operating area(TO-251)

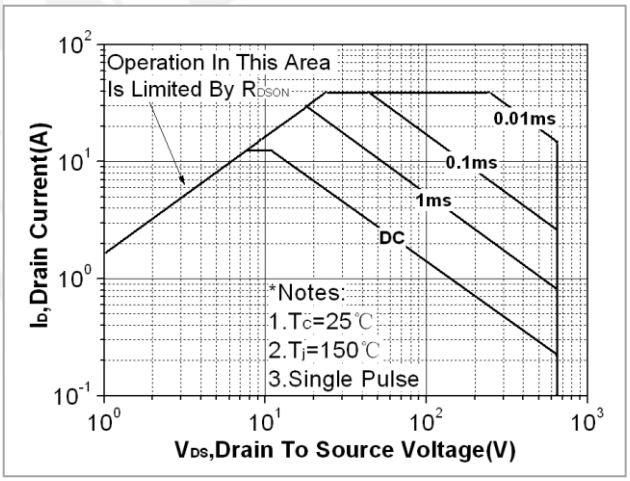


Fig. 11. Maximum safe operating area(TO-252)

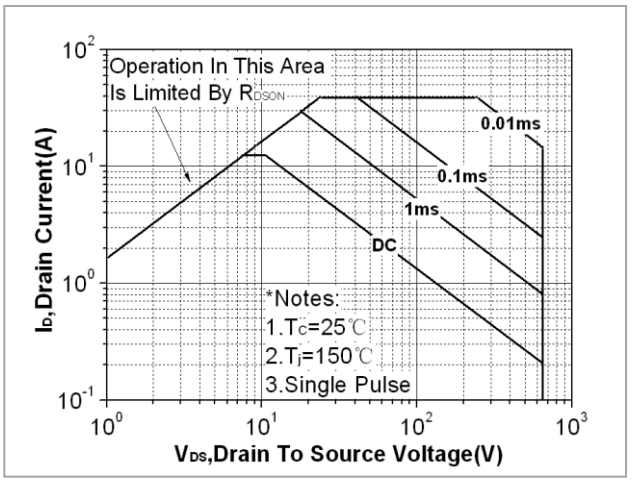


Fig. 12. Maximum safe operating area(TO-220)

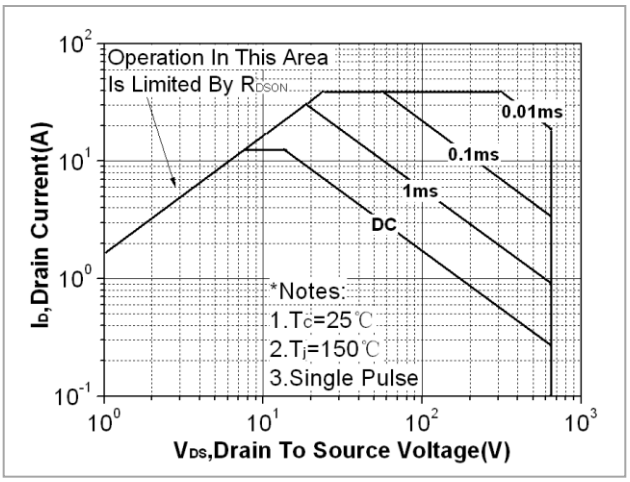


Fig. 13. Maximum safe operating area(TO-262N)

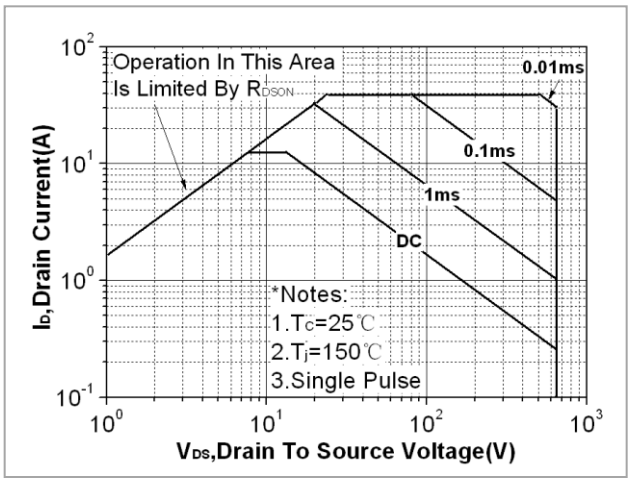


Fig.14. Maximum safe operating area(TO-263)

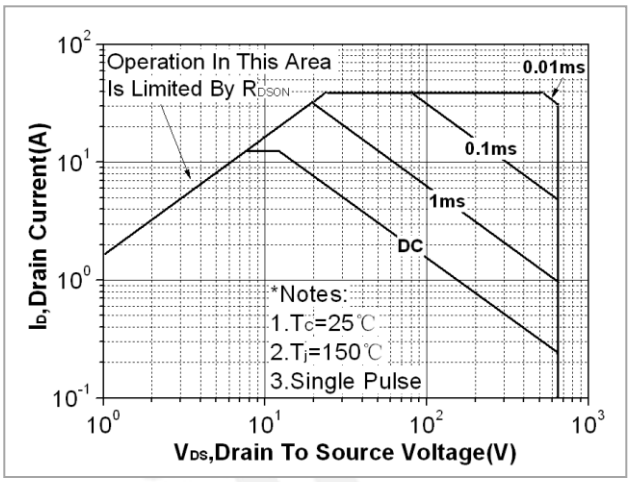


Fig. 15. Maximum safe operating area(DFN5*6)

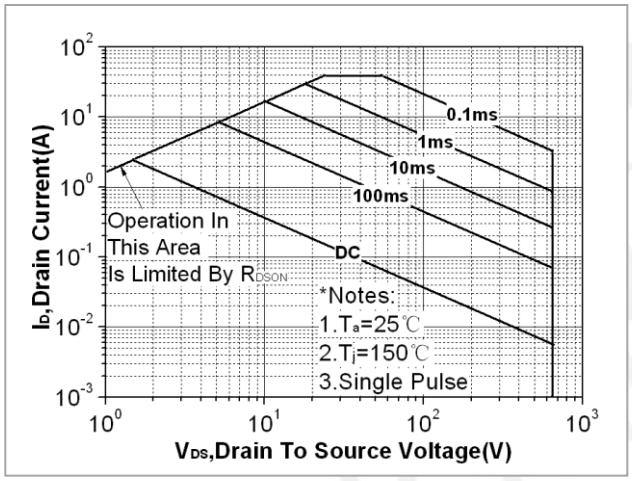


Fig. 16. Maximum safe operating area(QFN8*8)

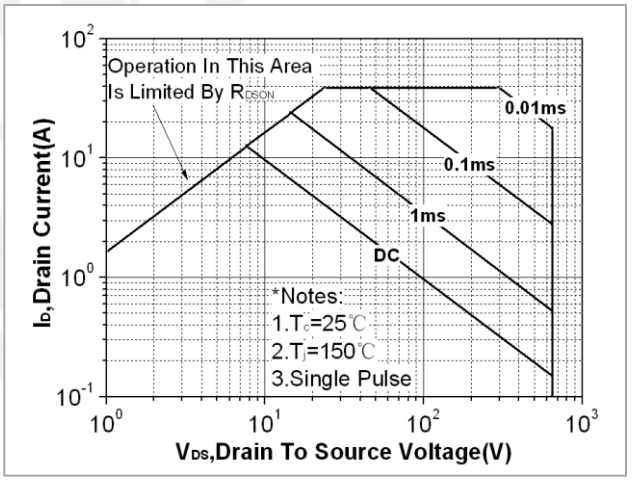


Fig. 17. Transient thermal response curve(TO-220F)

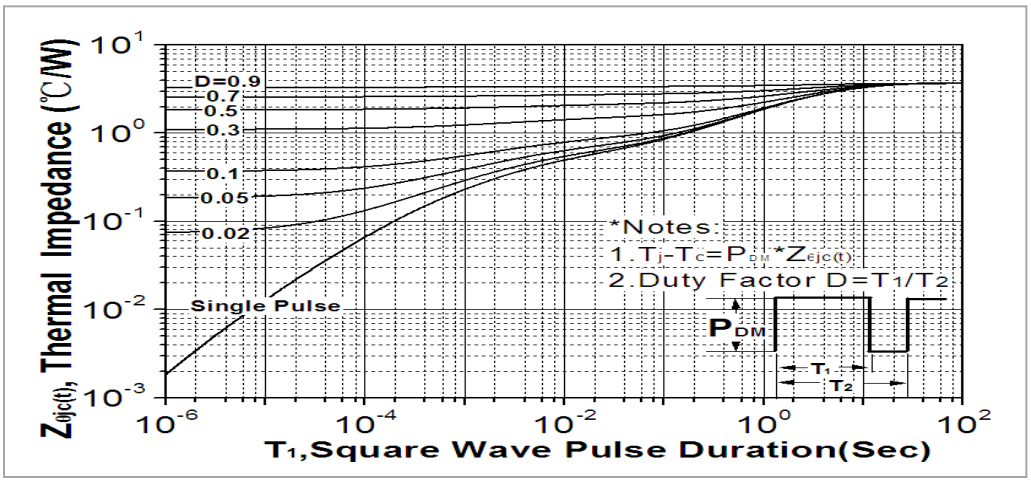


Fig. 18. Transient thermal response curve(TO-251)

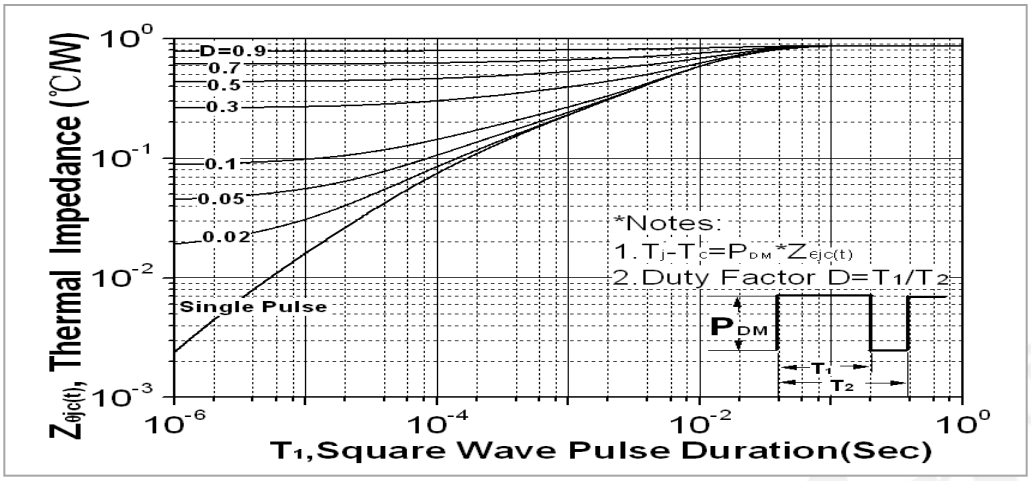


Fig. 19. Transient thermal response curve(TO-252)

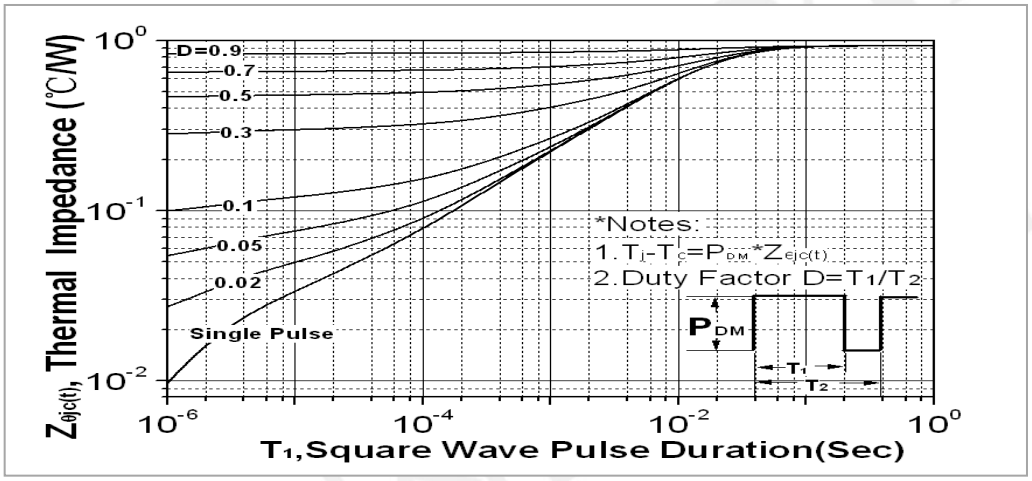


Fig. 20. Transient thermal response curve(TO-220)

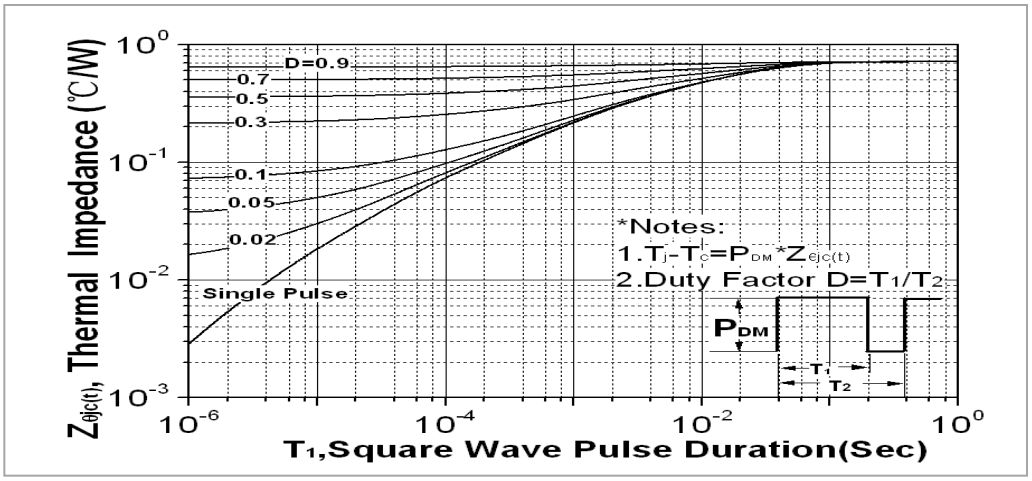


Fig. 21. Transient thermal response curve(TO-262N)

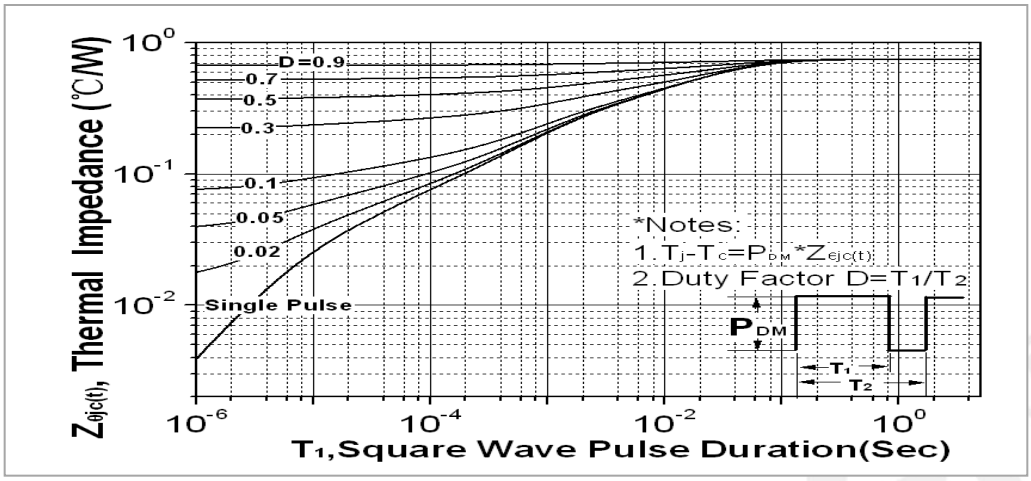


Fig. 22. Transient thermal response curve(TO-263)

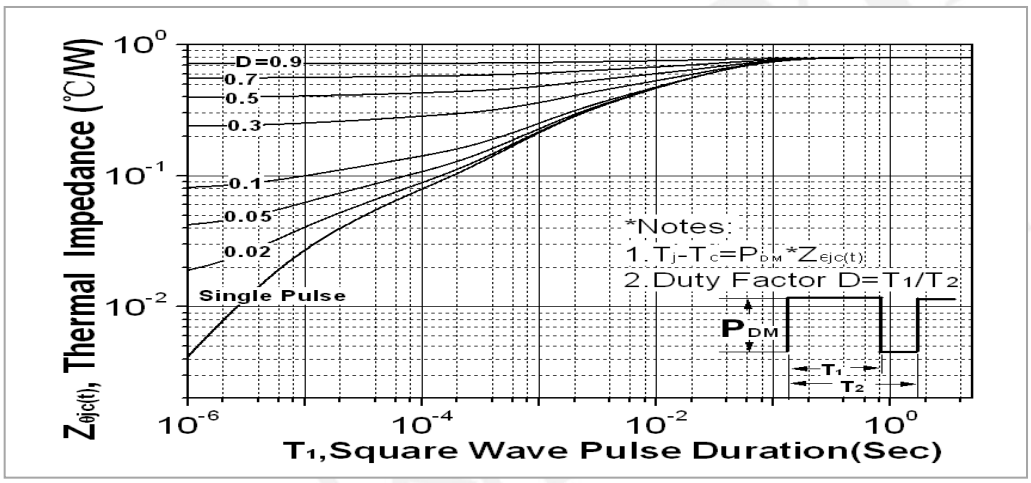


Fig. 23. Transient thermal response curve(DFN5*6)

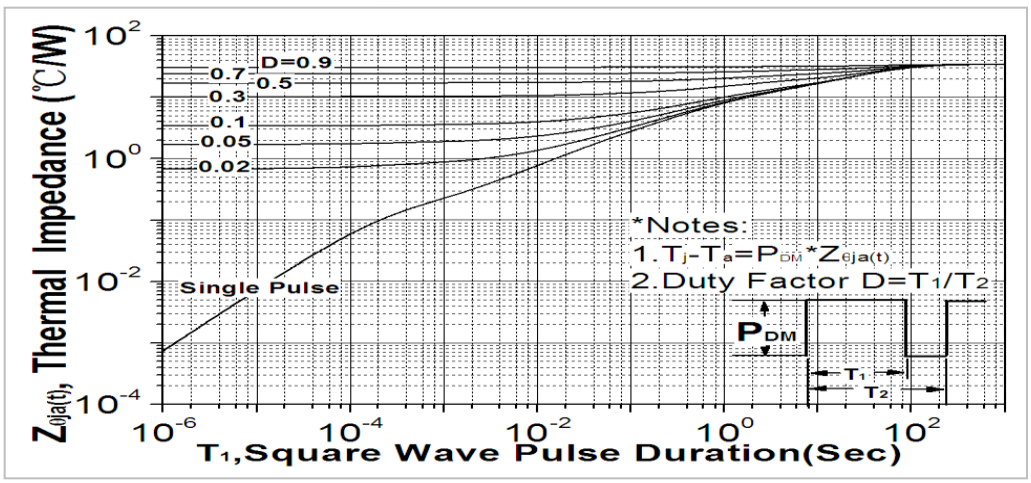


Fig. 24. Transient thermal response curve(QFN8*8)

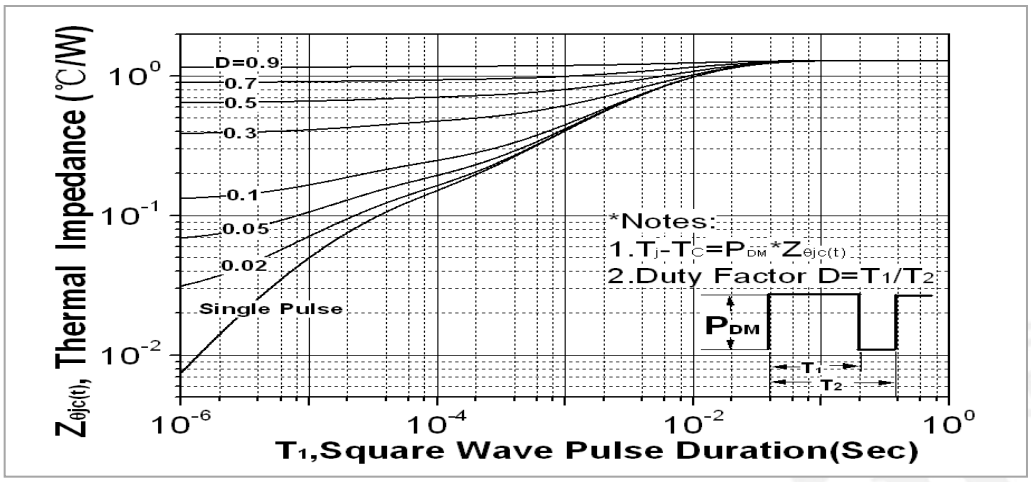


Fig. 25. Gate charge test circuit & waveform

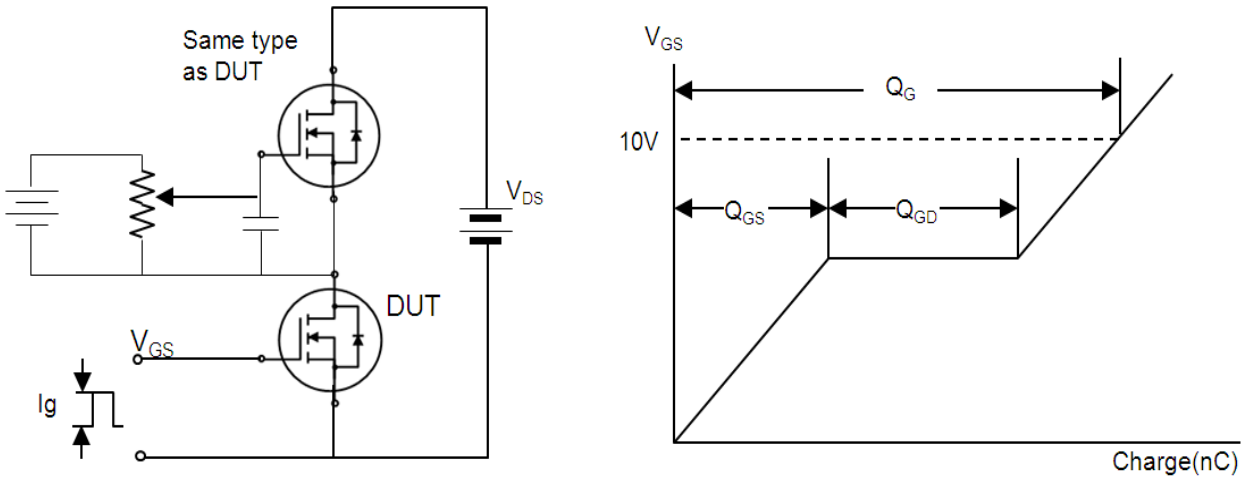


Fig. 26. Switching time test circuit & waveform

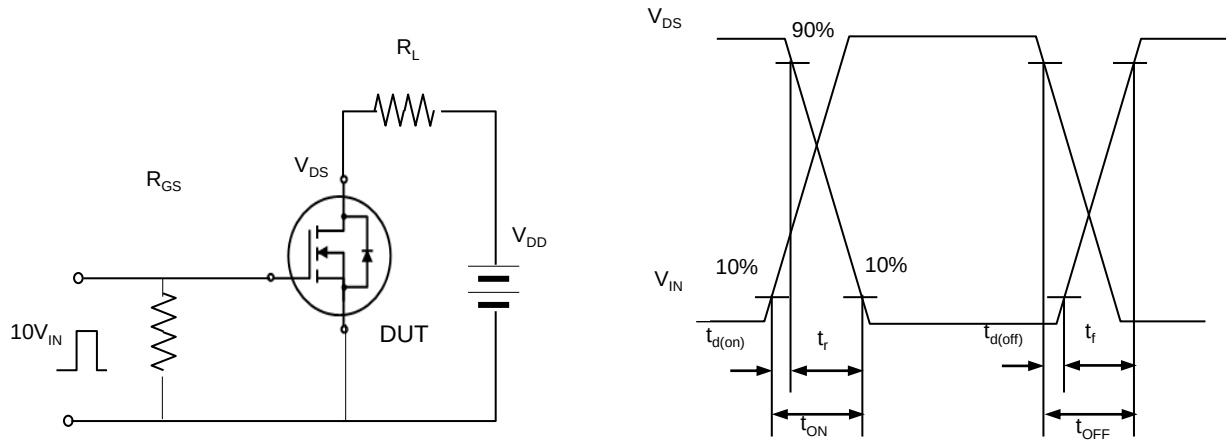


Fig. 27. Unclamped Inductive switching test circuit & waveform

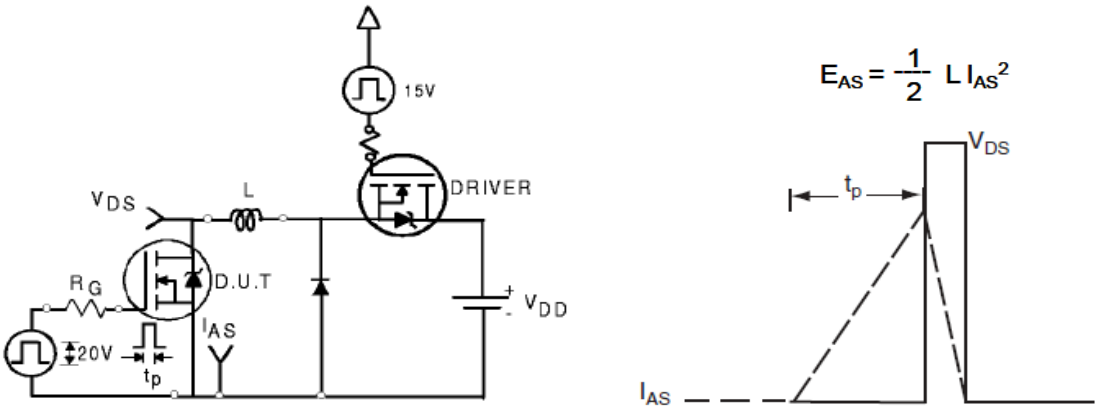
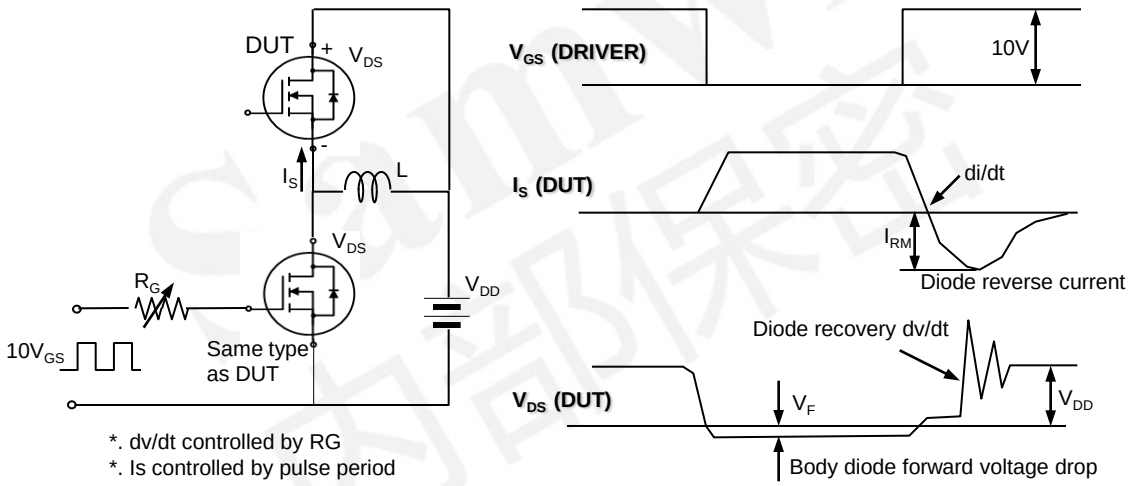


Fig. 28. Peak diode recovery dv/dt test circuit & waveform



DISCLAIMER

* All the data & curve in this document was tested in XI' AN SEMIPOWER TESTING & APPLICATION CENTER.
* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability test
* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**

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