ES8396

Low Power Stereo Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma stereo ADC and DAC
- Two independent I^2S/PCM master or slave serial data port
- Three pairs of analog input
- Four pairs of analog output
- 2x0.9W stereo or 1.8W mono class D speaker driver
- Ground centered headphone driver
- Mono ear speaker driver
- 256/384Fs, USB 12/24 MHz, fractional PLL for wide range of system clocks
- Sophisticated analog input and output routing, mixing and gain
- Support analog and digital microphone
- GPIO
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB dynamic range, 95 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Microphone bias

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB dynamic range, 95 dB signal to noise ratio, -85 dB THD+N
- Digital peak limiter (DPL)
- Pop and click noise suppression

DSP

- Flexible digital signal routing and mixing
- Asynchronous sample rate conversion
- Six programmable digital filters for PEQ and noise reduction
- Stereo enhancement
- Support u/A law

Low Power

- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

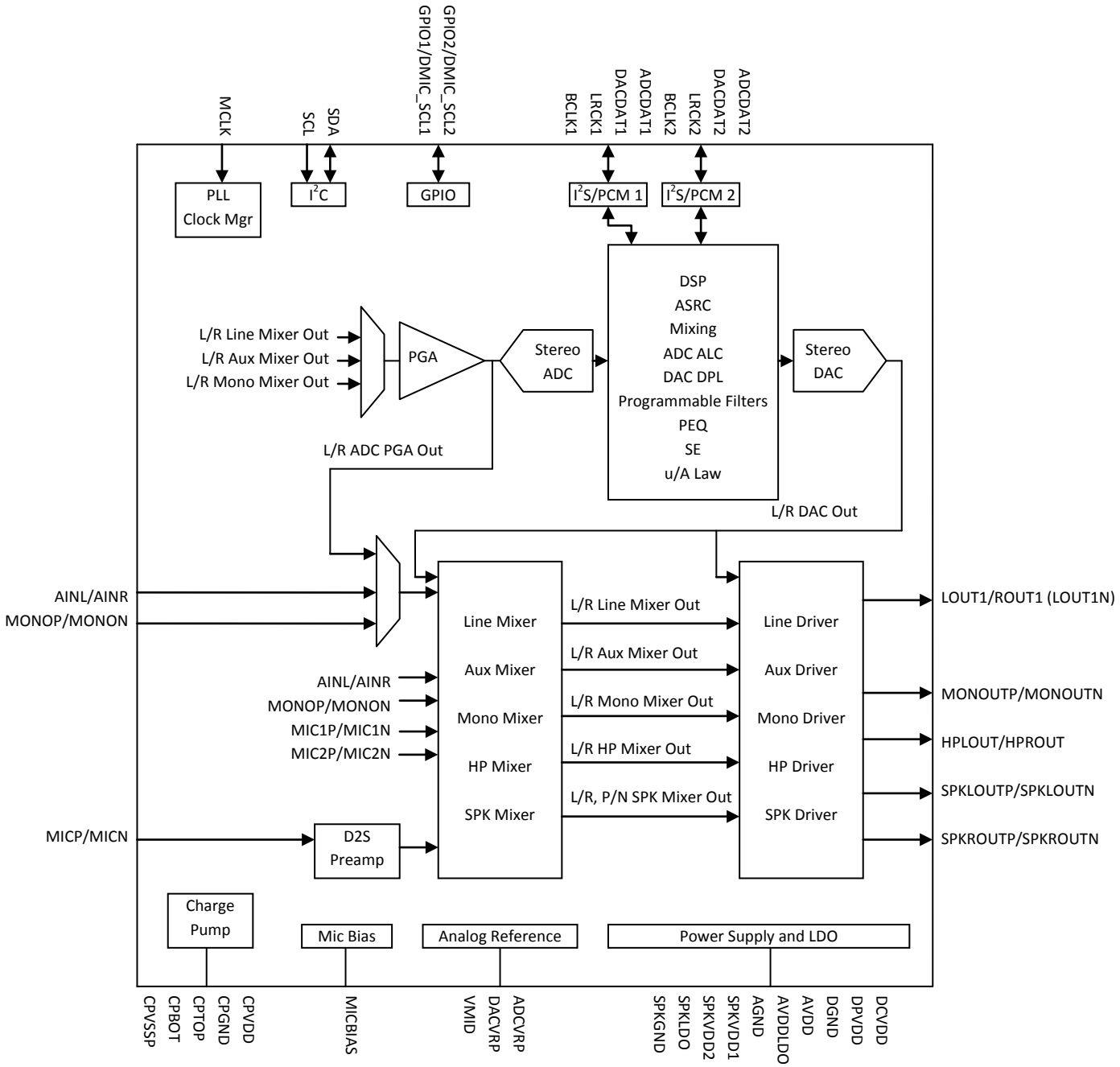
APPLICATIONS

- MID/Phoblet
- Smart Phone
- Digital amplifier

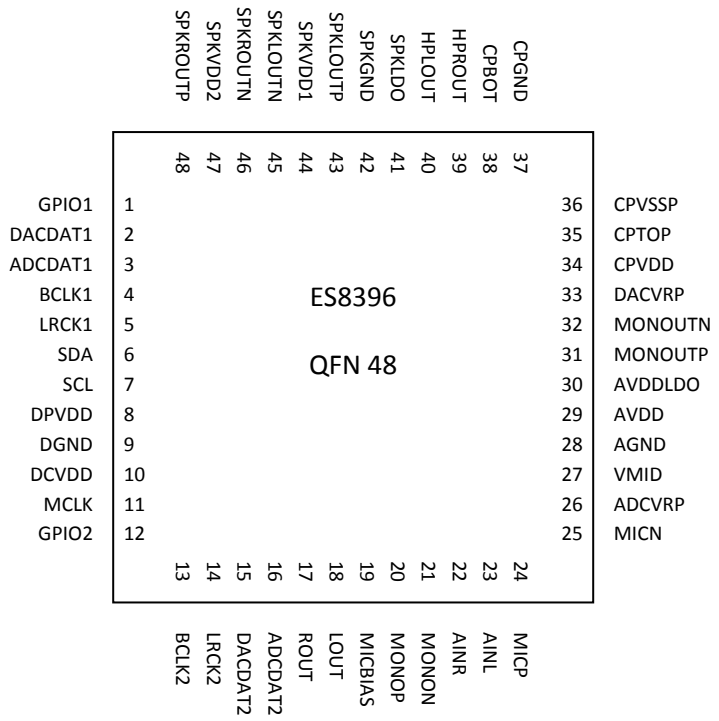
ORDERING INFORMATION

ES8396 -40°C ~ +85°C
QFN-48

1. BLOCK DIAGRAM



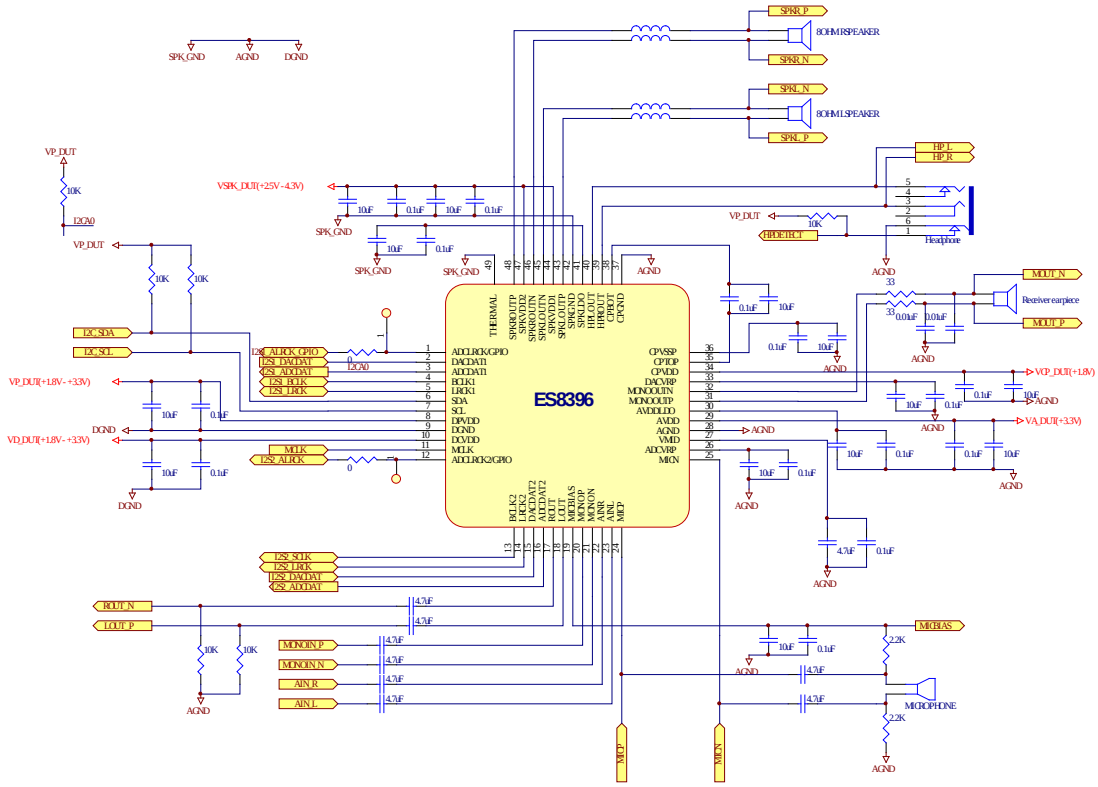
2. PIN OUT AND DESCRIPTION



Name	Type	Description
MCLK	DI	Master clock
SDA	DIO	I^2C data
SCL	DI	I^2C clock
GPIO1	DIO	GPIO (digital mic clock, ADC LRCK, etc)
GPIO2	DIO	GPIO (digital mic clock, ADC LRCK, etc)
ADCDAT1/AD0	DIO	I^2S/PCM serial data out; Also used as I^2C address
DACDAT1	DI	I^2S/PCM serial data in
LRCK1	DIO	I^2S/PCM left and right clock
BCLK1	DIO	I^2S/PCM bit clock
ADCDAT2	DIO	I^2S/PCM serial data out
DACDAT2	DI	I^2S/PCM serial data in
LRCK2	DIO	I^2S/PCM left and right clock
BCLK2	DIO	I^2S/PCM bit clock
AINL/JD1	AI	Left analog line input or jack detect 1
AINR/JD2	AI	Right analog line input or jack detect 2
MONOP	AI	Mono positive input or left analog line input
MONON	AI	Mono negative input or right analog line input
MICP	AI	Mic positive input or left analog line input
MICN/DMIC_SDA	AI	Mic negative input or right analog line input or digital mic data

LOUT	AO	Left line out
ROUT/LOUTN	AO	Right line out or negative left line out
MONOUTP	AO	Mono positive output
MONOUTN	AO	Mono negative output
HPLOUT	AO	Left headphone out
HPROUT	AO	Right headphone out
SPKLOUTP	AO	Positive left speaker out
SPKLOUTN	AO	Negative left speaker out
SPKROUTP	AO	Positive right speaker out
SPKROUTN	AO	Negative right speaker out
CPVDD		Charge pump power supply
CPGND		Charge pump ground
CPTOP		Charge pump capacitor top
CPBOT		Charge pump capacitor bottom
CPVSSP		Charge pump filtering
MICBIAS	AO	Mic bias
ADCVRP		ADC reference filtering
DACVRP		DAC reference filtering
VMID		Common mode filtering
DCVDD		Digital core power supply
DPVDD		Digital IO power supply
DGND		Digital ground
AVDD		Analog power supply
AVDDLDO		Analog LDO power supply
AGND		Analog ground
SPKVDD1		Speaker driver power supply
SPKVDD2		Speaker driver power supply
SPKLDO		Speaker driver LDO power supply
SPKGND		Speaker driver ground

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports three types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and an on-chip 22-bit fractional PLL clock.

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 100 kbps.

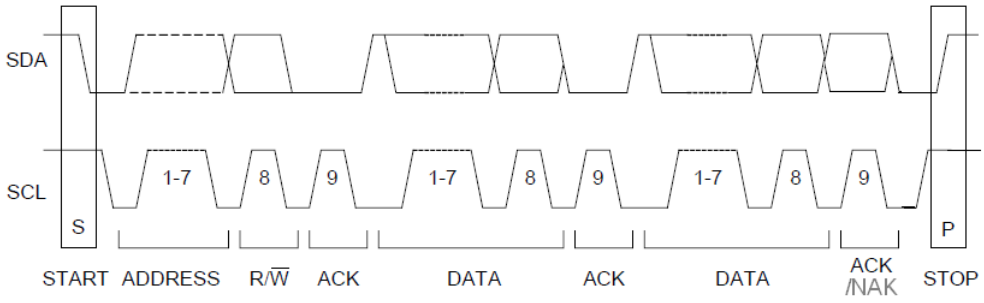


Figure 1 Data Transfer for I^2C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register. There are no acknowledge bit after data to be written or read, this is the only difference from the I²C protocol.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I²S, left justified, right justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

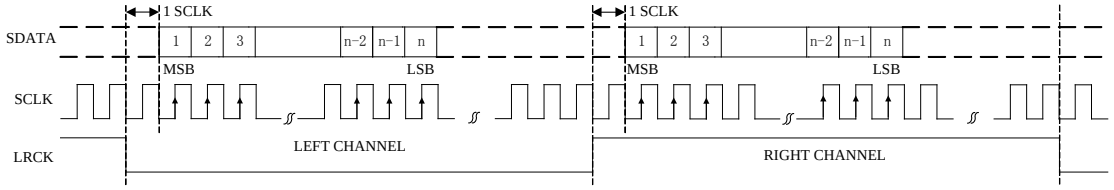


Figure 2 I²S Serial Audio Data Format Up To 24-bit

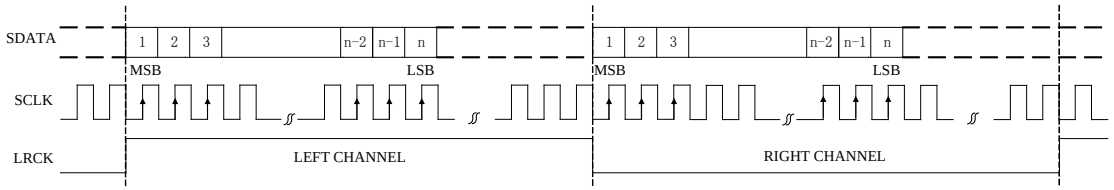


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

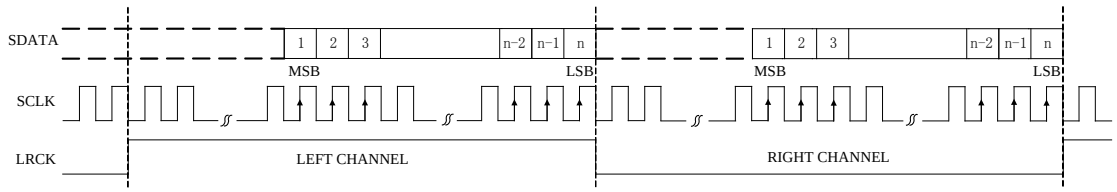


Figure 4 Right Justified Serial Audio Data Format Up To 24-bit

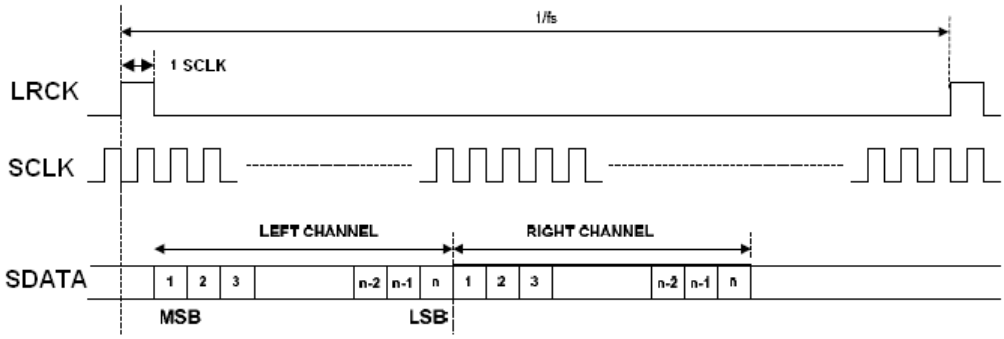


Figure 5 DSP/PCM Mode A

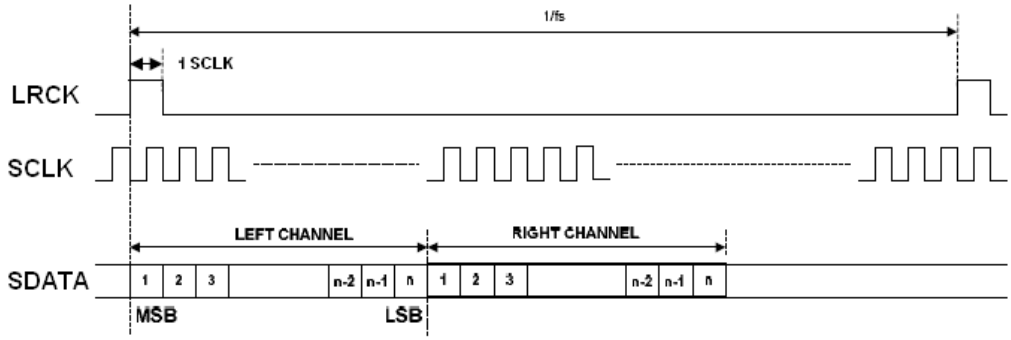


Figure 6 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+4.5V
Digital Supply Voltage Level	-0.3V	+5.0V
Input Voltage Range	DGND-0.3V	DVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage Level	2.0	3.3	3.6	V
Analog Supply Voltage Level – Class D	2.5	4.0	4.3	V
Digital Supply Voltage Level – DCVDD	1.6	3.3	3.6	V
Digital Supply Voltage Level – DPVDD (recommend to be the same as DCVDD)	1.6	3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	85	95	98	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		20		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	83	96	98	dB
THD+N	-85	-83	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	40			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz Fs = 44.1KHz Fs = 48KHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, AVDD=1.8V: Play back Play back and record DVDD=3.3V, AVDD=3.3V: Play back Play back and record		 7 16 31 59		mW
Power Down Mode				
DVDD=1.8V, AVDD=1.8V DVDD=3.3V, AVDD=3.3V		TBD TBD		mW

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz

LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

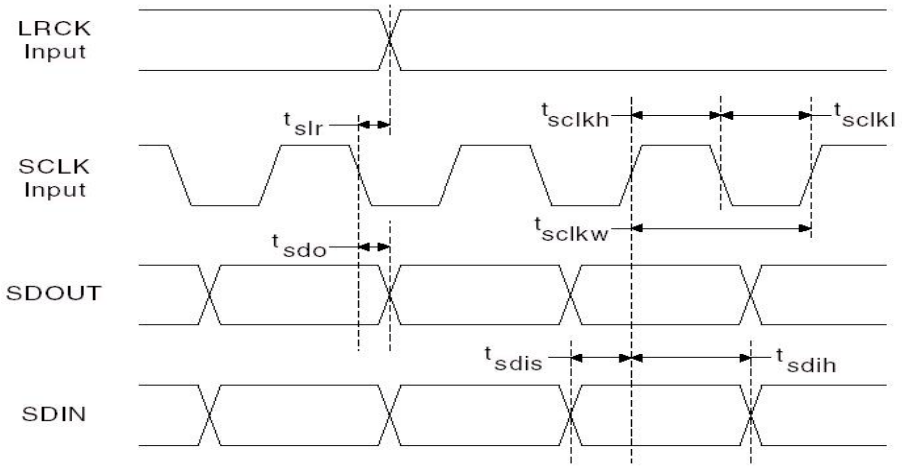


Figure 8 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
SCL Clock Frequency	FSCL		400	KHz
Bus Free Time Between Transmissions	TTWID	1.3		us
Start Condition Hold Time	TTWSTH	0.6		us
Clock Low time	TTWCL	1.3		us
Clock High Time	TTWCH	0.4		us
Setup Time for Repeated Start Condition	TTWSTS	0.6		us
SDA Hold Time from SCL Falling	TTWDH		900	ns
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		300	ns
Fall Time SCL	TTWF		300	ns

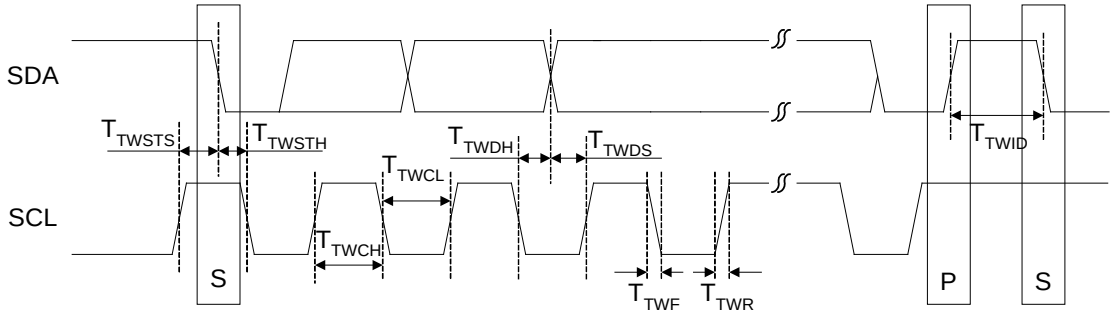
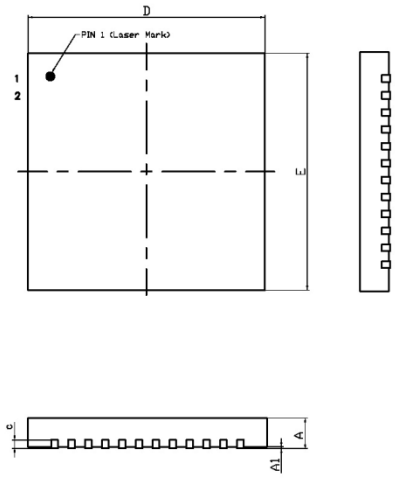
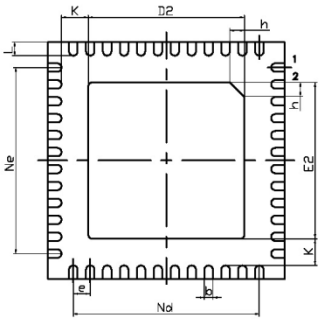


Figure 10 I^2C Timing

8. PACKAGE





SYMBOL	MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	—	0.05
b	0.15	0.25
c	0.18	0.23
D	5.90	6.10
D2	3.70	3.90
e	0.40BSC	
Ne	4.40BSC	
Nd	4.40BSC	
E	5.90	6.10
E2	3.70	3.90
K	0.20	—
L	0.35	0.45
h	0.30	0.40

QFN 48L(0606X0.75-0.40)(B)

9. CORPORATE INFORMATION

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