

N-Channel Enhancement Mode MOSFET

TDM3512

**DESCRIPTION**

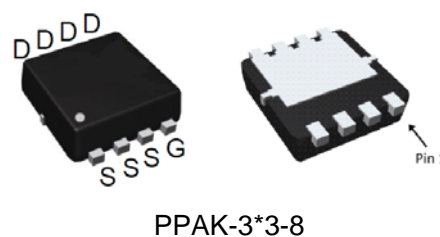
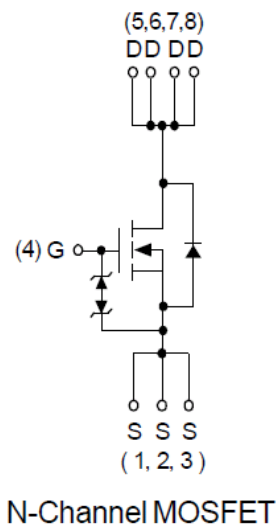
The TDM3512 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

**GENERAL FEATURES**

- RDS(ON) < 7mΩ @ VGS=1.8V  
RDS(ON) < 4.5mΩ @ VGS=2.5V  
RDS(ON) < 3.4mΩ @ VGS=4.5V
- High Power and current handling capability
- Surface Mount Package
- Lead Free and Green Devices available(RoHS Compliant)

**Application**

- PWM applications
- Load switch
- Power management
- Powered Systems



ABSOLUTE MAXIMUM RATINGS(TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Diode Continuous Forward Current	I <sub>S</sub> (T <sub>C</sub> =25°C)	25	A
Drain Current @ Continuous	I <sub>D</sub> (T <sub>C</sub> =25°C)	50	A
	I <sub>D</sub> (T <sub>C</sub> =100°C)	40	A
Drain Current @ Current-Pulsed (Note 1)	I <sub>DM</sub> (T <sub>C</sub> =25°C)	200	A
Maximum Power Dissipation	P <sub>D</sub> (T <sub>C</sub> =25°C)	35	W
	P <sub>D</sub> (T <sub>C</sub> =100°C)	14	W
Drain Current @ Continuous	I <sub>D</sub> (T <sub>A</sub> =25°C)	17.8	A
	I <sub>D</sub> (T <sub>A</sub> =70°C)	14.2	A
Maximum Power Dissipation	P <sub>D</sub> (T <sub>A</sub> =25°C)	1.6	W
	P <sub>D</sub> (T <sub>A</sub> =70°C)	1	W
Thermal Resistance,Junction-to-Case	R <sub>θJC</sub>	3.5	°C/W
Thermal Resistance,Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	78	°C/W
Maximum Operating Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 To 150	°C

**N-Channel Enhancement Mode MOSFET**
**TDM3512**
**ELECTRICAL CHARACTERISTICS** ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

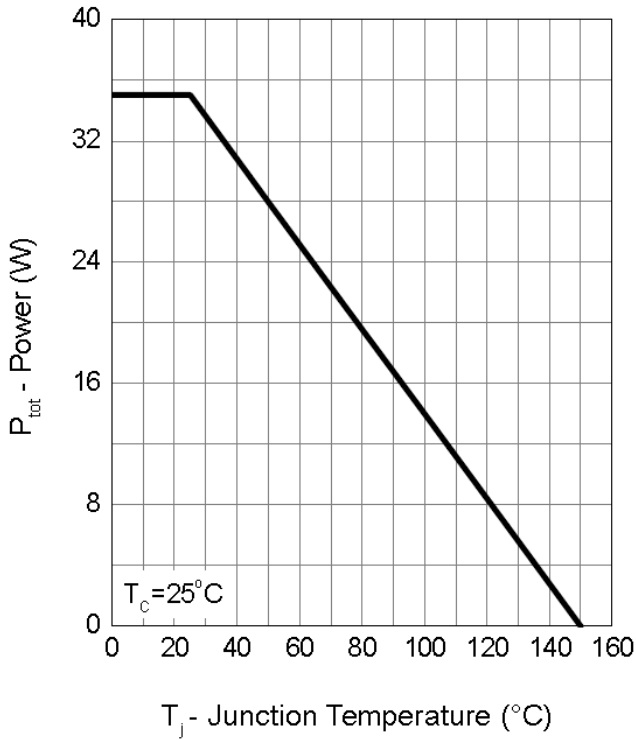
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=16V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=1.8V, I_D=2A$	-	4.6	7	m $\Omega$
		$V_{GS}=2.5V, I_D=10A$	-	3.3	4.5	m $\Omega$
		$V_{GS}=4.5V, I_D=13.5A$	-	2.7	3.4	m $\Omega$
<b>DYNAMIC CHARACTERISTICS</b> (Note3)						
Gate Resistance	$R_G$	$V_{DS}=0V, V_{GS}=0V, F=1.0\text{MHz}$	-	2	3.6	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V, F=1.0\text{MHz}$	-	3775	4910	PF
Output Capacitance	$C_{oss}$		-	730	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	525	-	PF
<b>SWITCHING CHARACTERISTICS</b> (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=10V, R_L=10\Omega, V_{GEN}=10V, R_G=6\Omega$ $I_D=1A$	-	14	26	nS
Turn-on Rise Time	$t_r$		-	14.5	27	nS
Turn-Off Delay Time	$t_{d(off)}$		-	130	234	nS
Turn-Off Fall Time	$t_f$		-	70	126	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=13.5A, V_{GS}=4.5V$	-	35	50	nC
Gate-Source Charge	$Q_{gs}$		-	4.7	-	nC
Gate-Drain Charge	$Q_{gd}$		-	11.5	-	nC
Body Diode Reverse Recovery Time	$T_{rr}$	$I_F=13.5A, di/dt=100A/\mu s$	-	18	-	nS
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	6.2	-	nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode Forward Voltage (Note 2)	$V_{SD}$	$V_{GS}=0V, I_S=2A$	-	0.7	1.1	V

**NOTES:**

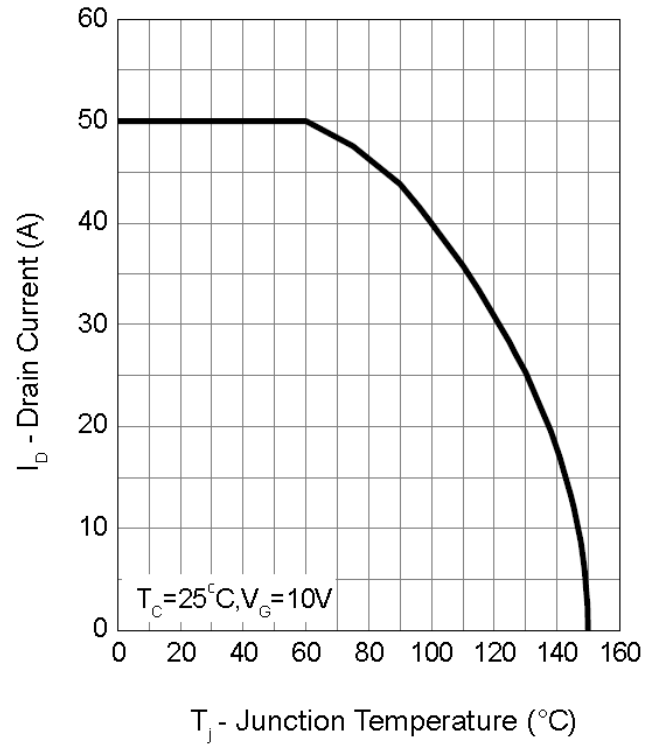
1. Pulse width limited by max. junction temperature.
2.  $R_{\theta JA}$  steady state=999s.  $R_{\theta JA}$  is measured with the device mounted on 1in2, Fr-4 board with 2oz.Copper
3. Guaranteed by design, not subject to production testing

Typical Operating Characteristics

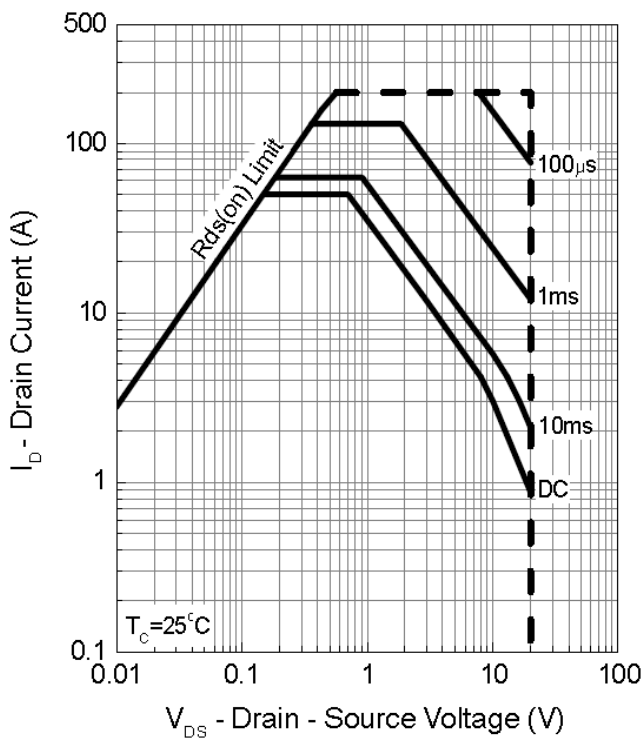
Power Dissipation



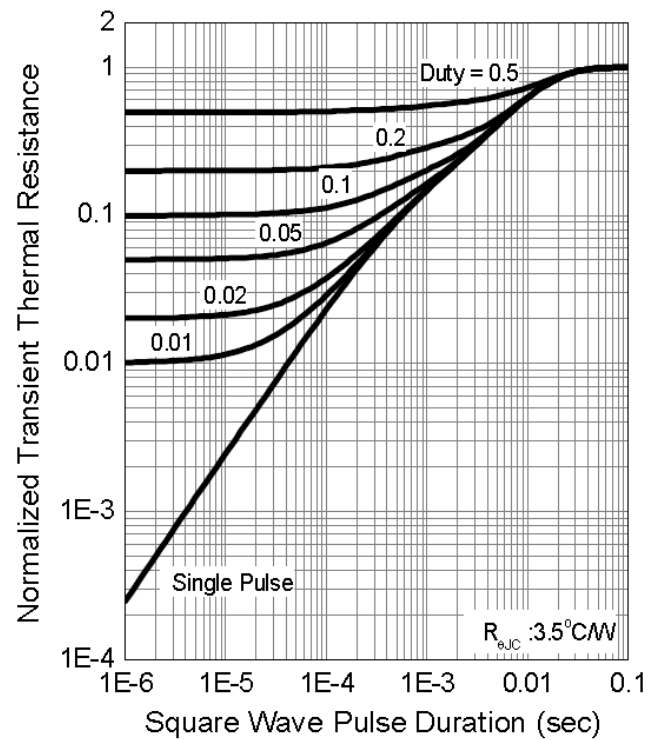
Drain Current



Safe Operation Area

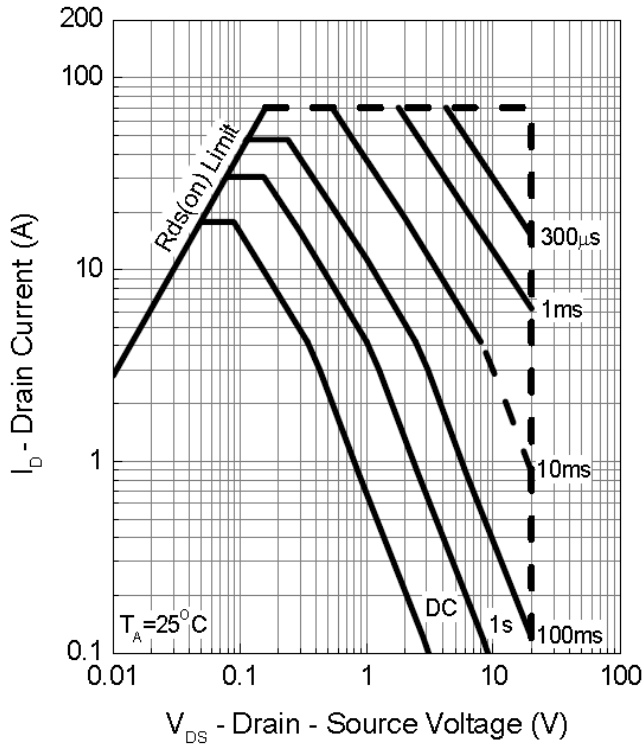


Thermal Transient Impedance

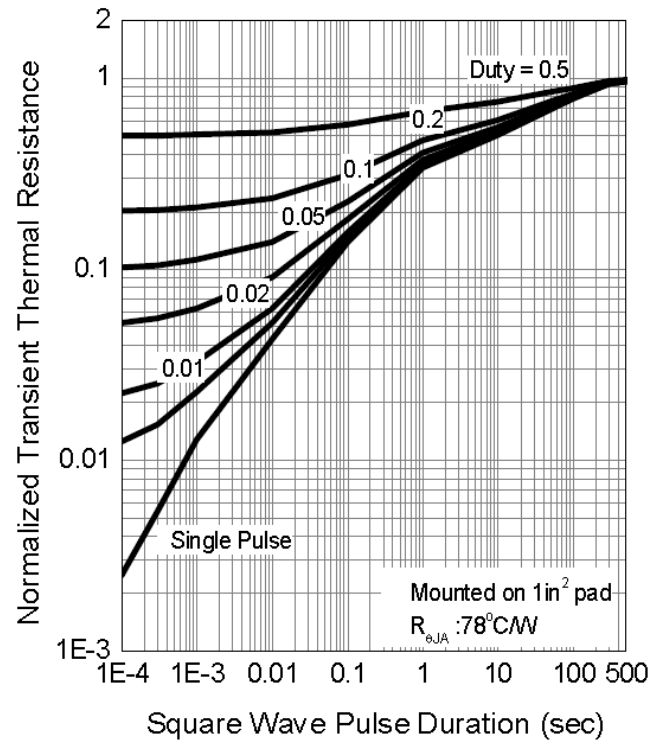


Typical Operating Characteristics(Cont.)

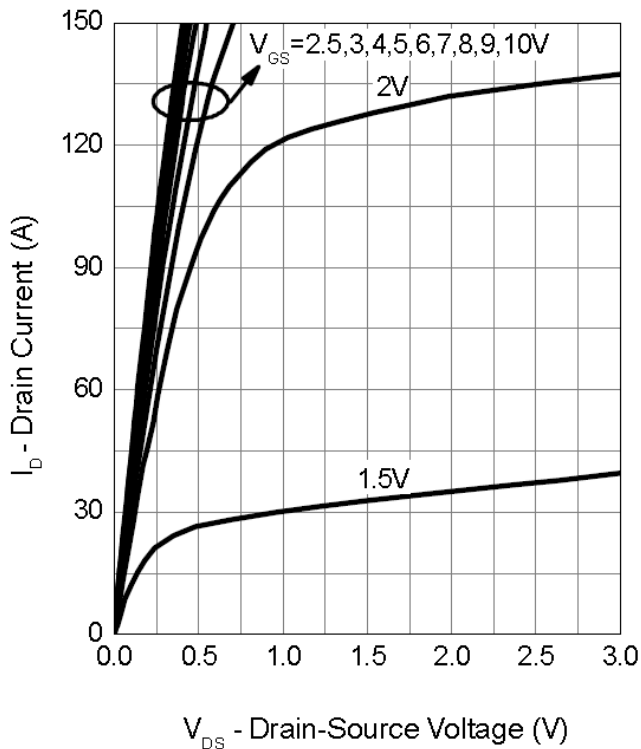
Safe Operation Area



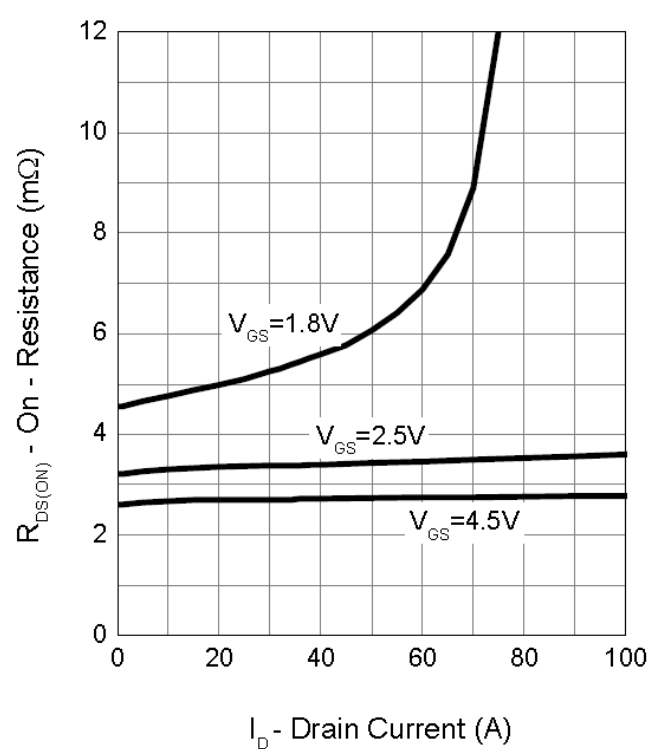
Thermal Transient Impedance



Output Characteristics

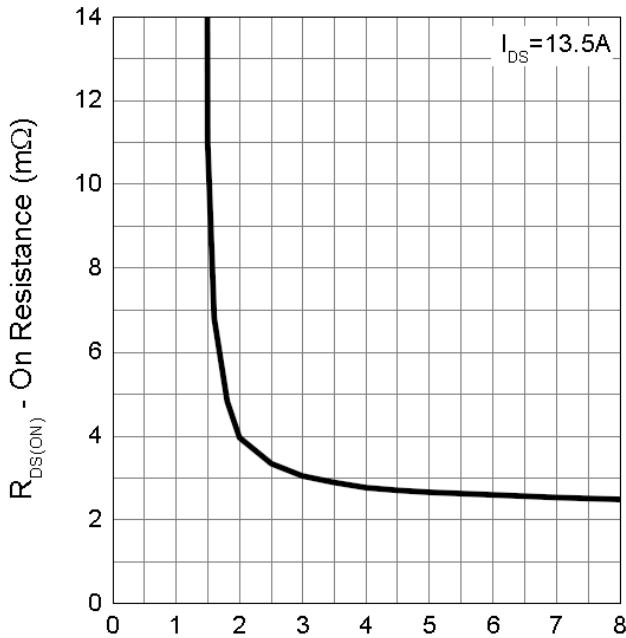


Drain-Source On Resistance



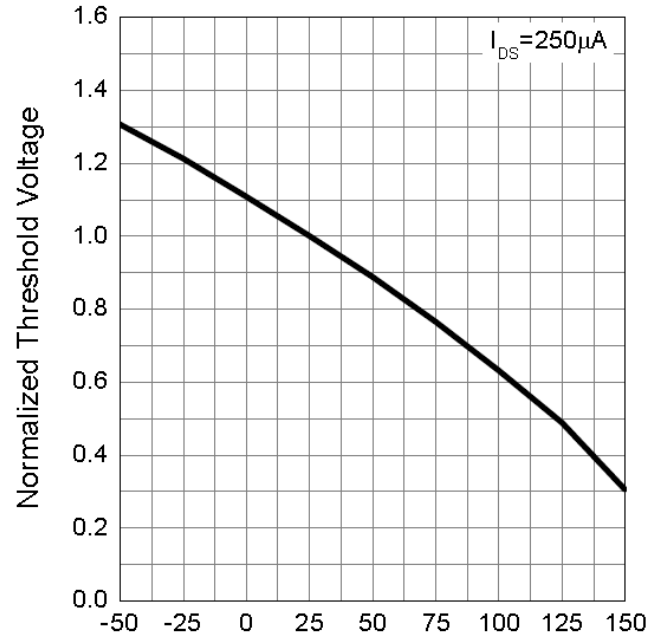
Typical Operating Characteristics (Cont.)

Gate-Source On Resistance

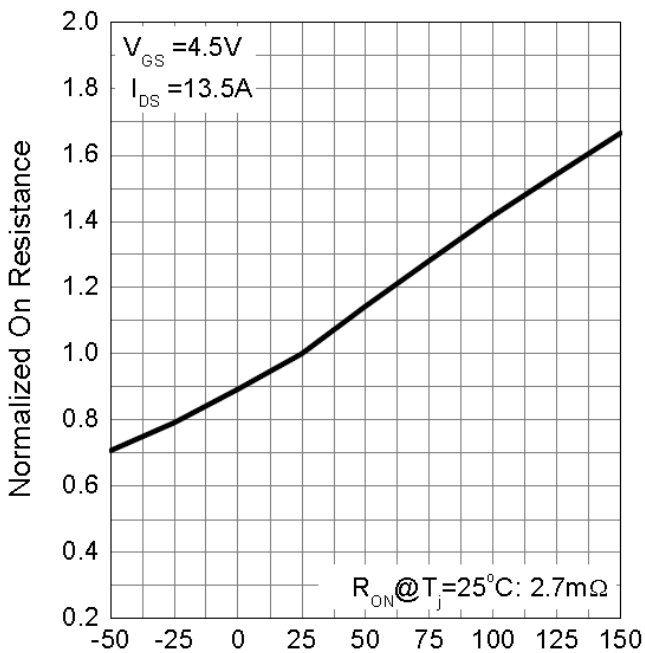


V<sub>GS</sub> - Gate - Source Voltage (V)  
Drain-Source On Resistance

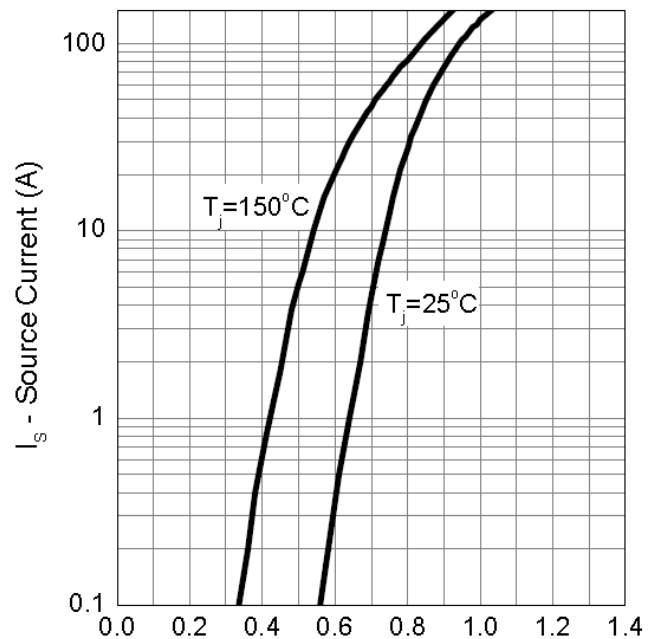
Gate Threshold Voltage



T<sub>J</sub> - Junction Temperature (°C)  
Source-Drain Diode Forward



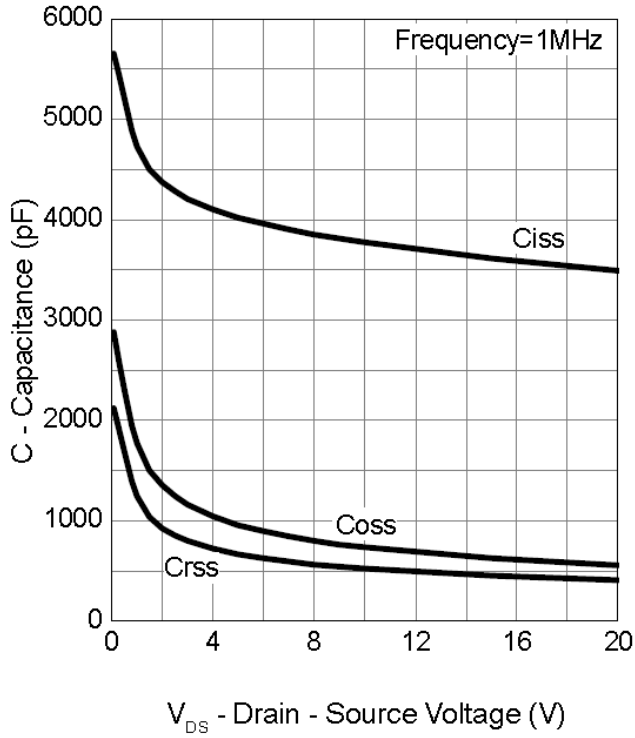
T<sub>J</sub> - Junction Temperature (°C)



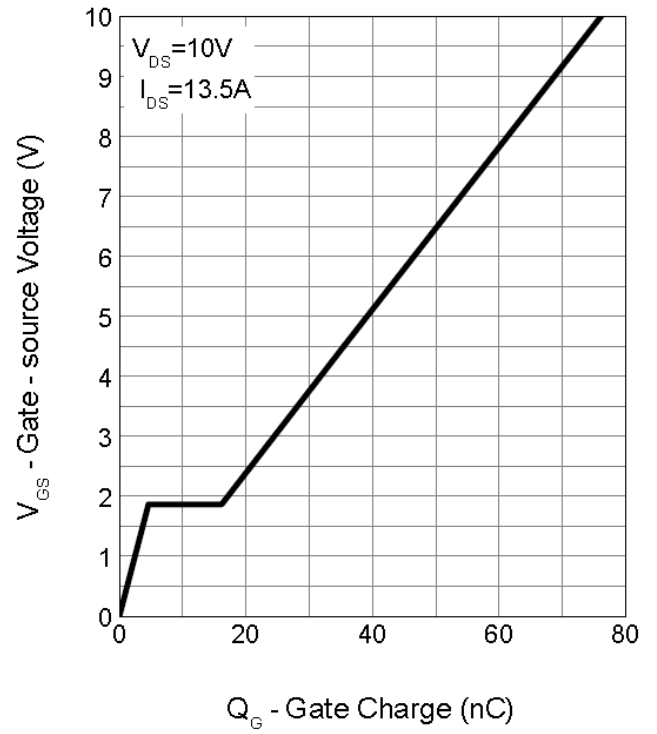
V<sub>SD</sub> - Source - Drain Voltage (V)

Typical Operating Characteristics (Cont.)

Capacitance

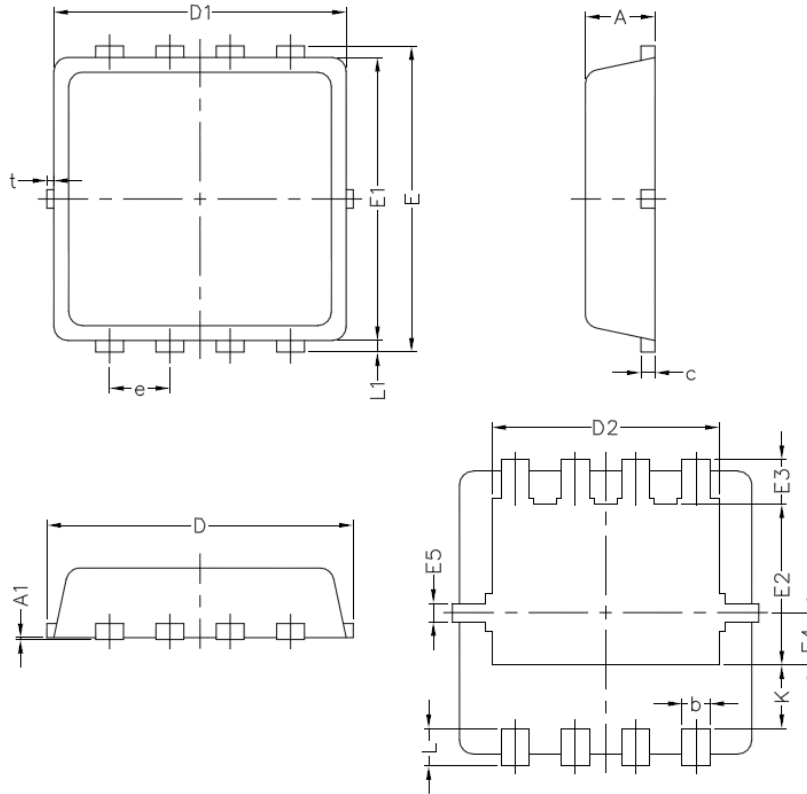


Gate Charge



Package Information

PPAK-3\*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes



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