



## PWM Dimming Control for LED Driver

### General Description

LP3351 is a cost effective LED driver optimized for LCD monitor and LCD TV backlighting application. It provides a high performance LED backlight solution with minimized bill of material count.

The LP3351 contains a PWM boost driver which uses current mode control and fixed frequency operation to regulate the LED current. The LED current is sensed through an external current sense resistor. The voltage across the sensing resistor is compared with reference level of 0.21V, the error amplified to control the pulse width of the power switch thus to regulate the current flowing the LED.

Otherwise, The LP3351 offers external frequency PWM dimming method for a wide range of dimming control.

Other features include over current protection (OCP), output over voltage protection (OVP), and under-voltage lockout (UVLO). The LP3351 is available in a space saving SOP-8 (0.5mm pitch) package.

### Order Information

LP3351 □□□  
 └─ F: Green  
 └─ Package Type  
 SO: SOP-8

### Features

- ◆ Wide  $V_{IN}$  Range: 8V to 28V
- ◆ Current-Mode PWM Controller
- ◆ External PWM Dimming Mode
- ◆ Under-Voltage Lockout
- ◆ Over Voltage Protection
- ◆ Over Current Protection
- ◆ Under-Voltage Protection
- ◆ Over-Temperature Protection
- ◆ Available in SOP-8
- ◆ RoHS Compliant and Halogen Free
- ◆ Pb-Free Package

### Applications

- ◆ TFT LCD TV
- ◆ TFT LCD Monitor
- ◆ Flat Panel Display

### Marking Information

Device	Marking	Package	Shipping
LP3351	LPS	SOP-8	3K/REEL
	LP3351		
	YWX		

Y: Y is year code. W: W is week code. X: X is series number.



### Typical Application Circuit

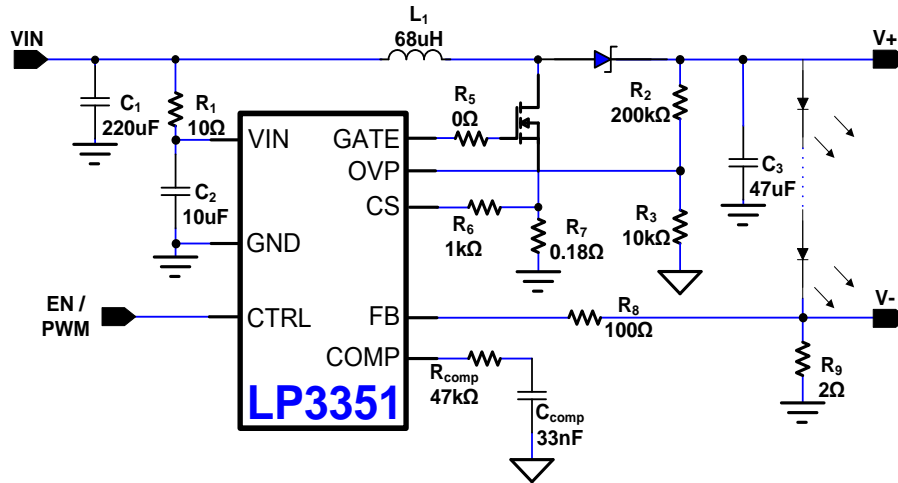


Figure 1. Typical Application Circuit of LP3351

### Pin Configuration

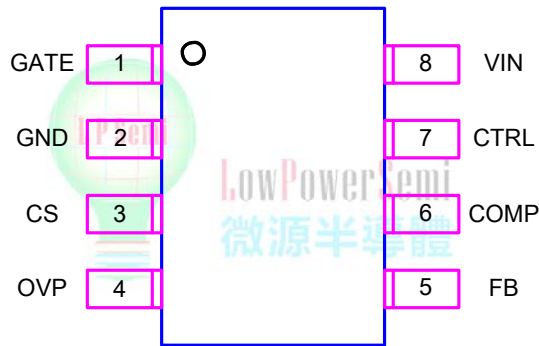


Figure 2. SOP-8 Package Top View



## Function Block Diagram

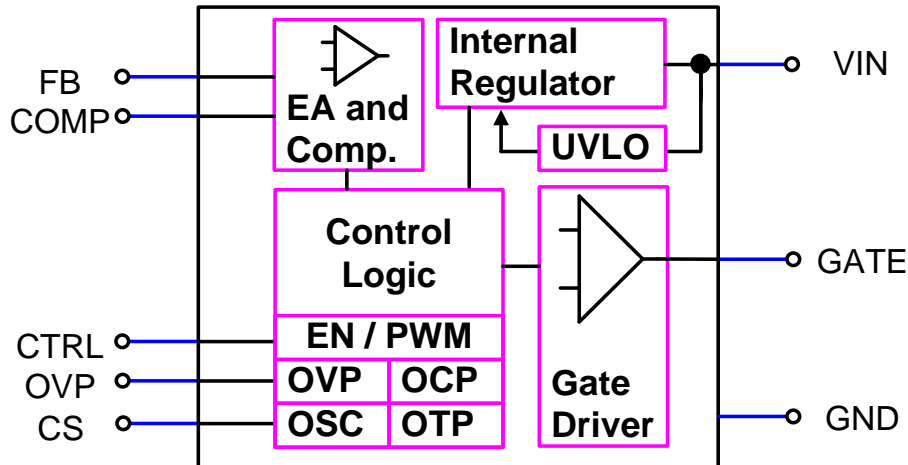


Figure 3. Function Block Diagram

## Functional Pin Description

Pin NO.	Pin Name	Description
1	GATE	External NMOS Gate Drive Pin.
2	GND	Ground.
3	CS	Current Sense Input Pin.
4	OVP	Over Voltage Protection Sense Input. Connect to an external resistive voltage divider from the V+ to GND.
5	FB	Regulator Feedback Input. Connect to an external resistive to set the output current.
6	COMP	Regulator Error Amplifier Compensation Pin.
7	CTRL	Enable and External PWM Dimming Control.
8	VIN	Input Supply Pin. Decouple with 10 $\mu$ F ceramic capacitor close to the pin.



## Absolute Maximum Ratings <sup>Note 1</sup>

◇ VIN to GND	-----	-0.3V to +36V
◇ GATE, CS, FB, COMP, OVP, CTRL to GND	-----	-0.3V to +20V
◇ Operating Junction Temperature Range (T <sub>J</sub> )	-----	-40°C to +150°C
◇ Operation Ambient Temperature Range	-----	-20°C to +85°C
◇ Storage Temperature Range	-----	-65°C to +150°C
◇ Maximum Soldering Temperature (at leads, 10sec)	-----	+260°C
◇ Maximum Junction Temperature	-----	+150°C

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Information

◇ Thermal Resistance		
SOP-8, $\theta_{JA}$	-----	112°C/W
SOP-8, $\theta_{JC}$	-----	39°C/W





## Electrical Characteristics

( $V_{IN}=12V$ ,  $V_{CTRL}=5V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>General</b>						
Input Supply Voltage	$V_{VLI}$		8		28	V
$V_{IN}$ Supply Current	$I_q$	Sleep Current		310	400	$\mu A$
		Operation Current		2.5	3	mA
Input UVLO Threshold	$V_{UVLO(VTH)}$	$V_{IN}$ Rising	6	7	8	V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$	Falling Hysteresis		500		mV
Thermal Shutdown Threshold	$T_{SD}$	Temperature Rising	140	160	180	$^{\circ}C$
Thermal Shutdown Hysteresis	$\Delta T_{SD}$			20		$^{\circ}C$
<b>PWM</b>						
Internal Oscillator Frequency	$F_{OSC}$		175	200	225	kHz
PWM Threshold Voltage	$V_{IH}$	Logic High.			2.6	V
	$V_{IL}$	Logic Low	1			
Pull Down Resistor	$R_{PULL\_Low}$			150		k $\Omega$
<b>Error Amplifier</b>						
Reference Voltage	$V_{REF}$	Reference voltage at non-inverting input.	-1.5%	0.21	+1.5%	V
Open Loop Voltage Gain	$A_m$			70		dB
Transconductance of EA	$G_m$		80	100	120	$\mu A/V$
Output Source Current	$I_{Source}$		24	30	36	$\mu A$
Output Sink Current	$I_{Sink}$		48	60	72	$\mu A$
<b>Protection Threshold</b>						
Over Voltage Protection	$V_{OVP}$	Threshold of OVP	1.8	2	2.2	V
Over Current Protection	$V_{OCP}$	Threshold of OCP (duty=90%)		330		mV
Fault Trigger Duration				50		ms
Connect detect time	$T_{det}$			1		ms
SCP Threshold	$V_{OVP\_UV}$	Normal Operation		0.2		V
		System Startup		100		mV



## Application Information

The LP3351 is designed in a current mode, constant frequency PWM boost converter. It can use dimming input that can be by external control signal with a duty ratio of 1%-100% in 100Hz to 1kHz. LP3351 offers protection features to protect the system such as output over voltage protection, boost diode disconnection protection, output short circuit protection and over temperature protection.

### Under Voltage Lockout (UVLO)

The LP3351 had an UVLO internal circuit that enable the device once the voltage on the VIN voltage exceeds the UVLO threshold voltage.

### Boost Controller

The LP3351 uses 200kHz fixed-frequency, current mode architecture to fixed the output current. The output voltage and soft start time can be adjustable by internal register.

### Boost Loop Compensation

The feedback loop can be compensated with an external compensation network consisted of R<sub>comp</sub>, C<sub>comp</sub>(As Figure 1). Choosing R<sub>comp</sub> to set high frequency integrator gain for fast transient response and C<sub>comp</sub> to set the integrator zero to maintain loop stability.

### Over Voltage Protection

The LP3351 converter has an over voltage protection by OVP pin. When the LEDs fail open circuit or LEDs are disconnected from the circuit, the over voltage function will monitor the output voltage through OVP pin to protect the converter. When LP3351 occur OVP, it will latch off until VIN is re-startup or CTRL input is recycled.

### LED Current Setting

The LED current is specified by current sense resistor between the FB pin to ground. In order to have accurate LED current, precision resistors are preferred. The LED current can be programmed by:

$$I_{LED} = 0.21/R_{FB}$$

### Dimming Control

The LED brightness is controlled by the PWM signal at CTRL pin which has different duty cycle. LP3351 can accept an external PWM signal to CTRL pin in the range of 100Hz to 1 kHz.

### Over Temperature Protection

The LP3351 device enters over temperature protection(OTP) if its junction temperature exceeds 160°C (Typ.). During over temperature protection none of the device's functions are available. To resume normal operation the junction temperature need cool down, and the outputs will restart.

### Current Sense and Over Current Protection (OCP)

The over current protection level can be set by R7(As Figure 1) and senses inductor current to compare with current limit value. When the inductor current exceeds the current limit, the switching will turns off immediately. It prevents large current damaging the external component. The OCP level is calculated as:

$$I_{OCP} = 0.33/R_7$$

The LP3351 uses a current mode control structure. The CS pin not only has current sense function but also build-in a slope compensation to avoid sub-harmonic oscillation. Additional slope compensation lessened the influence of the sensed current in the control loop.

### Layout Guideline

The proper PCB layout and component placement are critical for all circuit. The careful attention should be prevent electromagnetic interference (EMI) problems. Here are some suggestions to the layout of LP3351 design.

1. Connected all ground together with one uninterrupted ground plane with at least two vias .
2. The input capacitor should be located as closed as possible to the VIN and ground plane.
3. Minimize the distance of all traces connected to the LX node, that the traces short and wide route to obtain optimum efficiency.
4. All output capacitor must be closed to ground plane. The ground terminal of C<sub>OUT</sub> must be located as closed as possible to ground plane.
5. Radiated noise can be decreased by choosing a shielded inductor.

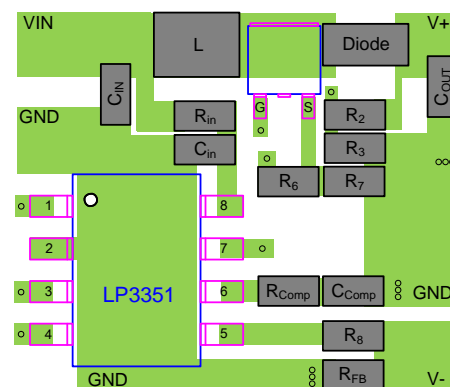
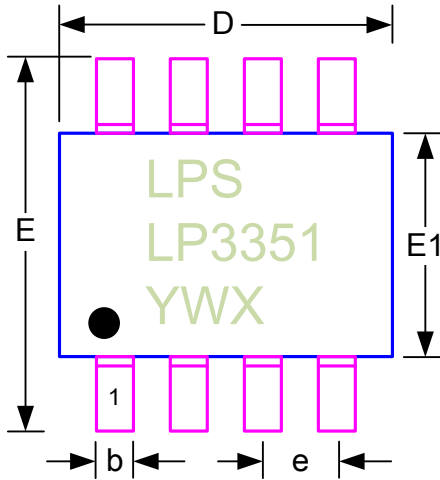


Figure 4. Recommended PCB Layout Diagram

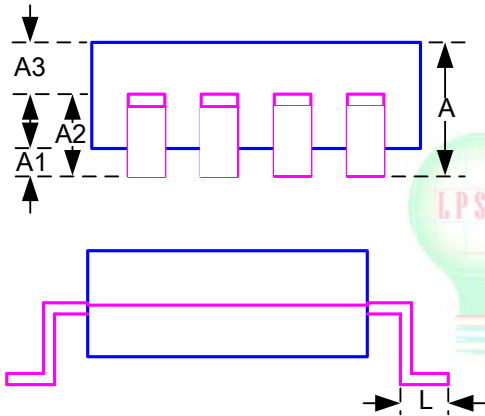


### Outline Information

SOP-8 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.750
A1	0.100	--	0.225
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.390	--	0.470
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.27BSC		
L	0.500	--	0.800



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