Dual Bootstrapped, 12V MOSFET Driver with Output Enable

General Description

The LP1110 is a single phase 12V MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive non-overlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate VBST voltages as high as 35V, with transient voltages as high as 40V. Both gate outputs can be driven low by applying a low logic level to the enable (EN) pin. An under voltage lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with over-temperature protection.

Order Information

LP1110 □ □ □

- F: Halogen Free & Pb Free
- Package Type QV:DFN-8

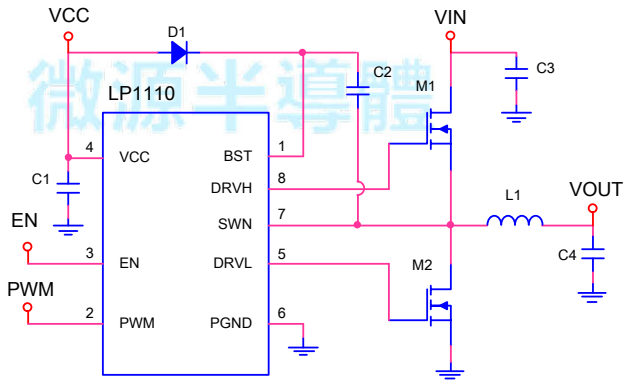
Features

- All-In-One Synchronous Buck Driver
- Bootstrapped High-Side Drive
- One PWM Signal Generates Both Drives
- Anti-cross Conduction Protection Circuitry

Applications

- Multiphase Desktop CPU Supplies
- Single-Supply Synchronous Buck Converters

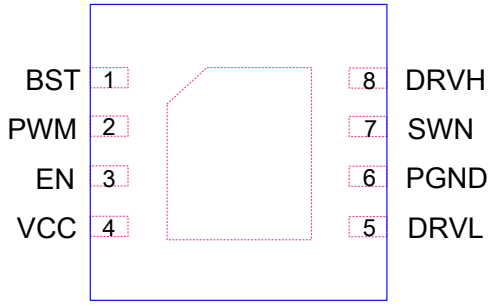
Typical Application Circuit



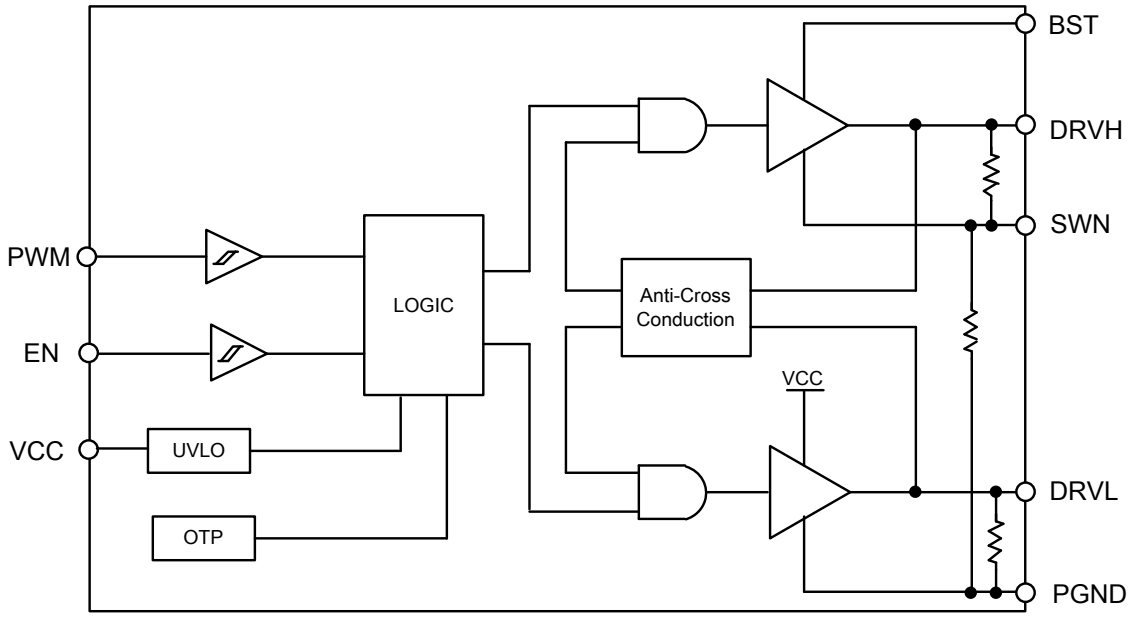
Marking Information

Device	Marking	Package	Shipping
LP1110	LPS LP1110 YWX	DFN8	5K/REEL
Y:Production year W:Production period X:Production batch			

Functional Pin Description

Package Type		Pin Configurations
DFN8		 (TOP View)
Pin	**Name**	**Description**
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and SW pins holds this bootstrap voltage for the high-side MOSFET as it is switched. The recommended capacitor value is between 100nF and 1.0μF. An external diode is required with the LP1110.
2	PWM	Logic-Level Input. This pin has primary control of the drive outputs.
3	EN	Active high output enable. When low, normal operation is disabled forcing DRVH and DRVL low.
4	VCC	Input Supply. A 1.0μF ceramic capacitor should be connected from this pin to PGND.
5	DRVL	Output drive for the lower MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SWN	Switch Node. Connect to the source of the upper MOSFET.
8	DRVH	Output drive for the upper MOSFET.

Function Diagram



Timing Diagram

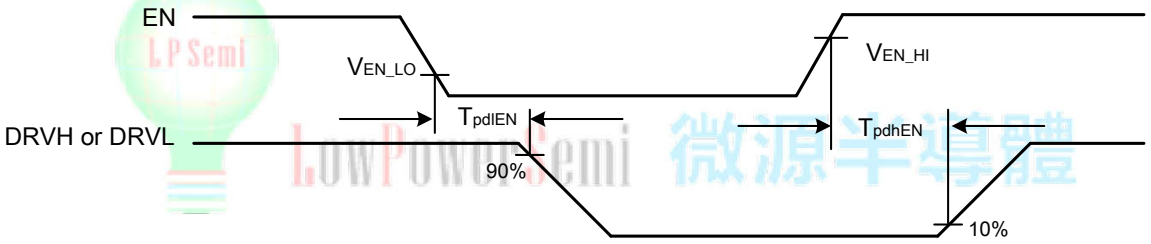


Figure 1. EN Timing waveforms

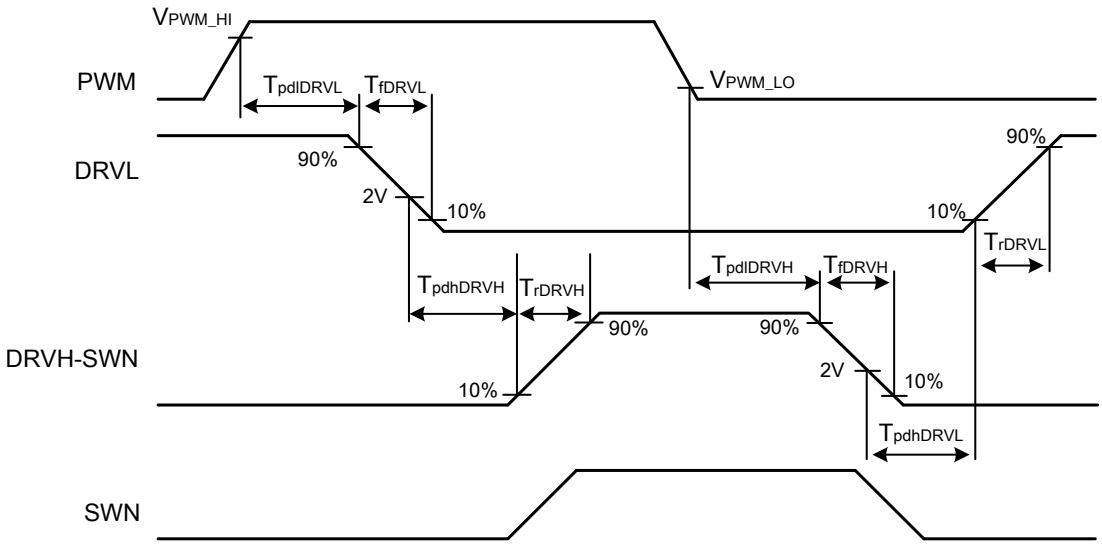


Figure 2. Input-Output Timing waveforms

Absolute Maximum Ratings

- ✧ VCC ---------- -0.3V to 15V
- ✧ BST ---------- -0.3V to 35V
- ✧ BST to SWN ---------- -0.3V to 15V
- ✧ SWN ---------- -5V to 20V
- ✧ DRVH ---------- SWN-0.3V to BST+0.3V
- ✧ DRVL ---------- -0.3V to VCC+0.3V
- ✧ EN,PWM ---------- -0.3V to 6.5V
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads,10 sec) ---------- 260℃
- ✧ Storage Temperature ---------- -65℃ to 150℃
- ✧ Operating Ambient Temperature Range ---------- -40℃ to 85℃

Note1：All voltages are with respect to PGND except where noted.

Note2：Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note3: This device is ESD sensitive. Use standard ESD precautions when handling.

Thermal Information

Package Thermal Resistance (DFN-8, Note4)

- ✧ Junction to Ambient, θ_{JA} ---------- 70℃/W
- ✧ Junction to Case, θ_{JC} ---------- 51℃/W

Note4： θ_{JA} measured with reference to JEDEC51-2; θ_{JC} measured with reference to JEDEC 51-14.

Electrical Characteristics

(VCC = 12 V, TA =25°C, unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply						
Supply Voltage Range	VCC	–	4.6	–	13.2	V
Supply Current	ISYS	BST = 12 V, IN = 0 V, EN=0V	–	0.7	–	mA
EN Input						
Input Voltage High	VEN_HI	–	2.0	–	–	V
Input Voltage Low	VEN_LO	–	–	–	0.8	V
Hysteresis		–	–	300	–	mV
Input Current		No internal pull-up or pull-down resistors	−1.0	–	+1.0	μA
PWM Input						
Input Voltage High	VPWM_HI	–	2.0	–	–	V
Input Voltage Low	VPWM_LO	–	–	–	0.8	V
Hysteresis	–	–	–	300	–	mV
Input Current	–	No internal pull-up or pull-down resistors	−1.0	–	+1.0	μA
High-Side Driver						
Output Resistance, Sourcing Current	–	BST – SWN = 12 V	–	3.3	-	Ω
Output Resistance, Sinking Current	–	BST – SWN = 12 V	–	0.5	-	Ω
Output Resistance, Unbiased	–	BST – SWN = 0 V	–	15	-	kΩ
Transition Times	trDRVH	BST – SWN = 12 V, CLOAD = 3.0 nF (See Figure 2)	–	30	-	ns
	tfDRVH			12	-	ns
Propagation Delay Times	tpdhDRVH	BST – SWN = 12 V, CLOAD = 3.0 nF (See Figure 2)	-	95	-	ns
	tpdlDRVH	BST – SWN = 12 V, CLOAD = 3.0 nF (See Figure 2)		15	-	ns
	tpdlEN	(See Figure 1)		30	-	ns
	tpdhEN	(See Figure 1)		35	-	ns
SW Pull-down Resistance	–	SWN to PGND	–	15	–	kΩ
Low-Side Driver						
Output Resistance, Sourcing Current	–		–	3.3	-	Ω
Output Resistance, Sinking Current	–		–	0.5	–	Ω
Output Resistance, Unbiased	–	VCC = PGND	–	15	–	kΩ
Transition Times	trDRVL	CLOAD = 3.0 nF, (See Figure 2)	–	30	-	ns
	tfDRVL			12	-	ns
Propagation Delay Times	tpdhDRVL	CLOAD = 3.0 nF, (See Figure 2)	–	105	-	ns
	tpdlDRVL		-	15	-	ns
	tpdlEN	(See Figure 1)	-	30	-	ns
	tpdhEN	(See Figure 1)	-	35	-	ns
Timeout Delay	–	DRVH – SWN = 0	–	110	–	ns
Under Voltage Lockout						
UVLO Startup	–	–	-	4.3	-	V
UVLO Shutdown	–	–	-	4.0	-	V
Hysteresis	–	–	-	0.3	-	V

Operation Information

The LP1110 is a single phase MOSFET driver for driving two N-channel MOSFETs in a synchronous buck converter topology. The LP1110 will operate from 5.0V or 12V, but have been optimized for high current multi-phase buck regulators that convert 12 V rail directly to the core voltage required by complex logic chips.

A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3nF load at frequencies up to 1 MHz.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(ON)}$ N-Channel MOSFET. The voltage rail for the low-side driver is internally connected to the VCC supply and PGND.

High-Side Driver

The high−side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (SWN) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the LP1110 are starting up, the SWN pin is at ground, so the bootstrap capacitor will charge up to VCC through the bootstrap diode. When the PWM input goes high, the high-side driver will begin to turn on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the SWN pin will rise. When the high-side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24V).The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot-through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The LP1110 prevent cross conduction by monitoring the status of the external MOSFETs and applying the appropriate amount of “dead-time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET. When the PWM input pin goes high, DRVL will go low after a propagation delay (tpdlDRVL). The time it takes for the low-side MOSFET to turn off (tfDRVL) is dependent on the total charge on the low-side MOSFET gate. The LP1110 monitor the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhDRVH) the turn on of the high-side MOSFET.

Likewise, when the PWM input pin goes low, DRVH will go low after the propagation delay (tpdlDRVH). The time to turn off the high-side MOSFET (tfDRVH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high-side MOSFET has stopped conducting, to delay (tpdhDRVL) the turn on of the low-side MOSFET.

Power Supply Decoupling

The LP1110 can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage(VCC), a low ESR capacitor should be placed near the power and ground pins. A 1μF to 4.7μF multilayer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

The PWM and the EN pins of the LP1110 have internal protection for Electro Static Discharge (ESD), but in normal operation they present relatively high input impedance. If the PWM controller does not have internal pull-down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the external diode. Selection of these components can be done after the high-side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where Q_{GATE} is the total gate charge of the high-side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive.

For example, an external MOSFET has a total gate charge of about 30nC. For an allowed droop of 300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor should be used. The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SWN. The average forward current can be estimated by:

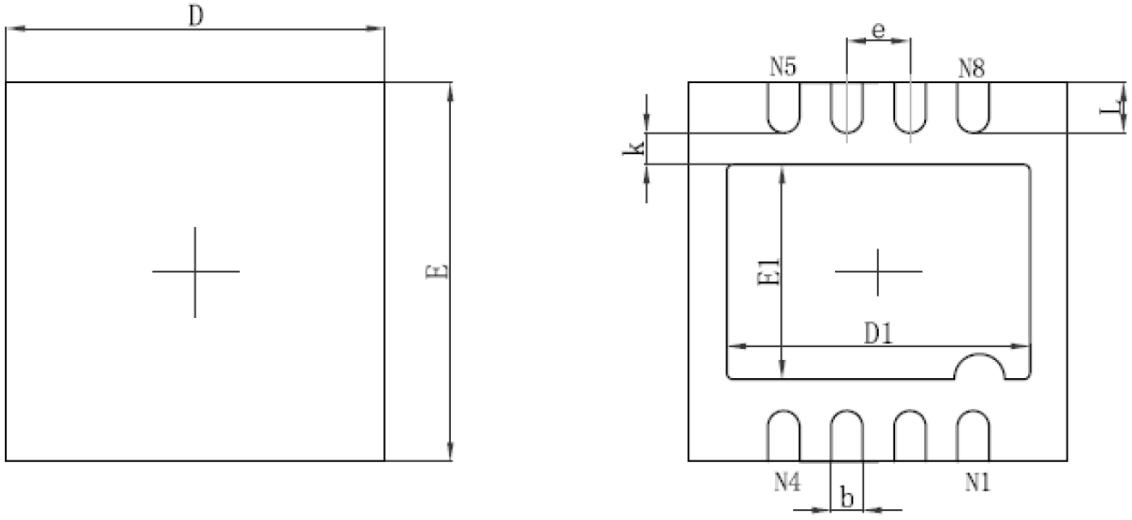
$$I_{F(AVG)} = Q_{GATE} \times F_{MAX}$$

Where F_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in-circuit, since this is dependent on the source impedance of the 12V supply and the ESR of C_{BST}.

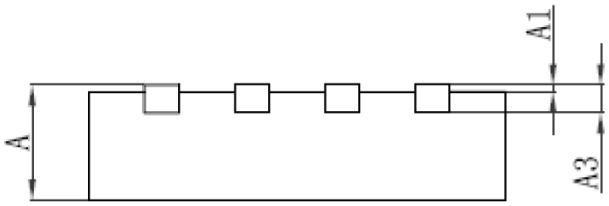
Layout Guideline

Packaging Information

DFN8



Top View Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Gate Drivers ***category:***

Click to view products by LOWPOWER ***manufacturer:***

Other Similar products are found below :

00028 00053P0231 8967380000 56956 CR7E-30DB-3.96E(72) 57.404.7355.5 LT4936 57.904.0755.0 5801-0903 5803-0901 5811-0902 5813-0901 58410 00576P0030 00581P0070 5882900001 00103P0020 00600P0005 00-9050-LRPP 00-9090-RDPP 5951900000 01-1003W-10/32-15 LTILA6E-1S-WH-RC-FN12VXCR1 0131700000 00-2240 LTP70N06 LVP640 0158-624-00 5J0-1000LG-SIL 020017-13 LY1D-2-5S-AC120 LY2-0-US-AC120 LY2-US-AC240 LY3-UA-DC24 00-5150 00576P0020 00600P0010 LZNQ2M-US-DC5 LZNQ2-US-DC12 LZP40N10 00-8196-RDPP 00-8274-RDPP 00-8275-RDNP 00-8609-RDPP 00-8722-RDPP 00-8728-WHPP 00-8869-RDPP 00-9051-RDPP 00-9091-LRPP 00-9291-RDPP