



Dual N -Channel Enhancement Power MOSFET

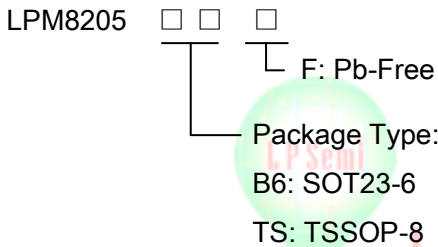
General Description

The LPM8205 integrates two N-Channel Enhancement MOSFET Transistor. It uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for using in DC-DC conversion, power switch and charging circuit. Standard Product LPM8205 is Pb-free and Halogen-free.

Features

- ◆ 100% EAS Guaranteed
- ◆ Green Device Available
- ◆ Super Low Gate Charge
- ◆ Excellent CdV/dt effect decline
- ◆ Advanced high cell density Trench technology

Order Information



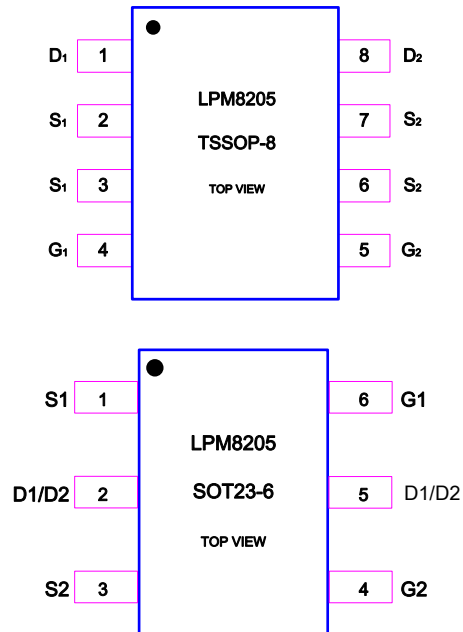
Applications

- ◇ Driver for Relay, Solenoid, Motor, LED etc.
- ◇ DC-DC converter circuit
- ◇ Power Switch
- ◇ Load Switch
- ◇ Charging

Marking Information

Device	Marking	Package	Shipping
LPM8205B6F		SOT23-6	
LPM8205TSF		TSSOP-8	

Pin Configurations



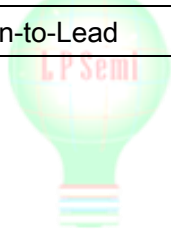


Absolute Maximum Ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current	TA=25°C	I_D	7.6	A
	TA=70°C		6.1	
Pulsed Drain Current		I_{DM}	38	
Power Dissipation	TA=25°C	P_D	2	W
	TA=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal resistance ratings

Parameter		Symbol	TYP	Unit
Junction-to-Case Thermal Resistance	$t \leq 10s$	$R_{\theta JA}$	48	°C/W
Junction-to-Case Thermal Resistance	Steady State		74	°C/W
Maximum Junction-to-Lead	Steady State	$R_{\theta JL}$	32	°C/W





Electrical Characteristics

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.4	0.75	1.1	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	38			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=7.6\text{A}$ $T_J=125^\circ\text{C}$		16.5	23	m Ω
				25	30	
		$V_{GS}=4.5\text{V}$, $I_D=7\text{A}$		18.5	26	
		$V_{GS}=2.5\text{V}$, $I_D=6\text{A}$		24	34	
		$V_{GS}=1.8\text{V}$, $I_D=2\text{A}$		32	52	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=7.6\text{A}$		25		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$	420	525	630	pF
C_{oss}	Output Capacitance		65	95	125	pF
C_{riss}	Reverse Transfer Capacitance		45	75	105	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.8	1.7	2.6	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=7.6\text{A}$		12.5		nC
$Q_g(4.5\text{V})$	Total Gate Charge			6		nC
Q_{gs}	Gate Source Charge			1		nC
Q_{gd}	Gate Drain Charge			2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=2\Omega$, $R_{GEN}=3\Omega$		3		ns
t_r	Turn-On Rise Time			7.5		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=7.6\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		14		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7.6\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		6		nC



Typical Characteristics

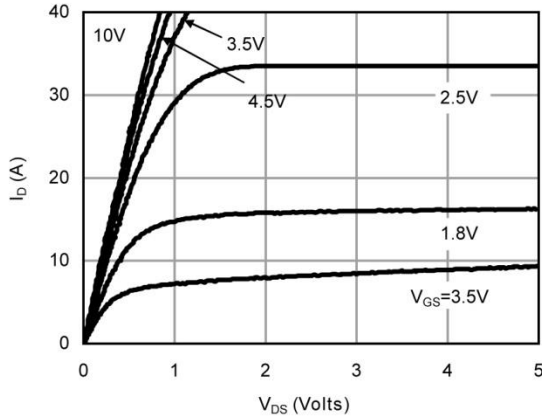


Fig 1: On-Region Characteristics (Note E)

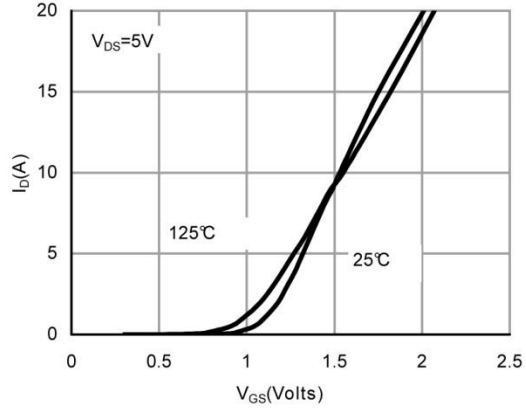


Figure 2: Transfer Characteristics (Note E)

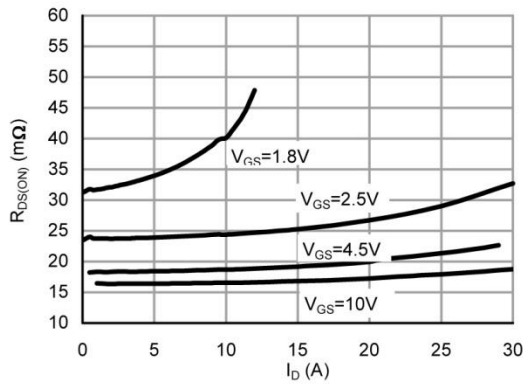


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

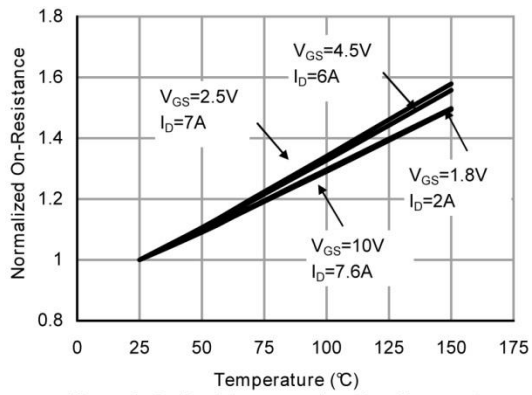


Figure 4: On-Resistance vs. Junction Temperature (Note E)

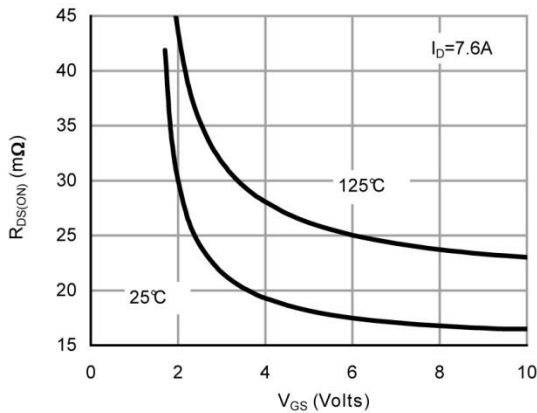


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

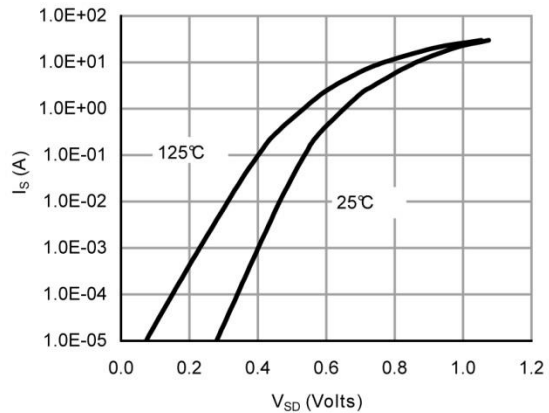


Figure 6: Body-Diode Characteristics (Note E)

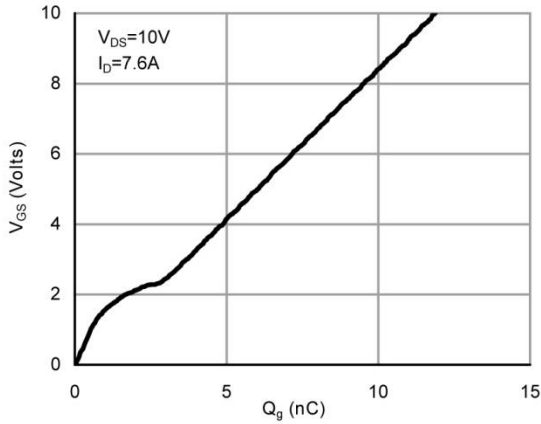


Figure 7: Gate-Charge Characteristics

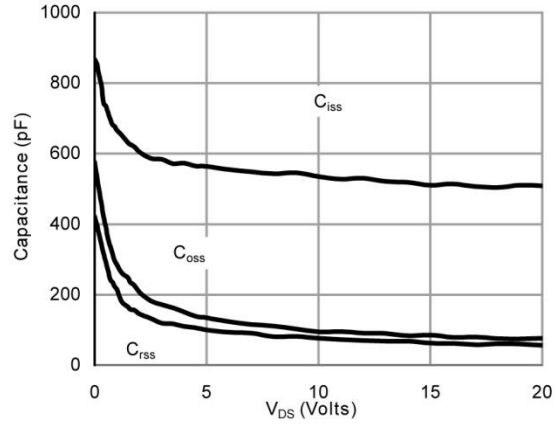


Figure 8: Capacitance Characteristics

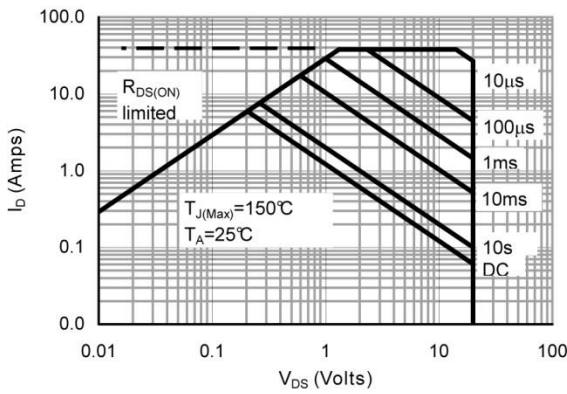


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

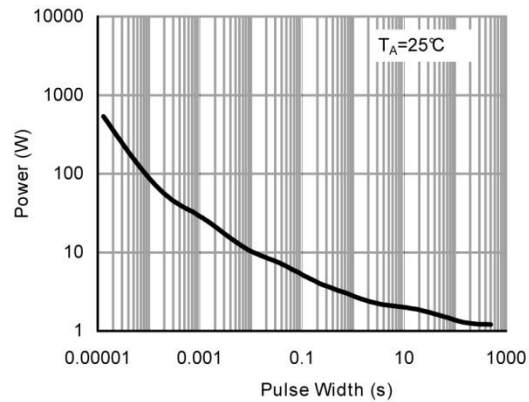


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

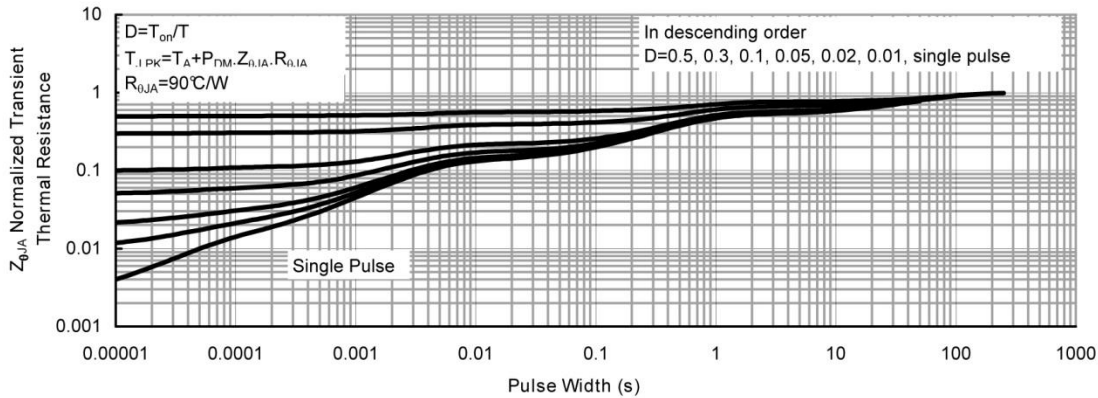
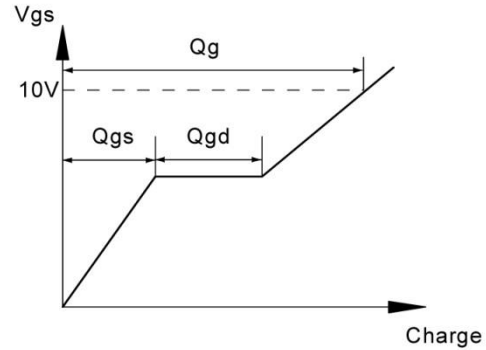
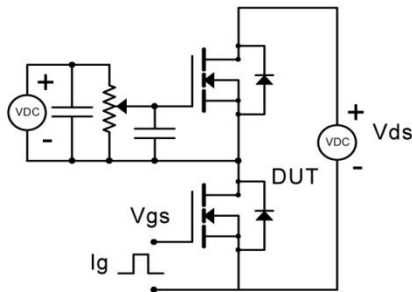


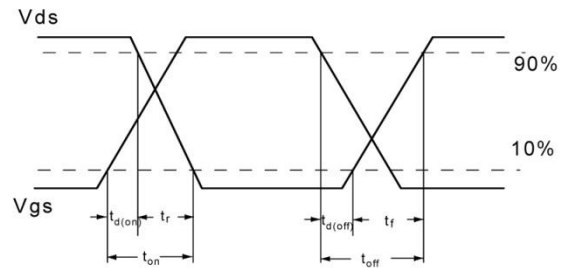
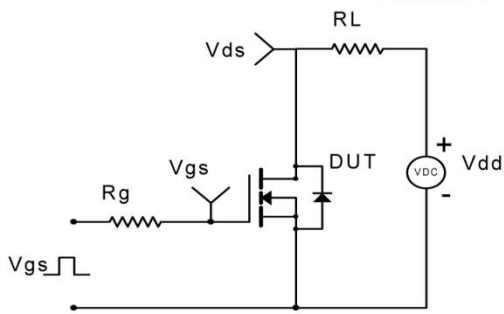
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



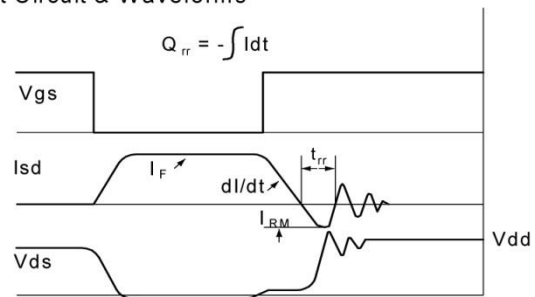
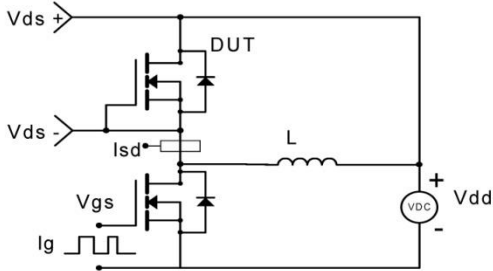
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



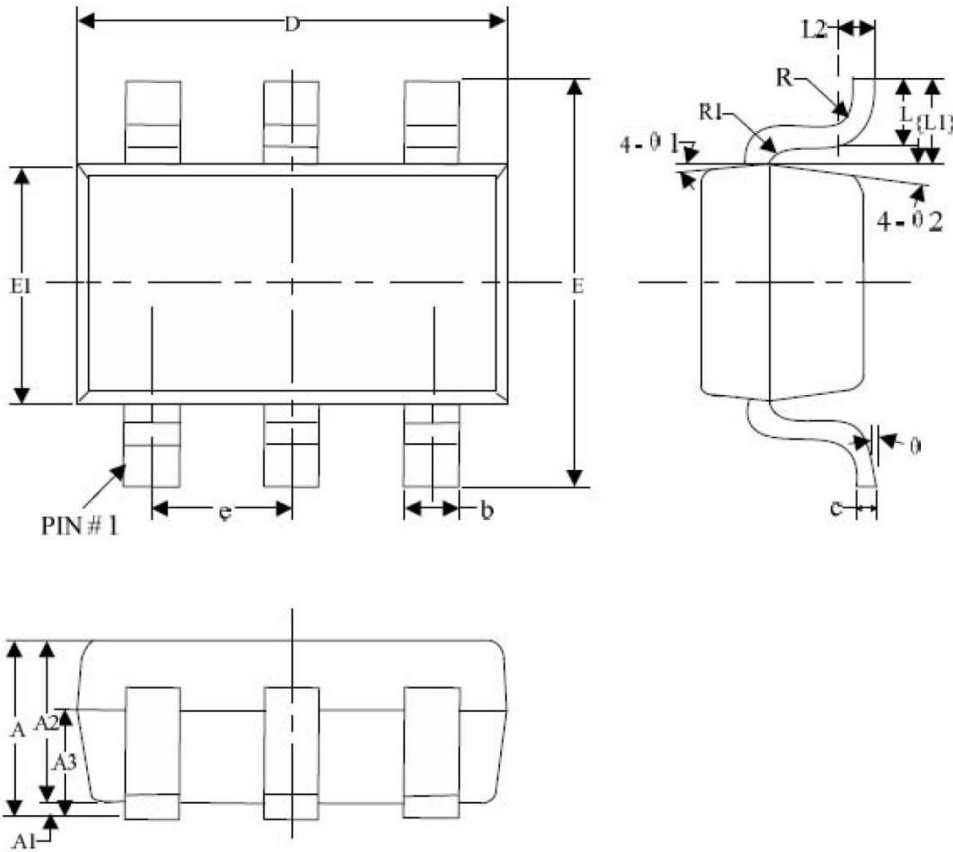
Diode Recovery Test Circuit & Waveforms





Packaging Information

SOT23-6

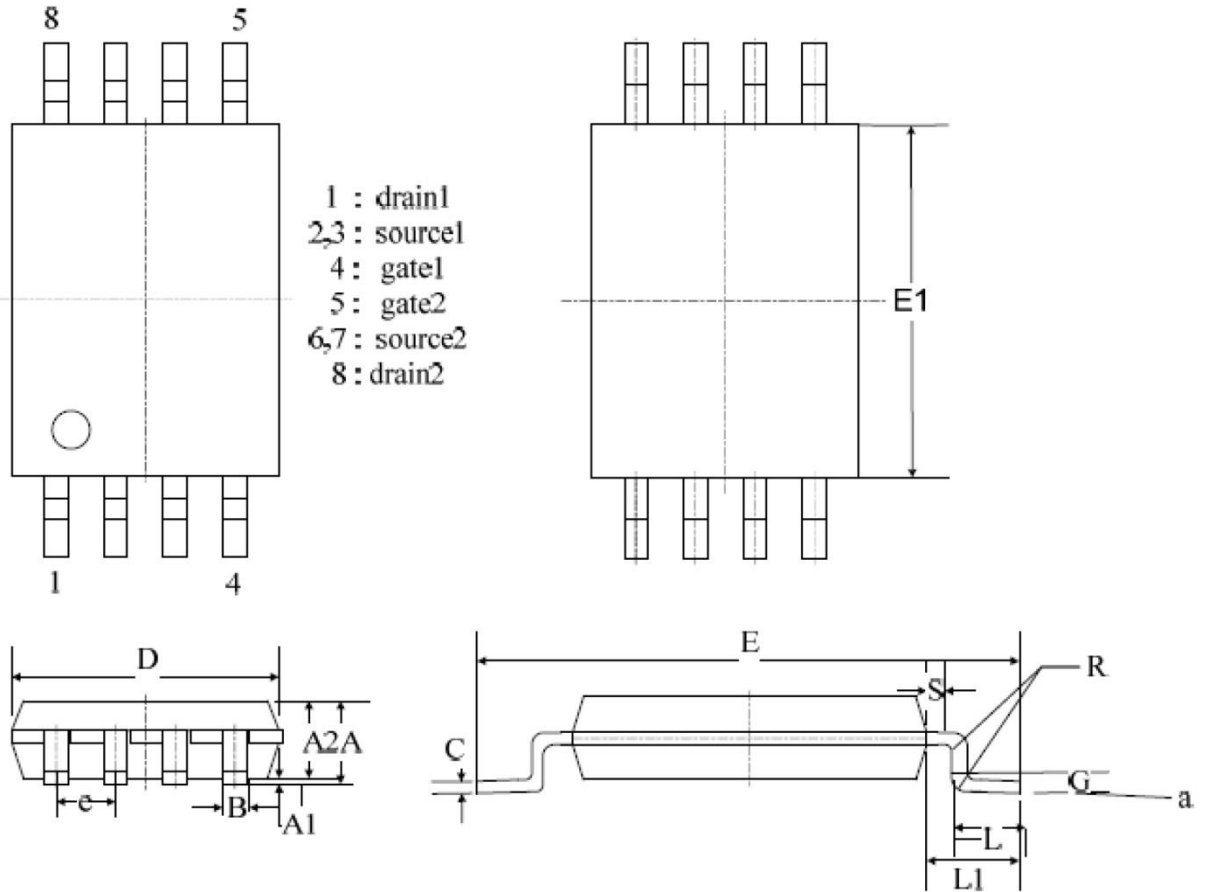


Dimensions (unit: mm)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	-	-	1.30	e	0.85	0.95	1.05
A1	0	-	0.15	L	0.35	0.45	0.60
A2	0.90	1.10	1.30	L1	0.59REF		
A3	0.60	0.65	0.70	L2	0.25BSC		
b	0.39	-	0.49	R	0.05	-	-
c	0.12	-	0.19	R1	0.05	-	0.02
D	2.85	2.95	3.15	θ	0°	-	8°
E	2.60	2.80	3.00	θ1	3°	5°	7°
E1	1.55	1.65	1.75	θ2	6°	8°	10°



TSSOP-8



DIM		A	A(1)	A(2)	B	C	D	E	E1	e	G	L	L1	a	R	S		
MM	Min.	1.05	0.05	0.99	0.19		2.9	6.2	4.3	0.65 BSC	0.254 GAGE PLANE	0.45	0.9	0°	0.09	0.2		
	Nom.	1.1	0.1	1.02	0.25	0.127	3	6.4	4.4			0.6	1	4°				
	Max.	1.2	0.15	1.05	0.3		3.2	6.6	4.5			0.75	1.1	8°				

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