LPM2301 -20V/-2A
# P-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM2301 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Ordering Information

LPM2301- □ □   □

└ F: Pb-Free

Package Type
B3: SOT23
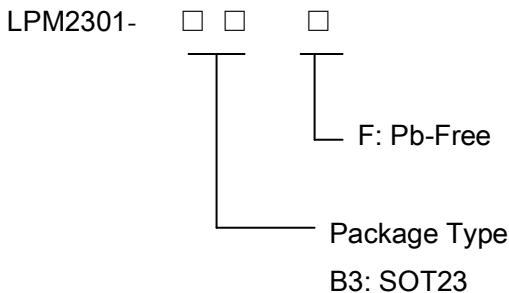
Features

- -20V/-2.0A, $R_{DS(ON)}$=170mΩ(typ.)@VGS=-2.5V
- -20V/-2.0A, $R_{DS(ON)}$=130mΩ(typ.)@VGS=-4.5V
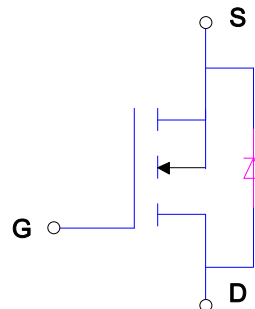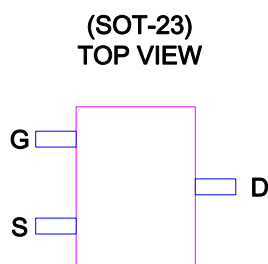- Super high density cell design for extremely low $R_{DS(ON)}$
- SOT23 Package

Applications

- Portable Media Players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM2301B3F	A1šHB	SOT23	3K/REEL

Pin Configurations

(SOT-23)
TOP VIEW

Absolute Maximum Ratings　T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current A	T_A=25°C	I_D	-2	A
	T_A=70°C		-1.5	
Pulsed Drain Current B		I_{DM}	-8	
Power Dissipation A	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ.	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	130	°C/W
Maximum Junction-to-Ambient	Steady-State		160	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	80	°C/W

Functional Pin Description

| Symbol	Parameter	Condition	Min	Typ.	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			-1	uA
		T_J=55°C			-10	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.4		-1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-2A		130		mΩ
		V_{GS}=-2.5V, I_D=-2A		170		mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-2A		10		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		400		pF
C_{oss}	Output Capacitance			220		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-2A		7		nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=3.6Ω, R_{GEN}=6Ω		15		nS
t_r	Turn-On Rise Time			36		
$t_{D(off)}$	Turn-Off DelayTime			42		
t_f	Turn-Off Fall Time			34		

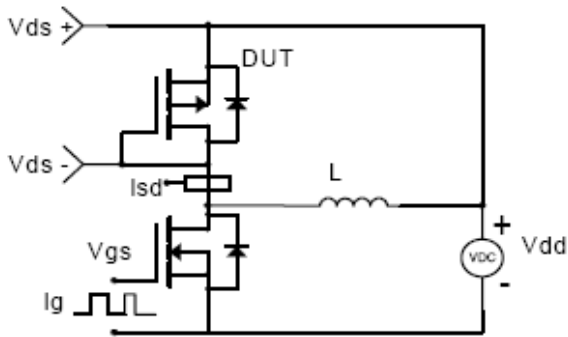## Gate Charge Test Circuit & Waveform
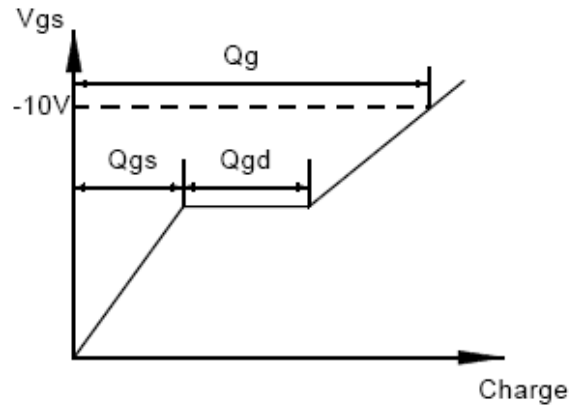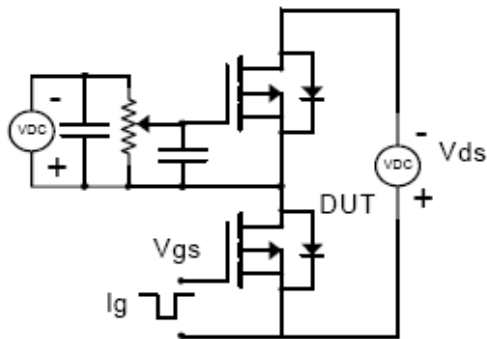
Resistive Switching Test Circuit & Waveforms
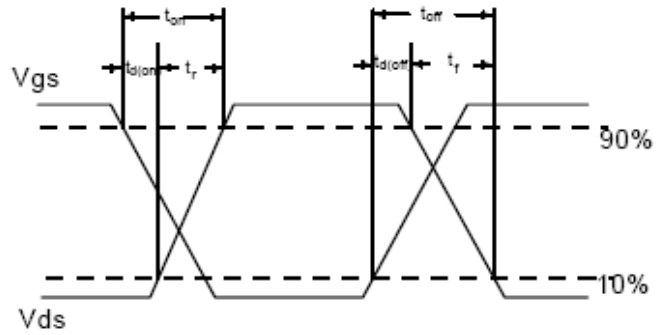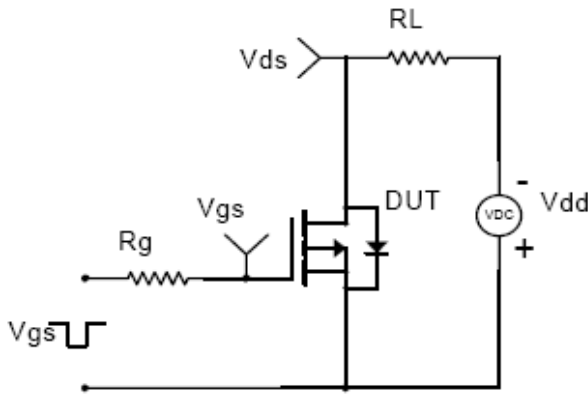
Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$
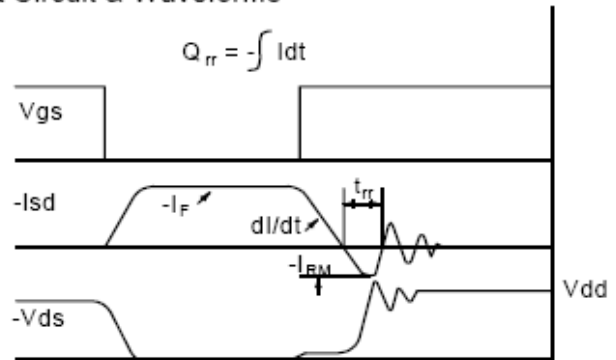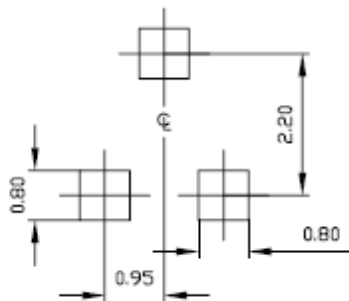
Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE
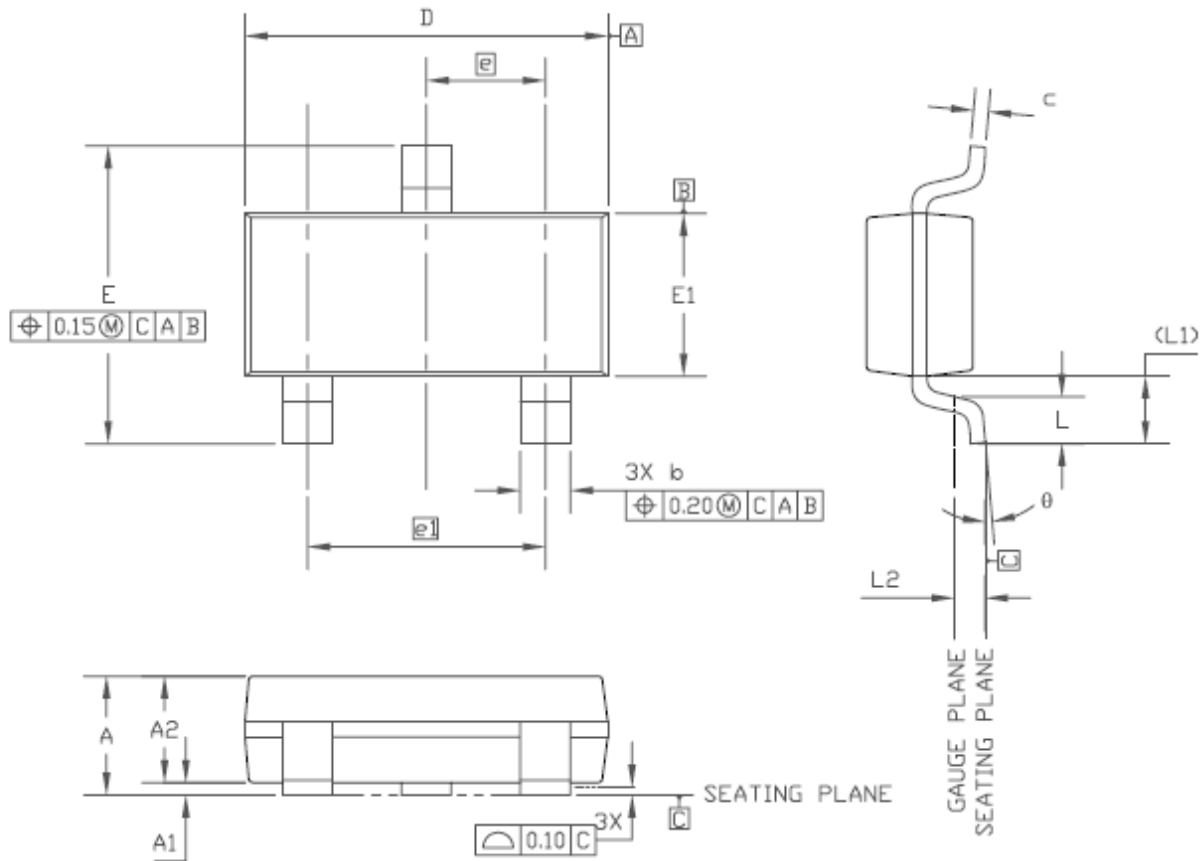
RECOMMENDED LAND PATTERN

UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°

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