

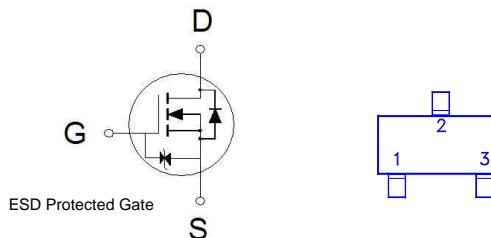
**NIKO-SEM**
**N-Channel Logic Level Enhancement  
Mode Field Effect Transistor**
**PZD502CYB**

SOT-523

Halogen-Free &amp; Lead-Free

**PRODUCT SUMMARY**

| $V_{(BR)DSS}$ | $R_{DS(ON)}$  | $I_D$ |
|---------------|---------------|-------|
| 20V           | 450m $\Omega$ | 0.7A  |


 1. GATE  
 2. DRAIN  
 3. SOURCE
**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$  Unless Otherwise Noted)**

| PARAMETERS/TEST CONDITIONS                     | SYMBOL         | LIMITS     | UNITS |
|--|----------------|------------|-------|
| Drain-Source Voltage                           | $V_{DS}$       | 20         | V     |
| Gate-Source Voltage                            | $V_{GS}$       | $\pm 8$    | V     |
| Continuous Drain Current                       | $I_D$          | 0.7        | A     |
|  |                | 0.6        |       |
| Pulsed Drain Current <sup>1</sup>              | $I_{DM}$       | 2          |       |
| Power Dissipation                              | $P_D$          | 0.4        | W     |
|  |                | 0.2        |       |
| Operating Junction & Storage Temperature Range | $T_j, T_{stg}$ | -55 to 150 | °C    |

**THERMAL RESISTANCE RATINGS**

| THERMAL RESISTANCE               | SYMBOL          | TYPICAL | MAXIMUM | UNITS |
|----------------------------------|-----------------|---------|---------|-------|
| Junction-to-Ambient <sup>2</sup> | $R_{\theta JA}$ |         | 280     | °C/W  |

<sup>1</sup>Pulse width limited by maximum junction temperature.<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ C$ . The value in any given application depends on the user's specific board design.**ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ C$ , Unless Otherwise Noted)**

| PARAMETER                                     | SYMBOL        | TEST CONDITIONS                               | LIMITS |     |          | UNIT      |
|---|---------------|---|--------|-----|----------|-----------|
|   |               |   | MIN    | TYP | MAX      |           |
| <b>STATIC</b>                                 |               |   |        |     |          |           |
| Drain-Source Breakdown Voltage                | $V_{(BR)DSS}$ | $V_{GS} = 0V, I_D = 250\mu A$                 | 20     |     |          | V         |
| Gate Threshold Voltage                        | $V_{GS(th)}$  | $V_{DS} = V_{GS}, I_D = 250\mu A$             | 0.35   | 0.6 | 1        |           |
| Gate-Body Leakage                             | $I_{GSS}$     | $V_{DS} = 0V, V_{GS} = \pm 8V$                |        |     | $\pm 30$ | $\mu A$   |
| Zero Gate Voltage Drain Current               | $I_{DSS}$     | $V_{DS} = 16V, V_{GS} = 0V$                   |        |     | 1        | $\mu A$   |
|   |               | $V_{DS} = 10V, V_{GS} = 0V, T_J = 55^\circ C$ |        |     | 10       |           |
| Drain-Source On-State Resistance <sup>1</sup> | $R_{DS(ON)}$  | $V_{GS} = 1.8V, I_D = 0.35A$                  |        | 384 | 850      | $m\Omega$ |
|   |               | $V_{GS} = 2.5V, I_D = 0.5A$                   |        | 274 | 765      |           |
|   |               | $V_{GS} = 4.5V, I_D = 0.6A$                   |        | 213 | 450      |           |
| Forward Transconductance <sup>1</sup>         | $g_{fs}$      | $V_{DS} = 5V, I_D = 0.6A$                     |        | 2   |          | S         |

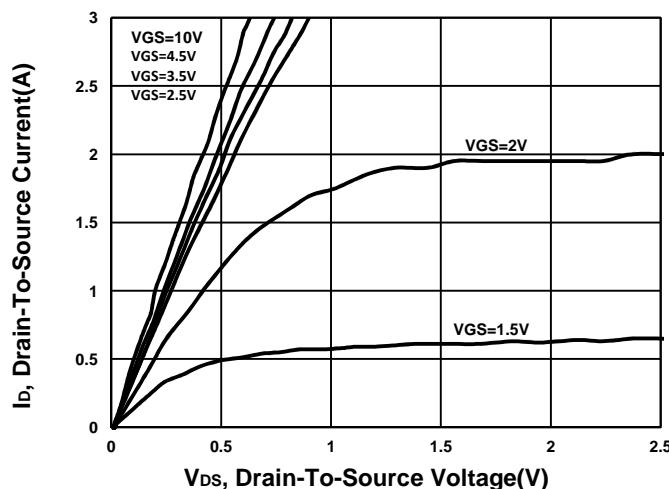
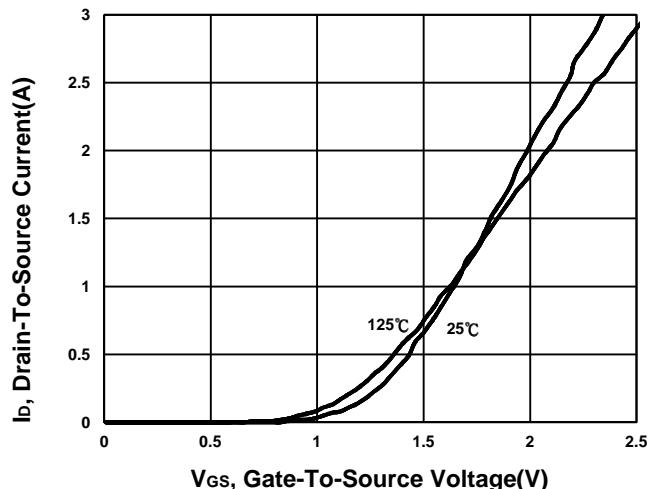
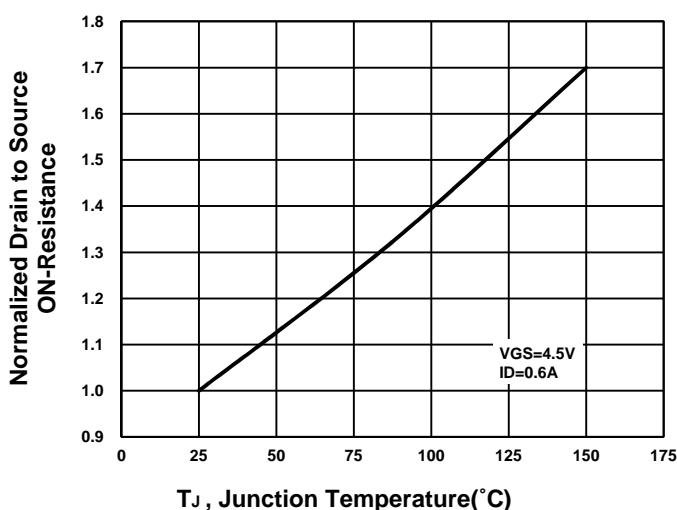
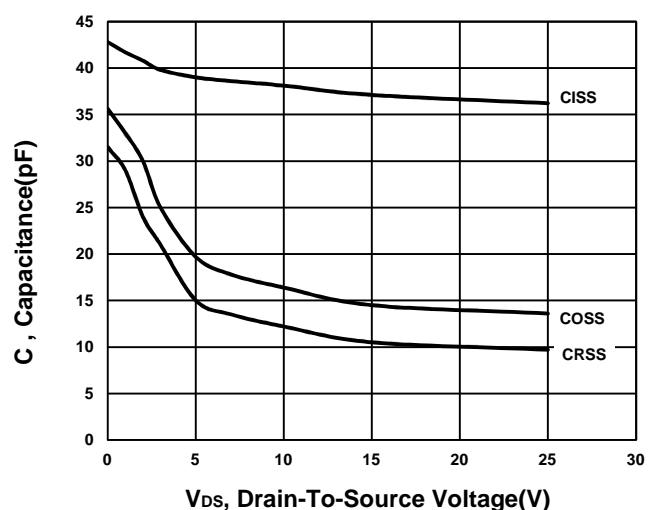
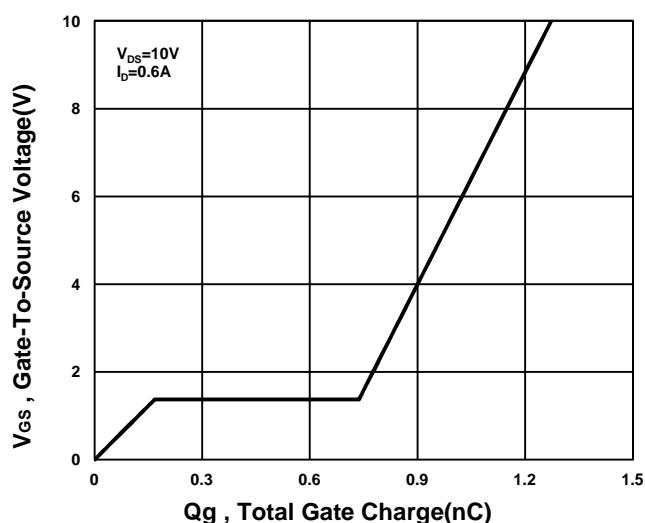
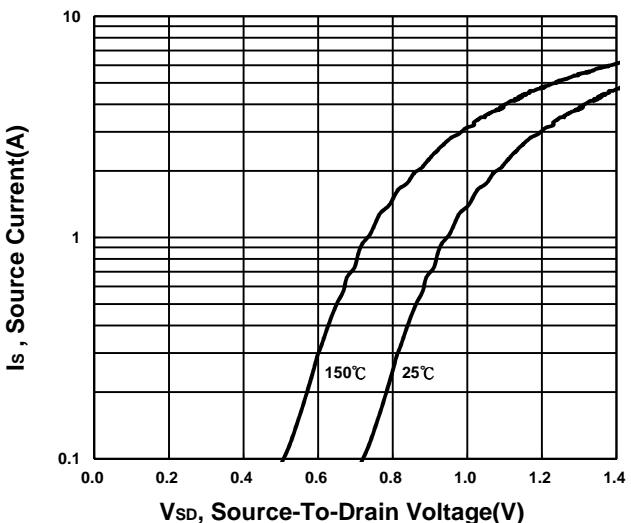
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| DYNAMIC   |              |   |  |     |   |    |
|---|--------------|---|--|-----|---|----|
| Input Capacitance   | $C_{iss}$    | $V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$                             |  | 38  |   | pF |
| Output Capacitance  | $C_{oss}$    |   |  | 16  |   |    |
| Reverse Transfer Capacitance  | $C_{rss}$    |   |  | 12  |   |    |
| Total Gate Charge <sup>2</sup>  | $Q_g$        | $V_{DS} = 10V, V_{GS} = 4.5V, I_D = 0.6A$                         |  | 1.4 |   | nC |
| Gate-Source Charge <sup>2</sup>                                       | $Q_{gs}$     |   |  | 0.4 |   |    |
| Gate-Drain Charge <sup>2</sup>  | $Q_{gd}$     |   |  | 0.8 |   |    |
| Turn-On Delay Time <sup>2</sup>                                       | $t_{d(on)}$  | $V_{DS} = 6V, I_D \approx 0.6 A, V_{GS} = 4.5V, R_{GS} = 6\Omega$ |  | 6   |   | nS |
| Rise Time <sup>2</sup>  | $t_r$        |   |  | 18  |   |    |
| Turn-Off Delay Time <sup>2</sup>                                      | $t_{d(off)}$ |   |  | 30  |   |    |
| Fall Time <sup>2</sup>  | $t_f$        |   |  | 25  |   |    |
| SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_J = 25^\circ C$ ) |              |   |  |     |   |    |
| Continuous Current  | $I_S$        |   |  | 0.7 | A |    |
| Forward Voltage <sup>1</sup>  | $V_{SD}$     | $I_F = 0.15A, V_{GS} = 0V$  |  | 1.2 | V |    |
| Reverse Recovery Time   | $t_{rr}$     | $V_{DS} = 12V, I_F = 2A, dI_F/dt = 100 A/\mu s$                   |  | 233 |   | nS |
| Reverse Recovery Charge   | $Q_{rr}$     |   |  | 630 |   | nC |

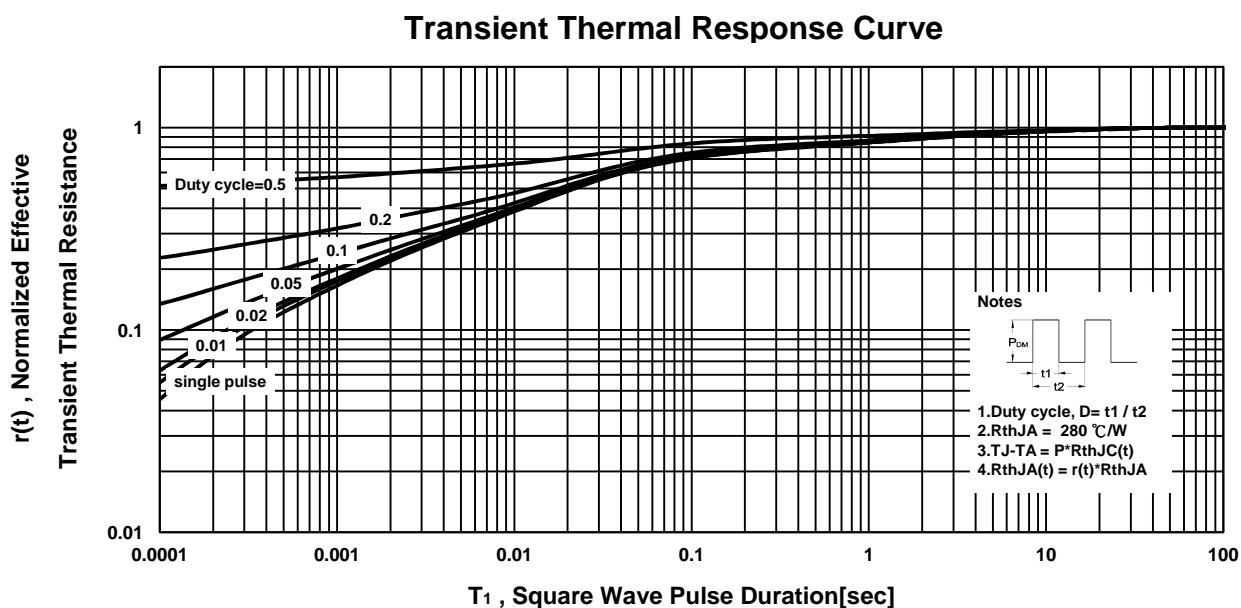
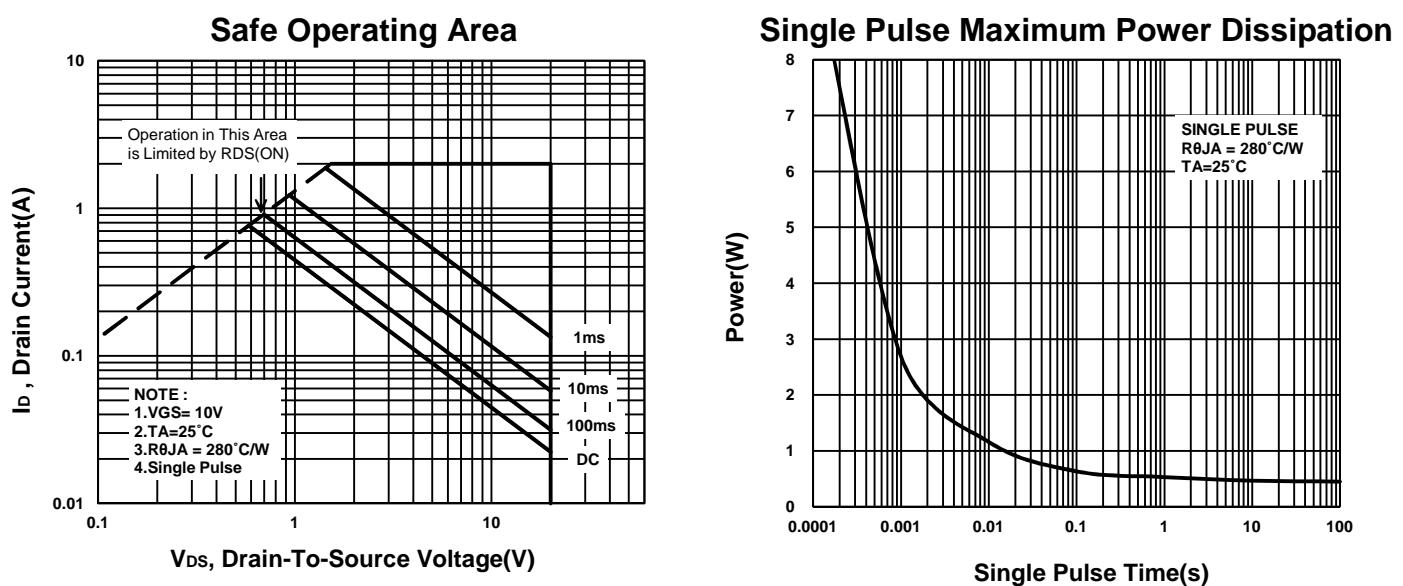
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .<sup>2</sup>Independent of operating temperature.

**NIKO-SEM****N-Channel Logic Level Enhancement  
Mode Field Effect Transistor****PZD502CYB  
SOT-523  
Halogen-Free & Lead-Free****Output Characteristics****Transfer Characteristics****On-Resistance VS Temperature****Capacitance Characteristic****Gate charge Characteristics****Source-Drain Diode Forward Voltage**

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SOT-523  
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