



## LPM2302 20V/3.5A

# N-Channel Enhancement Mode Field Effect Transistor

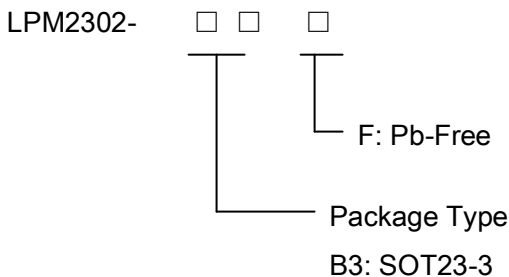
### General Description

The LPM2302 is N-channel logic enhancement mode power field effect transistor, which are produced by using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suitable for low voltage applications, notebook computer power management and other battery powered circuits where high-side switching are needed.

### Ordering Information



### Features

- 20V/3.5A,  $R_{DS(ON)}=50m\Omega(Typ.)@V_{GS}=4.5V$
- 20V/3.0A,  $R_{DS(ON)}=75m\Omega(Typ.)@V_{GS}=2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- SOT23 Package

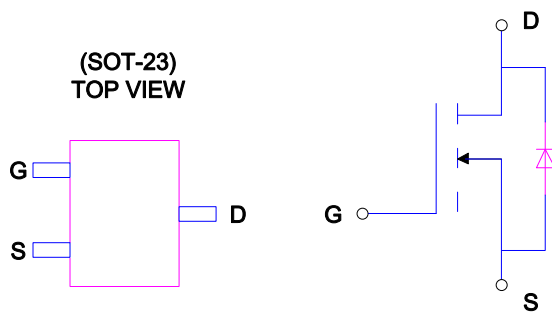
### Applications

- ◇ Portable Media Players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

### Marking Information

Device	Marking	Package	Shipping
LPM2302B3F	A23HB	SOT23-3	3K/REEL

### Pin Configurations





## Functional Pin Description

Name	Description
G	Gate Electrode
S	Source
D	Drain Electrode

## Absolute Maximum Ratings

Absolute Maximum Ratings TA=25°C Unless Otherwise noted				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current A	TA=25°C	$I_D$	3.5	A
	TA=70°C		2.4	
Pulsed Drain Current E		$I_{DM}$	8	
Power Dissipation	TA=25°C	$P_O$	1.25	W
	TA=70°C		0.8	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter		Symbol	Typ.	Units
Maximum Junction-to-Ambient	$t \leq 10S$	$R_{\theta JA}$	130	°C/W
Maximum Junction-to-Ambient	Steady-state		160	°C/W
Maximum Junction-to-Lead	Steady-state	$R_{\theta JL}$	80	°C/W

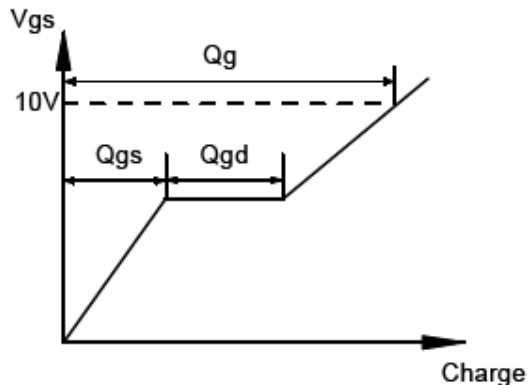
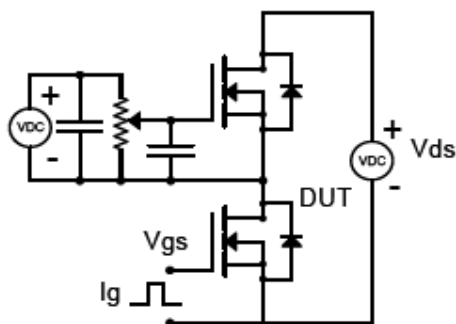


## Electrical Characteristics

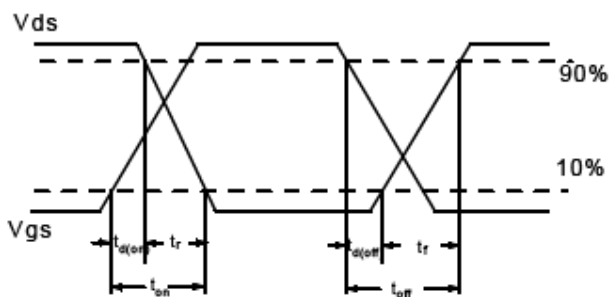
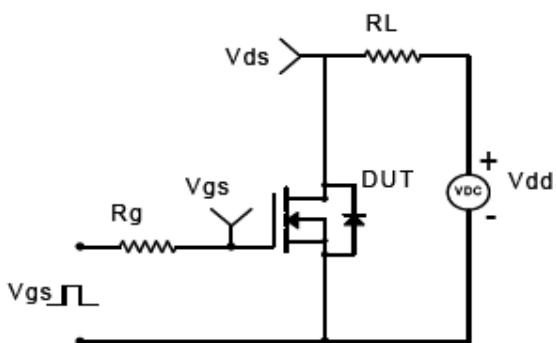
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>STATIC PARAMETER</b>						
BVDSS	Drain-Source Breakdown Voltage	ID=250 $\mu$ A , VGS=0V	20			V
IDSS	Zero-Gate Voltage Drain Current	VDS=16V,VGS=0V TJ=55°C			1 5	$\mu$ A
IGSS	Gate-Body Leakage Current	VDS=0V,VGS= $\pm$ 12V			1	$\mu$ A
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250 $\mu$ A	0.4	0.7	1	V
RDS(ON)	Static Drain-Source On-Resistance	VGS=4.5V, ID=3.5A		50		m $\Omega$
		VGS=2.5V, ID=3A		75		m $\Omega$
gFS	Forward Transconductance	VDS=5V,ID=3A		12		S
VSD	Diode Forward Voltage	IS=1A,VGS=0V		0.75	1	V
<b>DYNAMIC PARAMETERS</b>						
Ciss	Input Capacitance	VDS=10V,VGS=0V		330		pF
CDSS	Output Capacitance	f = 1MHz		110		pF
Crss	Reverse Transfer Capacitance			30		pF
Rg	Gate Resistance	VDS=0V,VGS=0V f = 1MHz		4		$\Omega$
<b>SWITCHING PARAMETERS</b>						
Qg	Total Gate Charge	VDS=10V,VGS=4.5V ID=3.5A		4.2		nC
Qgs	Gate Source Charge			1		nC
Qgd	Gate Drain Charge			0.5		nC
tD(ON)	Turn-On Delay Time	VDS=10V,VGS=5V RL=2.7 $\Omega$ ,RGEN=1 $\Omega$		10		nS
t <sub>r</sub>	Turn-On Rise Time			8		nS
tD(OFF)	Turn-Off Delay Time			35		nS
t <sub>f</sub>	Turn-Off Fall Time			10		nS
t <sub>rr</sub>	Body-Diode Reverse Recovery Time	IF=3A,d I/dt=100A/ $\mu$ S		12.3		nS
Q <sub>rr</sub>	Body-Diode Reverse Recovery Charge	IF=3A,d I/dt=100A/ $\mu$ S		2.5		nC



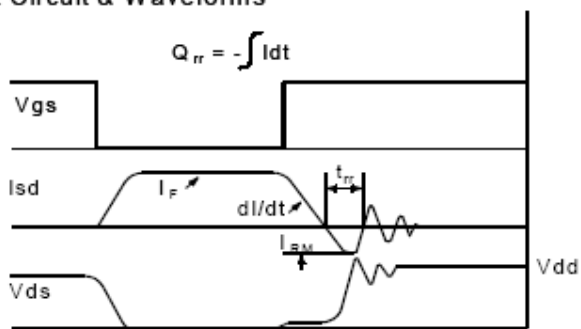
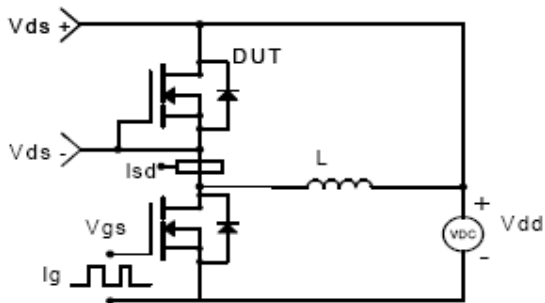
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



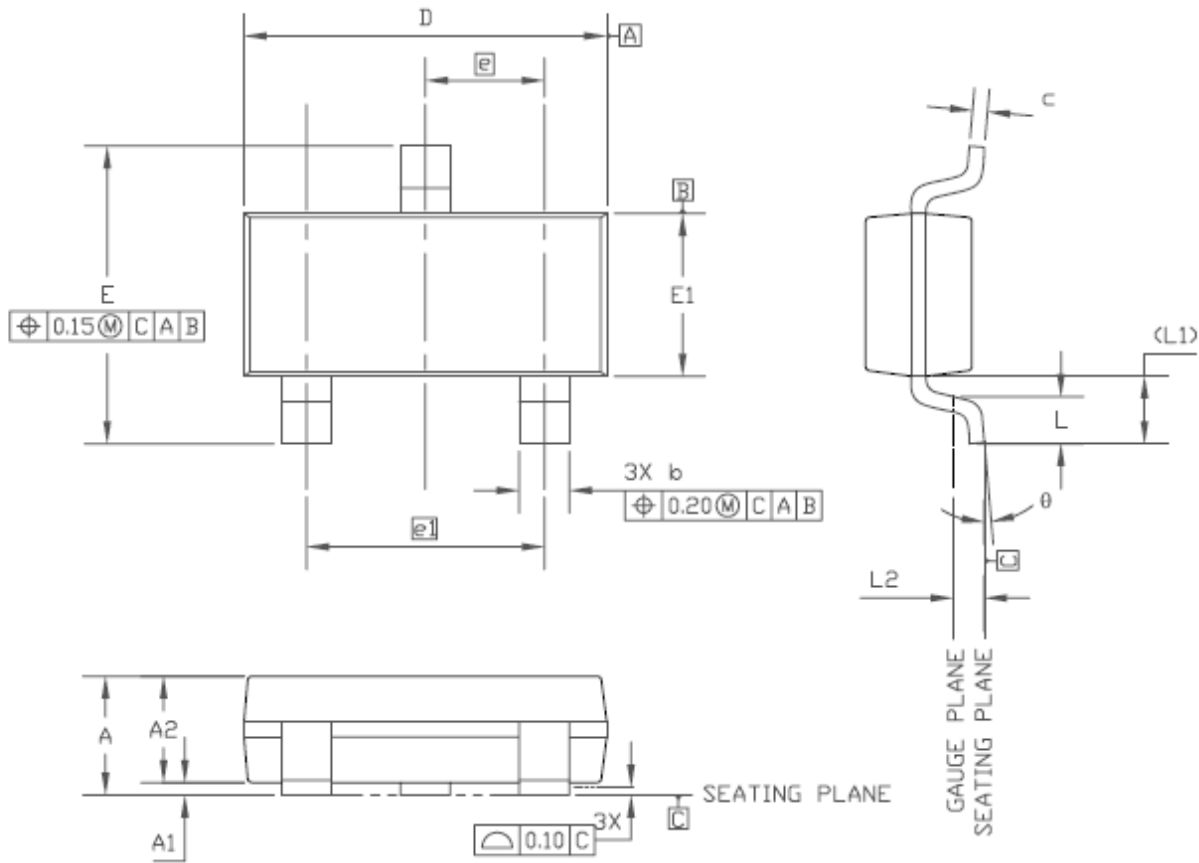
Diode Recovery Test Circuit & Waveforms



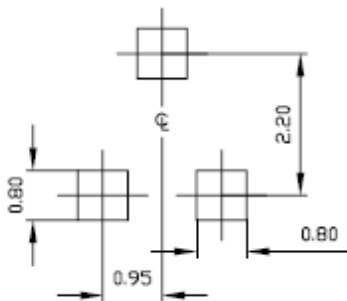


## Packaging Information

### SOT-23 STANDARD PACKAGE OUTLINE



#### RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°

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