DESCRIPTION

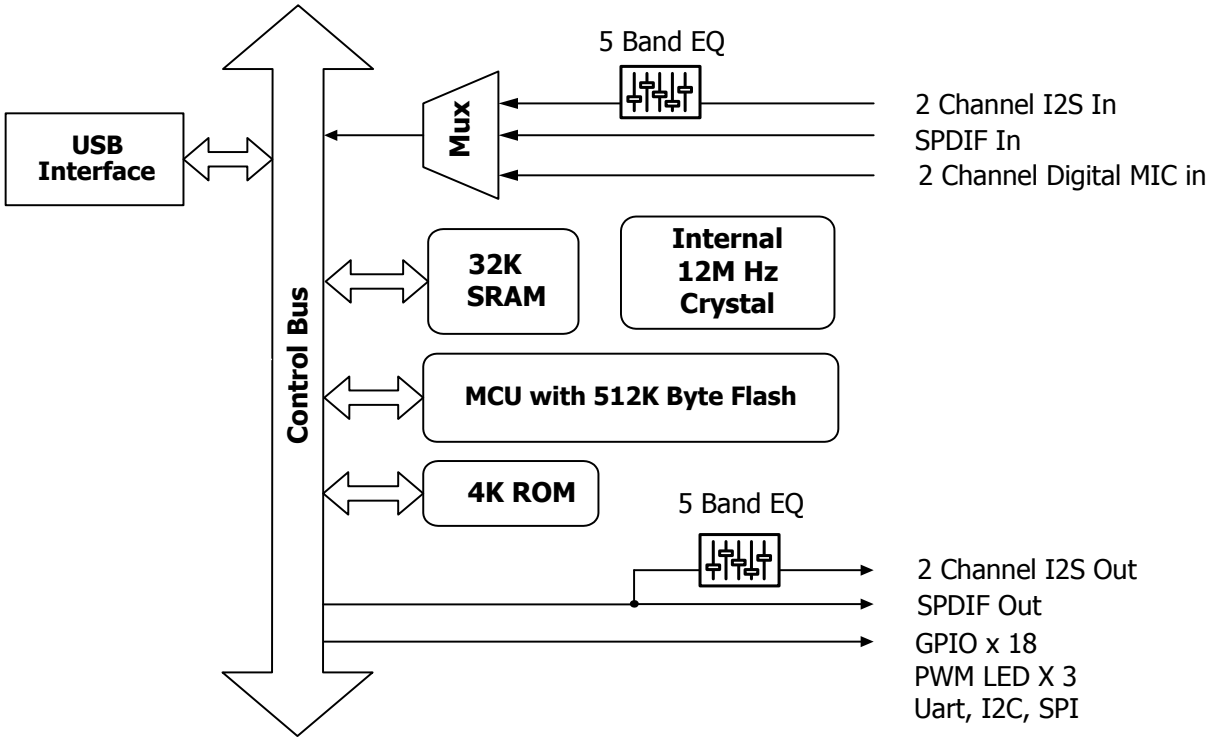
The CM6530N is a low power USB 2.0 audio controller builds in 8051 for flexible applications. Accompany with ultra low power codec makes it suitable for low power headset, notebook/mobile docking and microphone applications. The internal 8051 can also be developed to different applications, such as Android Phone Accessories with special functions, such as HID buttons or LED control. The CM6530N is compatible with USB Audio Class 1.0 and USB 2.0 full-speed, Thus it can plug and play without additional software installation on the major operation systems. The I2S support 8~96 KHz sampling rate and 16/24bits resolution.

The CM6530N also integrates 512K Byte flash (Including 32KB F/W programming size) and just requires few passive components to make a finish product. Thus it can save the total BOM cost and PCB area can be smaller.

FEATURES

- USB 2.0 full-speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.1 compliant
- Two (2) channel I2S for audio output interface
- Two (2) channel I2S for audio input interface
- Supports Digital Microphone Interface
- Built-in S/PDIF Input/output Interface
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers
- Embedded 1T 8051 with 32K Byte SRAM and 512K Byte Flash (Including 32K Byte F/W programming size)
- Integrated Tricolors PWM LED driver
- Master/Slave hardware I2C/SPI/UART control interface for external audio devices or FLASH access
- On chip watchdog timer
- Support crystal and crystal-less mode

BLOCK DIAGRAM



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Release notes

Revision	Date	Description
1.0	2016/12/15	First release.

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1 Description and overview

The CM6530N is a low power USB 2.0 audio controller builds in 8051 for flexible applications. Accompany with ultra low power codec makes it suitable for low power headset, notebook/mobile docking and microphone applications. The internal 8051 can also be developed to different applications, such as Android Phone accessories with special functions, such as HID buttons or LED control. The CM6530N is compatible with USB Audio Class 1.0 and USB 2.0 full-speed, Thus it can plug and play without additional software installation on the major operation systems. The I2S support 8~96 KHz sampling rate and 16/24bits resolution.

The CM6530N also integrates 512K Byte flash (Including 32KB F/W programming size) and just requires few passive components to make a finish product. Thus it can save the total BOM cost and PCB area can be smaller.

2 Features

2.1 USB compliance

- USB 2.0 full-speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.1 compliant
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers
- Support Synchronous and Asynchronous audio data synchronization

2.2 Integrated 8051 micro-processor

- Embedded 8051 micro-processor to handle the command/protocol transactions
- Embedded 512K Byte SPI Flash(Including 32KB F/W programming size)
- 32K Byte RAM for firmware extension and plug-in
- HID interrupts/buttons/functions can be implemented via firmware codes
- Provides maximum hardware configuration flexibility with firmware code upgrade
- VID/PID/Product String can be programmed by firmware

2.3 Control interface

- Master/Slave I2C control interface, bus speed supports 100 and 400kbit/s
- One 4-wire SPI mater / slave interface, bus speed supports from 150k to 12Mbit/s
- Twelve (12) GPIO pins and firmware programmable.
- JTAG debug interface
- GPIOs are configured as HID key and LED indicators
- Tri-color PWM LED Driver

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2.4 General

- CM6530N can auto detect and switch to crystal mode or none crystal mode. The power consumption for crystal mode is 8mA lower than non-crystal mode.
- Single 5V power supply (embedded 5V to 1.8V regulator for digital core, 5V to 3.3V regulator for digital IO, 5V to 3.6V regulator for analog codec)
- 3.3V digital I/O pads with 5V tolerance
- Industrial standard QFN-48 package (6.5mm x 5mm)

2.5 Audio I/O

- Playback Stream:
  - I2S interface
    - Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48/88.2/96KHz
    - Supported Bit Length: 16/24 bits
  - S/PDIF transmitter
    - Sample Rates: 44.1K/48K/88.2K/96KHz
    - Supported Bit Length: 16/24 bits
- Recording Stream:
    - I2S interface Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/96KHz
    - Supported Bit Length: 16/24 bits.
  - S/PDIF receiver
    - Sample Rates: 44.1K/48K/88.2K/96KHz
    - Supported Bit Length: 16/24 bits

**Note:

CM6530N is a USB 2.0 full-speed audio device. Since there is a bandwidth limitation, CM6530N cannot support 96 KHz/24bits for playback and capture streams simultaneously. The possible combinations are shown below:

	Playback	Capture
Audio Format	Stereo, 96KHz/24bits	Stereo, 48kHz/24bits or below
		Mono, 96KHz/24bits or below
	Stereo, 48kHz/24bits or below	Stereo, 96KHz/24bits
	Mono, 96KHz/24bits or below	

3 Applications

- Low power USB Headset
- Low power Notebook/Ultrabook Docking
- Low power Android Phone/Tablet Docking
- USB DAC, Headphone amplify
- Low power USB Microphone

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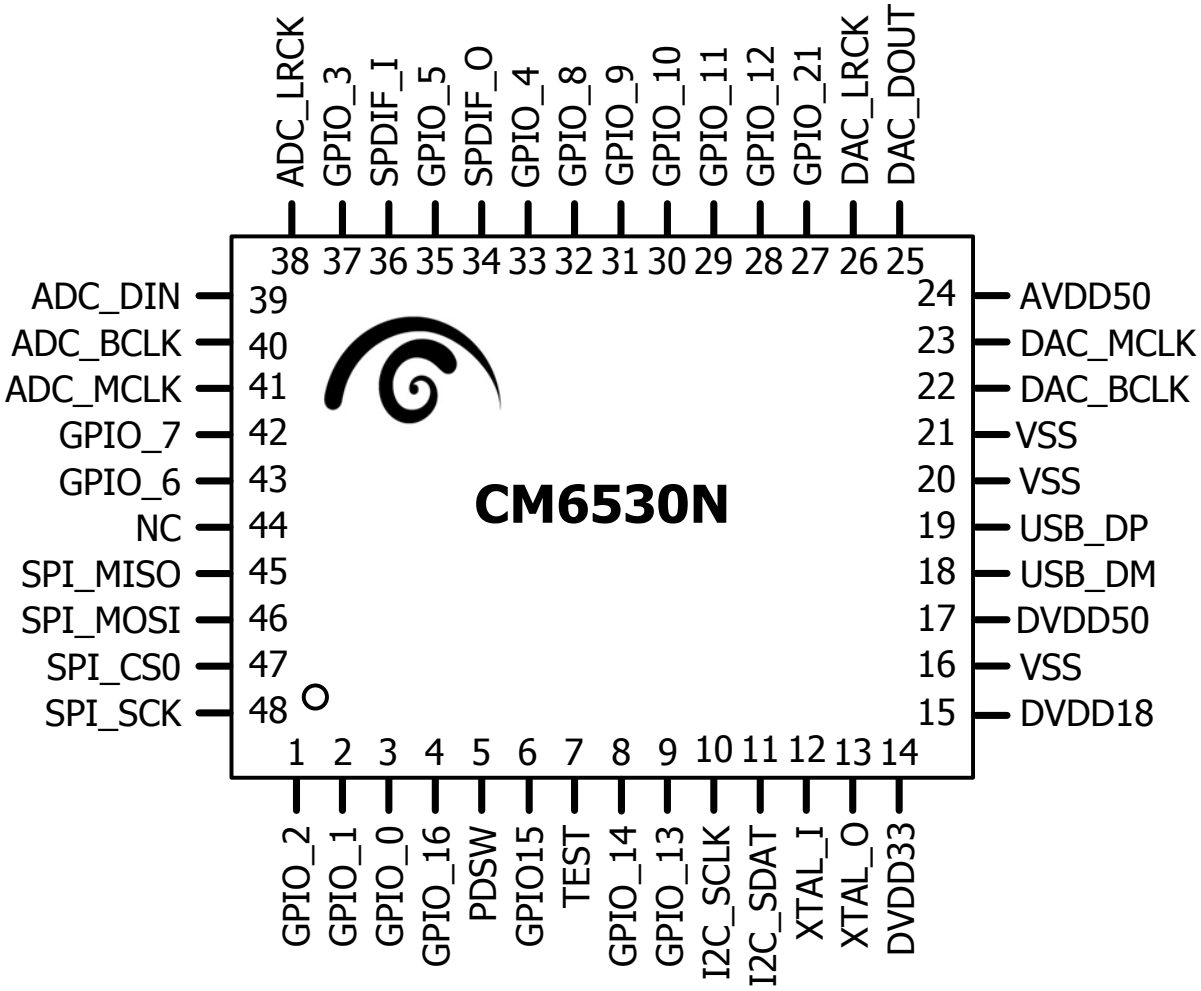
4 Pin assignment

4.1 CM6530N Pin-out diagram



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4.2 Pin description

Pin #	Symbol	I/O	Description
			Clock
13	XTAL_O	AO	12MHz crystal oscillator output
12	XTAL_I	AI	12MHz crystal oscillator input
			USB2.0 BUS Interface
19	USB_DP	AIO	USB 2.0 data plus (USB D+ signal)
18	USB_DM	AIO	USB 2.0 data minus (USB D- signal)
			Power/Ground
14	DVDD33	AO	Regulator 3.3V output, drive capacity 10mA
15	DVDD18	AO	Regulator 1.8V output, no current drive capacity
17	DVDD50	PWR	5V digital power for 5/3.3/1.8V regulator
24	AVDD50	PWR	5V analog power for 4.2/3.6V regulator
16	VSS	GND	Digital Ground
20	VSS	GND	Digital Ground
21	VSS	GND	Digital Ground
			Two (2)-channel I2S DAC Output Interface
23	DAC_MCLK	DIO	I2S out master clock Programmable 3.3V output buffer
22	DAC_BCLK	DIO	I2S out bit clock Programmable 3.3V bidirectional buffer Internal default pull-down
25	DAC_DOUT	DO	I2S out serial data output Programmable 3.3V output buffer
26	DAC_LRCK	DIO	I2S out left/right clock Programmable 3.3V bidirectional buffer Internal default pull-down
			Two (2)-channel I2S ADC Input Interface
38	ADC_ LRCK	DIO	I2S in left/right clock Programmable 3.3V bidirectional buffer Internal default pull-down
39	ADC_ DIN	DI	I2S in serial data input Programmable 3.3V input buffer, Schmitt trigger Internal default pull-down
40	ADC_ BCLK	DIO	I2S in bit clock Programmable 3.3V bidirectional buffer Internal default pull-down
41	ADC_ MCLK	DIO	I2S in master clock Programmable 3.3V output buffer
			S/PDIF I/O
34	SPDIF_O	DO	S/PDIF transmitter SPDIF_O is an output buffer with 8mA Tri-state
36	SPDIF_I	DI	S/PDIF Receiver SPDIF_O is an input buffer with 8mA Tri-state
			GPIO
3	GPIO_0	DIO	General purpose input/output (default Volume Up button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input (JTAG-TCK)

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2	GPIO_1	DIO	General purpose input/output (default Volume Down button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input (JTAG-TMS)	
1	GPIO_2	DIO	General purpose input/output (default Play Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input (JTAG-TDI)	
37	GPIO_3	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
33	GPIO_4	DIO	Programmable 2 in 1 I/O interface. GPIO/PWM select by firmware. General purpose input/output (default PWM LED Blue). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
35	GPIO_5	DIO	Programmable 2 in 1 I/O interface. GPIO/PWM select by firmware. General purpose input/output (default PWM LED Green). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
43	GPIO_6	DIO	Programmable 2 in 1 I/O interface. GPIO/PWM select by firmware. General purpose input/output (default PWM LED Red). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input (JTAG-TRST)	
42	GPIO_7	DIO	General purpose input/output (JTAG-TDO). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, default EQ disable and weak pull-up for input.	There are 4 kinds of preset EQ, GPIO7 and 8 are used to determine in which mode. The combinations are shown below. GPIO[8:7]=0,0: Normal mode GPIO[8:7]=0,1: Gaming mode GPIO[8:7]=1,0: Communication mode GPIO[8:7]=1,1: Movie mode EQ function can enable via configuration tool or firmware.
32	GPIO_8	DIO	General purpose input/output 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default EQ disable and weak pull-up for input.	
31	GPIO_9	DIO	General purpose input/output (default Rec Clip Indicator). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
30	GPIO_10	DIO	Programmable 3 in 1 I/O interface. GPIO/Digital MIC Clock (DMIC_CLK)/ UART_RX select by firmware. GPIO (Default MIC Jack Detect): 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
29	GPIO_11	DIO	Programmable 3 in 1 I/O interface. GPIO/Digital MIC Data (DMIC_DAT)/ UART_TX select by firmware. GPIO (Default Headphone Jack Detect): 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
28	GPIO_12	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
9	GPIO_13	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
8	GPIO_14	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	

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9	GPIO_15	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
4	GPIO_16	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
27	GPIO_21	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
4-Wire SPI Serial Bus			
45	SPI_MISO	DIO	SPI data master in/slave out, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, default weak pull-down for input.
46	SPI_MOSI	DIO	SPI data master out/slave in, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, default weak pull-down for input.
47	SPI_CS0	DIO	SPI chip select, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
48	SPI_SCK	DIO	SPI clock, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, default weak pull-down for input.
2-Wire Serial Bus (I2C)			
11	I2C_SDAT	DIO	2-wire serial data, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
10	I2C_SCLK	DIO	2-wire serial clock, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
Miscellaneous			
5	PDSW	DO	Power Down Switch is an output buffer with 8mA Tri-state output. Normal mode: 0 Suspend mode: 1
7	TEST	DI	The TEST pin is used for IC test, another one is in the instance when F/W crashes or USB was not recognized, set TEST pin to 3.3V before USB connect can force MCU into boot loader mode and be able to update F/W via configuration tool, default weak pull-down for input. 1: Boot loader mode 0 : Normal operation
44	NC	N.C.	No Connection.

**Note1: GPIOs, I2C, SPI, SPDIF, PDSW, NC, RESETN pins can be left floating if not in use.

**Note2: Suggest connect TEST pin to GND by default setting.

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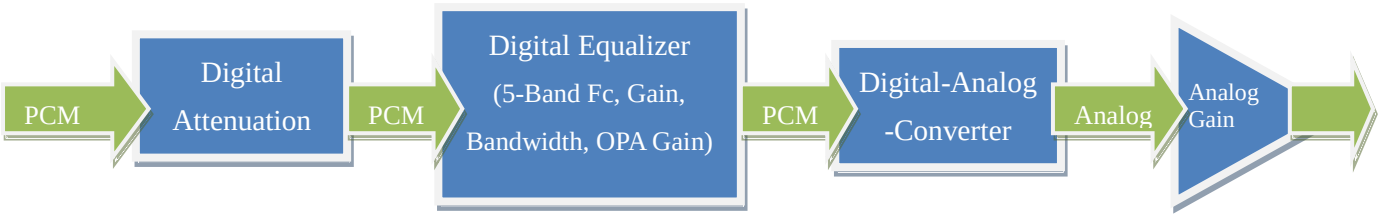
5 Function description

5.1 Playback Equalizer

5.1.1 5-band equalizer

CM6530N has integrated five (5)-band hardware digital equalizer (EQ) engine inside the chips to fulfill various application usages. It provides up to four (4)-preset modes on client's product design for different user scenarios including default/music, movies, gaming and communication modes. Clients could also change the gain parameters for each of the preset application EQ mode via embedded FLASH coding. Also, the EQ engine could also be utilized for compensating and fine-tuning the headphone driver for Sound Pressure Level (SPL) performance to a specific preference. In this case, clients could fully customize all EQ coefficients such as center frequency, gain values, and bandwidth to one optimized frequency response curve and setting in terms of the headphone driver and housing's acoustics characteristics, also via embedded FLASH programming.



The EQ engine contains five (5) frequency bands (Fc) of digital filters to conduct transfer functions of the frequency response over the audio band. It allows maximum +-12dB digital gain (Gain) for each band with 0.5dB adjustment per step. Each filter will have its bandwidth (BW) factor between 0 and 1.0.

Fc: Center Frequency, F1~F5, 20<Fc<20K (Hz)

Gain: Digital Frequency Gain, -12dB <= Gain <=+12dB, 0.5dB/step

BW: Filter Bandwidth Factor, 0<BW<1

OPA Gain: Analog Gain Compensation setting for each equalizer mode

The EQ engine already provides four (4)-preset modes/settings based on the same preset F1~F5 center frequencies and OPA gain:

F1 (Bass)= 100Hz

F2 = 350Hz

F3 = 1KHz

F4 = 3.5KHz

F5 (Treble) = 13KHz

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With the four (4)-preset EQ modes, clients could use embedded FLASH parameters to change the gain values for each band of the center frequency and hence customize the four (4)-preset EQ curves based on the preset center frequencies and bandwidth. Alternatively, clients could also skip the four (4) preset modes and create a customized EQ curve by changing the center frequencies, gain values and even the bandwidth factors in embedded FLASH parameters to make the headphone sound better or meet some frequency requirements. However, in this case, the product will always use one optimized EQ setting and could not allow users to dynamically change into different preset modes. Clients could also consider reporting Treble/Bass feature unit by embedded FLASH to Windows UAA driver to allow end-users to adjust Bass (F1) and Treble (F5) by themselves. Therefore there are three usage/application scenarios as shown by the summary table below:

3 EQ Usage/Application Scenarios

No	Scenario	Gain Value	Center Frequency / Bandwidth Factor	Number of Modes	User Control Type
1	**4 Switchable Presets**	Configurable	Fixed	4	Hardware
2	**Full-Customized EQ**	Configurable	Configurable	1	N.A.
3	**Treble/Bass Feature Unit**	Configurable	Configurable	1	Software

**Note: Hardware user control type means end-users could select which EQ mode they are going to use by a hardware switch/button on the product; software control means they could control the treble/bass gain values by GUI in Windows OS sound device advanced settings.

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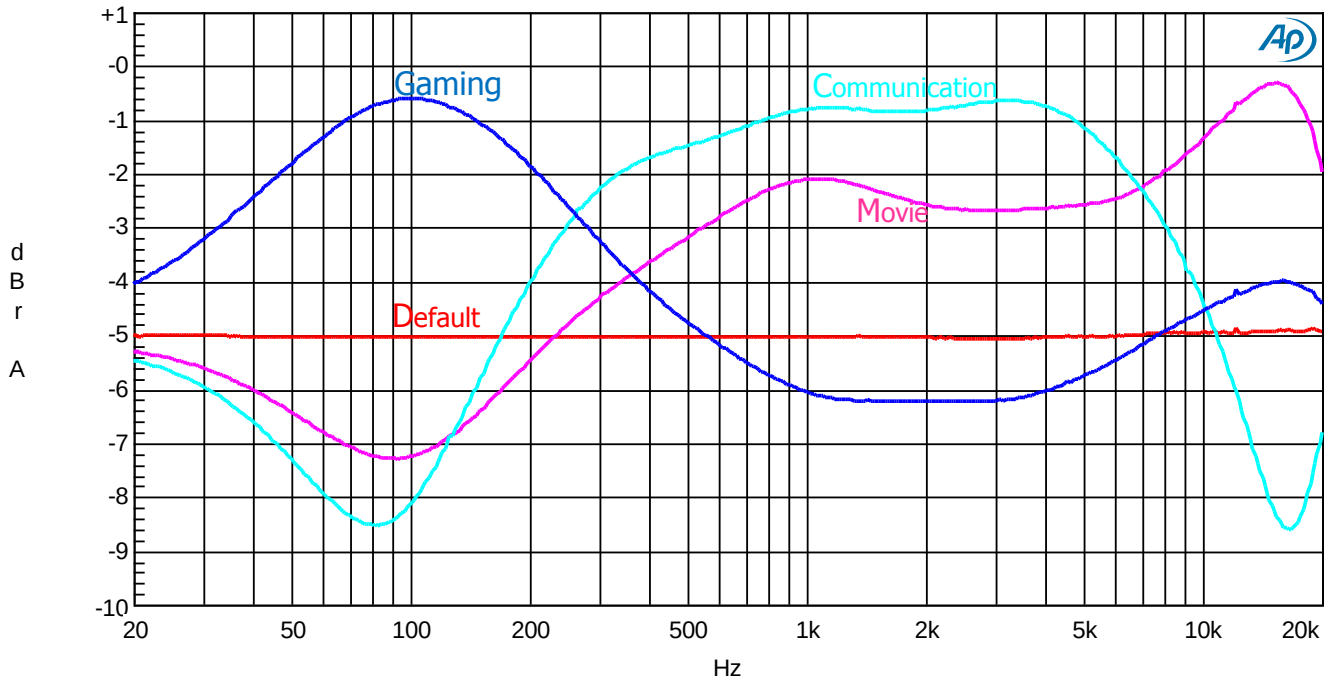
5.1.2 Four (4) Preset EQ Mode

As mentioned above, EQ engine already provides four (4)-preset EQ modes for different user scenarios/applications. The EQ function default was disable but it can enable via configuration tool or firmware, End users could use the hardware switch on the product (determined by 2 EQ configuration input pins) to dynamically change to different EQ modes. The following shows the frequency response of each mode.

Mode	GPIO8	GPIO7	Color
Default	0	0	----------
Gaming	0	1	----------
Communication	1	0	----------
Movie	1	1	----------

Audio Precision 04/20/11 15:35:35



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Ampl	Left	00
2	1	Magenta	Solid	2	Anlr.Ampl	Left	11
3	1	Cyan	Solid	2	Anlr.Ampl	Left	10
4	1	Blue	Solid	2	Anlr.Ampl	Left	

DA-EQ-SPDIF_In_DA_Out.at27

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5.2 Recording Equalizer

CM6530N also provide five (5)-band equalizer for the input. It can be used to compensate the frequency response of microphone unit. Clients could fully customize all EQ coefficients (center frequency, gain values, and bandwidth) through embedded FLASH.

5.3 HID function

5.3.1 HID interrupt in

Input Data Format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT (slave mode int)
	bit3: SPIM_INT (master mode int)
	bit2:I2CS_INT (slave mode int)
	bit1:I2CM_INT (master mode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

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5.3.2 HID get_input_report

Command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h A1	8'h 01 (Get_Report)	16'h 01 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

*Note: The Start_Addr value in the input reported is put in the Internal Register Address 0xff. Software must set the value of Start_Addr Register to make sure Get Input Report can read the proper data you want.

Input Data Format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6: UART_INT
	bit5: GPI_INT
	bit4: SPIS_INT(slave mode int)
	bit3: SPIM_INT(master mode int)
	bit2: I2CS_INT(slave mode int)
	bit1: I2CM_INT(master mode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

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5.3.3 HID set_output_report

Command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 21	8'h 09 (Set_Report)	16'h 02 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

*Note: Byte5 is the beginning address of this write sequence.

Output data format:

byte0	always 1 for org HID event report ID
byte1	start address of write reg (H-start_addr)
byte2	start address of write reg (L-start_addr)
byte3	effective write/read data length (<=12)
byte4	write data to [start_addr]
byte5	write data to [start_addr+1]
byte6	write data to [start_addr+2]
byte7	write data to [start_addr+3]
byte8	write data to [start_addr+4]
byte9	write data to [start_addr+5]
byte10	write data to [start_addr+6]
byte11	write data to [start_addr+7]
byte12	write data to [start_addr+8]
byte13	write data to [start_addr+9]
byte14	write data to [start_addr+10]
byte15	write data to [start_addr+11]

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5.4 Vendor command definition

5.4.1 Vender command read

Command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h C3	8'h 02 (Command 2)	16'h -- -- (Starting Address of input Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

Input data format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

5.4.2 Vender command write

Command format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 43	8'h 01 (Command 1)	16'h -- -- (Start Address of Output Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

Output data format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

5.4.3 USB vendor requests

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x43 (Vendor Other)	0x01 Register Write	Address	0x0000	Data Length (<=64 bytes)	Data
0xC3 (Vendor Other)	0x02 Register Read	Address	0x0000	Data Length (<=64 bytes)	Data
0x43 (Vendor Other)	0x03 Flash Write	Address	0x0000: Write only 0x0001: Auto Verify	Data Length (<=64 bytes)	Data
0xC3 (Vendor Other)	0x04 Flash Read	Address	0x0000	Data Length (<=64 bytes)	Data
0x43 (Vendor Other)	0x05 Flash Control	0x0000	0x0001: Chip Erase	0x0000	None
		Address	0x0002: Sector Erase		
0xC3 (Vendor Other)	0x06 Flash Control - Get Status	0x0000	0x0000	0x0001	1-byte data 0x01: Erasing 0x00: Ready

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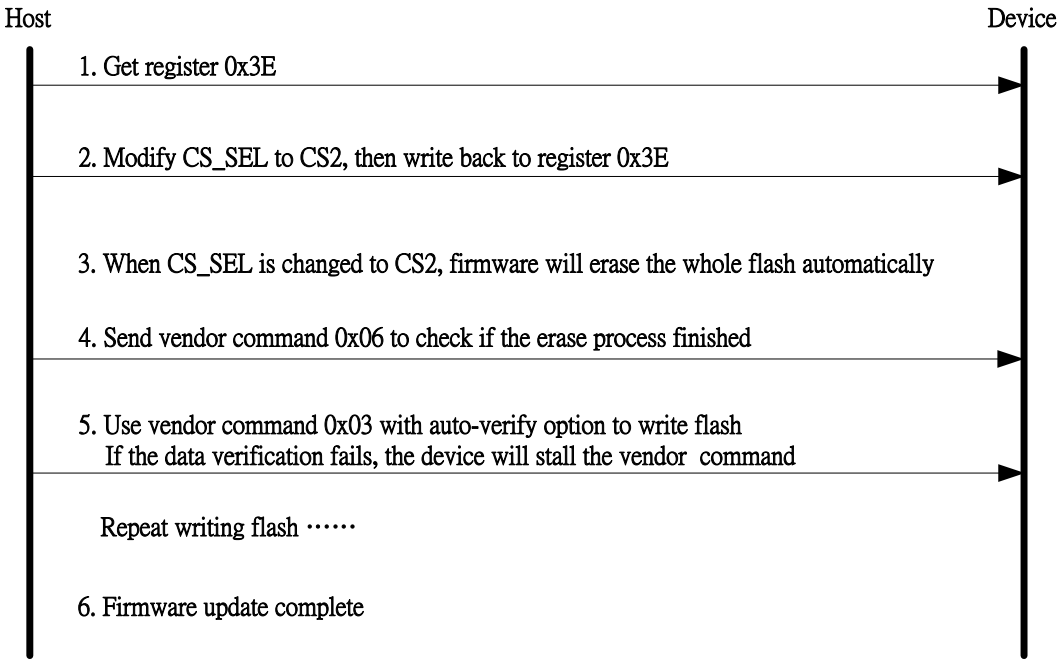
5.4.4 Simple process of firmware update



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5.5 I²S Control description

5.5.1 I²S Interface setting

I²S has three clock signals (MCLK, BCLK and LRCK) and at least one data line depending on the channels supported. One data line contains two channels. Therefore, there is one data line for a 2-channel I²S DAC controller. The three I²S clock symbols are explained below:

MCLK = main clock.
BCLK = bit clock.
LRCK = left and right clock.

5.5.2 Basic of I²S bus

Both master and slave modes of I²S are supported, namely I²S DAC, I²S ADC. Master mode means BCLK and LRCK are provided as shown in the left diagram below. On the contrary, slave mode means BCLK and LRCK are provided by the I²S codecs as shown in the right diagram below.

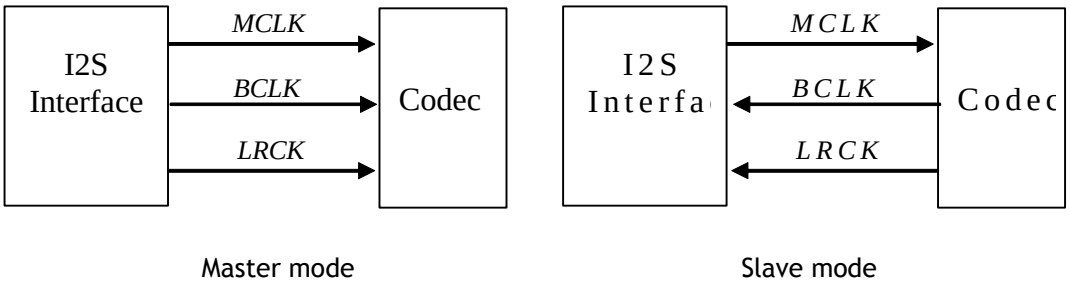

Figure -1 I2S Master/Slave Block Diagram

Below figure illustrates the basic waveform of I²S. Note that BCLK is generated at the positive edges of MCLK with the ratios 1, 1/2, 1/4, or 1/8, and LRCK is generated at the negative edges of BCLK with the ratios 1/64, 1/128, 1/256. Data lines are transmitted at the negative edges of BCLK, and are sampled at the positive edges of BCLK by codecs in case of playback or recording.

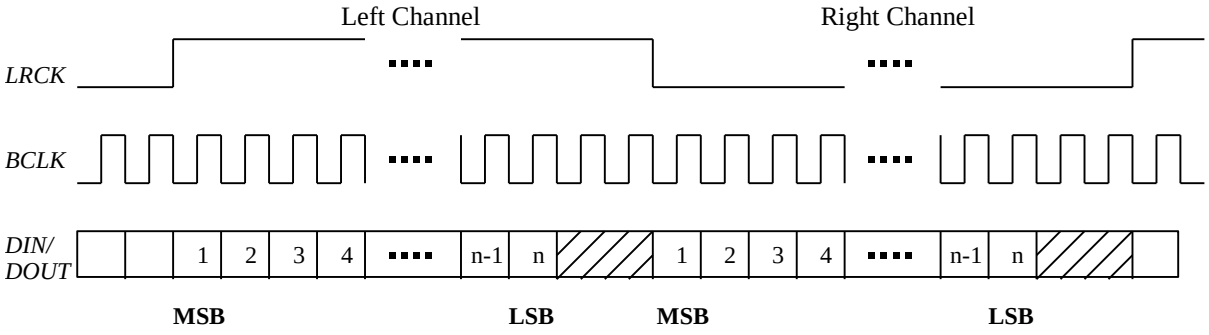

Figure -2 I²S Timing Diagram

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For the I²S DAC controller, the audio data is transformed from the parallel format to the serial format before being transmitted. Then, the bit data is shifted out one by one with the MSB first via DOUT signal. If the I²S DAC controller is set to 32 bits, at least 32 BCLK clocks must exist in both LRCK left and right channels. In the same manner, the audio data is transformed from serial format to the parallel format for the I²S ADC controller.

5.5.3 Left justified mode

In the left justified mode of the I²S DAC controller, the MSB data bit is clocked out at the negative edge of BCLK which is aligned to the transition of LRCK. In the left justified mode of I²S ADC controllers, the MSB data bit is clocked out by codecs and sampled at the first positive edge of BCLK which follows a LRCK transition. LRCK is high during left channel transmission and low during right channel transmission in the left justified mode.

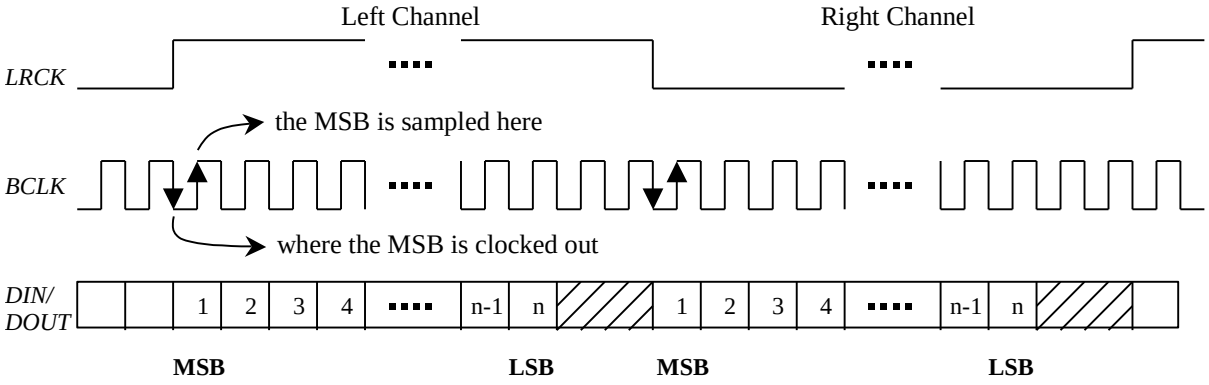

Figure -3 Left Justified Mode Timing Diagram of I²S

5.5.4 I²S Mode

In the I²S mode of the I²S DAC controller, the MSB data bit is clocked out by CM6530N at the first negative edge of BCLK which follows a LRCK transition. In the same manner, the MSB data bit is clocked out by codecs and sampled at the second positive edge of BCLK which follows a LRCK transition. LRCK is low during left channel transmission and high during right channel transmission in the I²S mode.

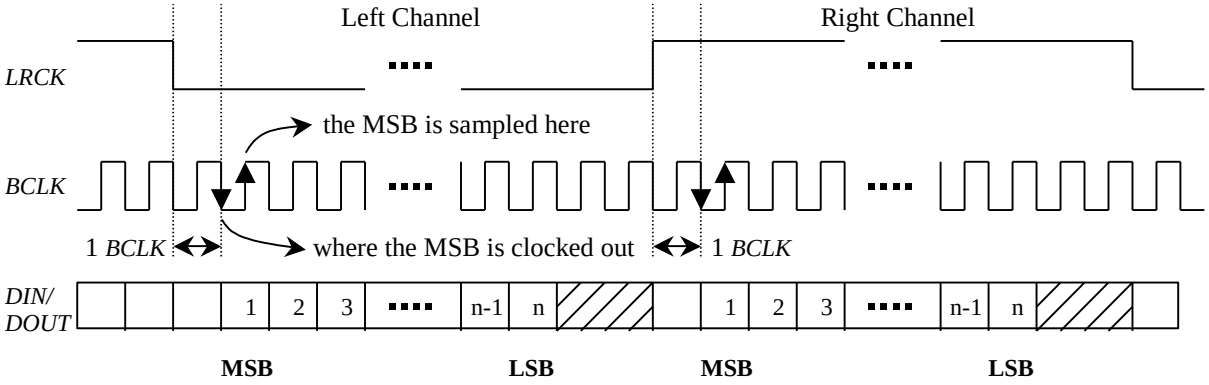

Figure -4 I²S Mode Timing Diagram of I²S

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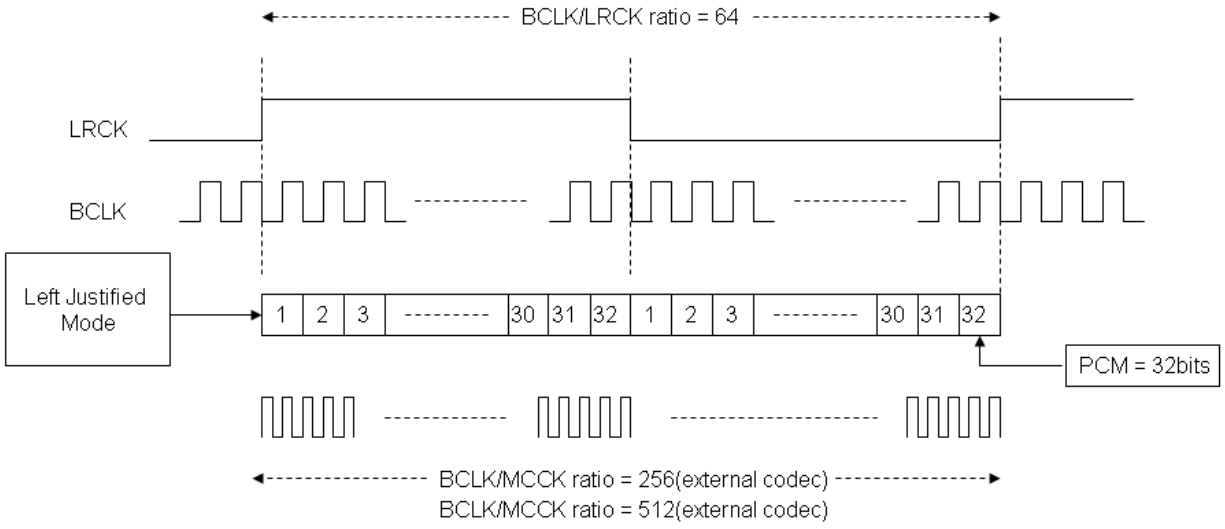
5.5.5 I²S MCLK/BCLK/LRCK ratio and format for CM6530N

I2S clock format					
	Sampling Freq.	Resolution	Format	BCLK/LRCK	MCLK/LRCK
Master Mode	8/11.025/16/ 22.5/32/44.1/48	16/24 bits	Left Justified / I2S-Mode	64	256/512
	88.2/96	16/24 bits	Left Justified / I2S-Mode	64	256
Slave Mode MCLK from CM6530N	8/11.025/16/ 22.5/32/44.1/48	16/24 bits	Left Justified / I2S-Mode	64	256/512
	88.2/96	16/24 bits	Left Justified / I2S-Mode	64	256
Slave Mode MCLK from external	8/11.025/16/ 22.5/32/44.1/48 /88.2/96	16/24 bits	Left Justified / I2S-Mode	64	128/256/512



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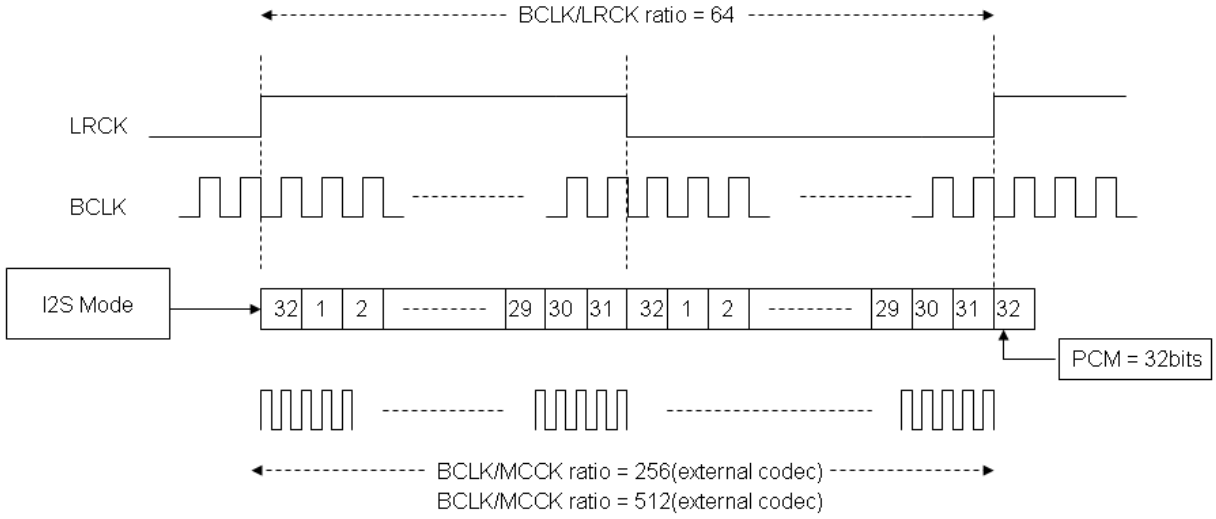

5.5.6 I2S output enable setting and data stream path

Pin-Out-En	Ext-I2S-master	Ext-I2S-slave with mclk-out	Ext-I2S-slave with mclk-in	Int-I2S-master	Int-I2S-master with DSP
	Codec_sel=1	Codec_sel=1	Codec_sel=1	Codec_sel=2	Codec_sel=3
ADCMK_EXT	0	0	1	0	0
ADC_MKEN	1	1	0	0	1
ADC_BLKEN	1	0	0	0	1
ADC_DSPEN	0	0	0	0	1
DACMK_EXT	0	0	1	0	0
DAC_MKEN	1	1	0	0	1
DAC_BLKEN	1	0	0	0	1
DAC_DOEN	1	1	1	0	1

5.5.7 Slave Mode Playback and Record

CM6530N supports slave mode playback and record. In slave mode record, CM6530N use external LRCR and BCLK clock to latch ADC DIN and has one register to determine to use internal MCLK or external MCLK. Because of using external MCLK, PLL adjustment circuit can't increase or decrease ADC clock rate to prevent FIFO from empty or full. In slave record, we will declare the ISO-IN endpoint as asynchronous type. Host will not receive data with uniform length but depend on what record device receiving.

In slave mode playback, we still can't control the DAC clock rate if MCLK comes from external. In this mode, we will declare ISO-OUT endpoint as asynchronous type and declare one feedback endpoint. When feedback endpoint support, the host will adjust sending package length by the content of feedback. Using the feedback operation, we can prevent FIFO running full or empty.

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5.6 SPDIF control description

5.6.1 SPDIF frame description

- Audio format: linear 16 bit default.
- Allowed sampling frequencies (Fs) of the audio:
  - 96 kHz from DVD
  - 88.2kHz from DVD
  - 48 kHz from DAT
  - 44.1 kHz from CD
- One way communication: from transmitter to receiver.
- Control information:
  - V (validity) bit: indicates if audio sample is valid.
  - U (user) bit: user free coding i.e. running time song, track number.
  - C (channel status) bit: emphasis, sampling rate and copy permit.
  - P (parity) bit: error detection bit to check for good reception.
- Coding format: bi-phase mark except the headers (preambles), for sync purposes.
- Bandwidth occupation: 100 kHz up to 6 MHz (no DC!)
- Signal bitrate as following table:

Sampling Rate (KHz)	SPDIF Bit Rate (MHz, 64*Fs)
96	6.144
88.2	5.6448
48	3.072
44.1	2.8224

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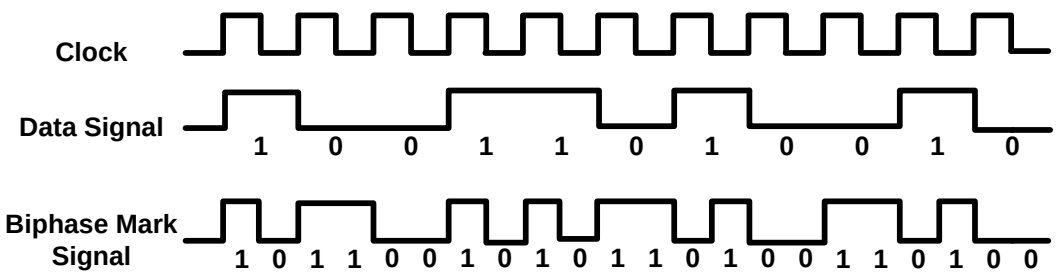


Figure -17 Bi-phase Mark Signal of SPDIF

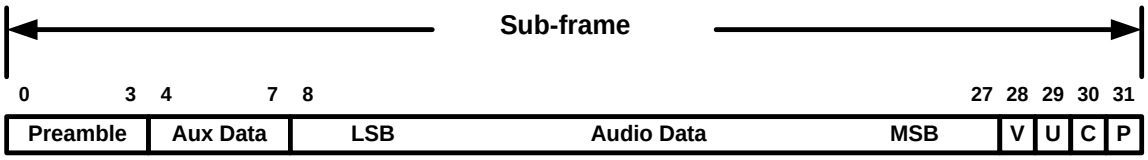
Preamble	cell-order (last cell "0")	cell-order (last cell "1")
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

Preamble B:
Marks a word containing data for channel A (left) at the start of the data-block.

Preamble M:
Marks a word with data for channel A that isn't at the start of the data-block.

Preamble W:
Marks a word containing data for channel B (right, for stereo). When using more than 2 channels, this could also be any other channel (except for A).

The number of sub-frames that will be used will depend on the number of channels that is being transmitted. A CD-player uses Channels A and B (left/right) and so each frame contains two sub-frames. A block contains 192 frames and starts with a preamble "B":



V: Valid, U: User-Data, C:Channel-Status-Data, P:Parity-Bit

Figure -5 SPDIF Subframe Description

In each block, 384 bits of channel status and subcode info are transmitted. The Channel-status bits are equal for both sub-frames, so actually only 192 useful bits are transmitted:

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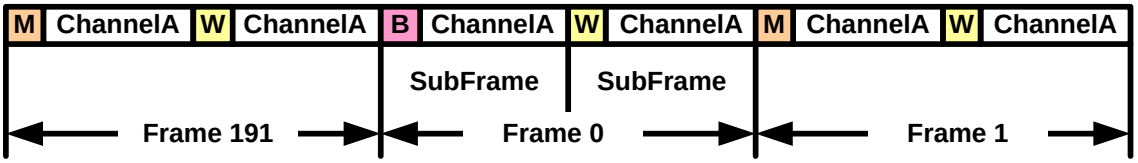

Figure -6 Preamble Description of 192 SPDIF frame

5.6.2 SPDIF out channel status

	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
byte0	**consumer /professional**	**audio/ non-audio**	**copyright**	**pre-emphasis**			**mode**	
default	0(P)	0(P)	1(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte1	**category code**							**L**
default	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)
byte2	**source number**				**channel number**			
default	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte3	**sampling frequency**				**clock accuracy**		**reserved**	
default	0(P)	0(P)	0(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)

**note: P: these bits can be programmed by USB HID or USB vendor command

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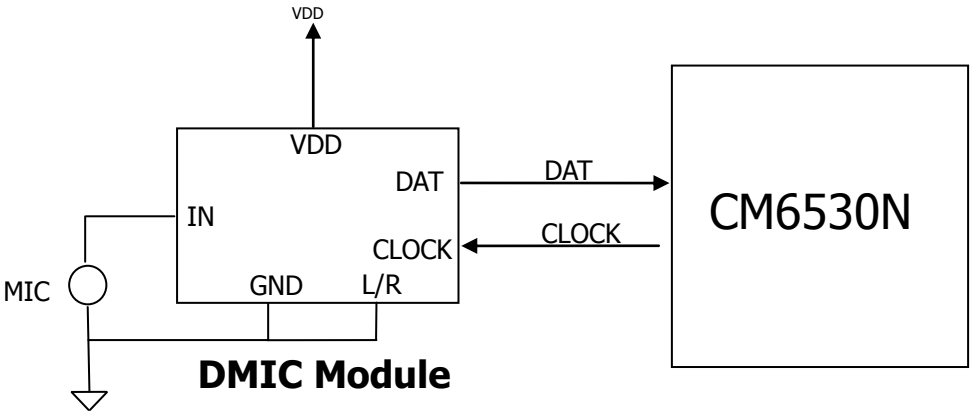
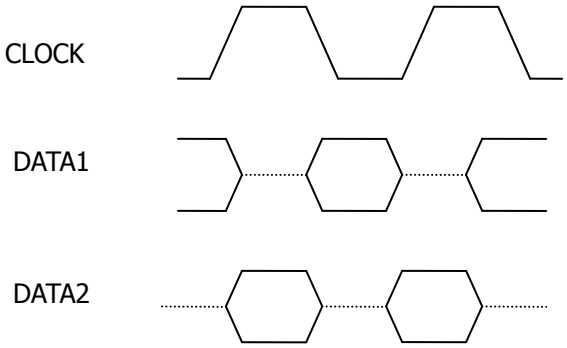
5.7 Digital microphone

CM6530N provide digital microphone interface for recording. There are two microphone signals transmitted on a single DATA line from DMIC module. The oversampling bit stream output from DMIC module connects to internal decimation filter to generate PCM output.





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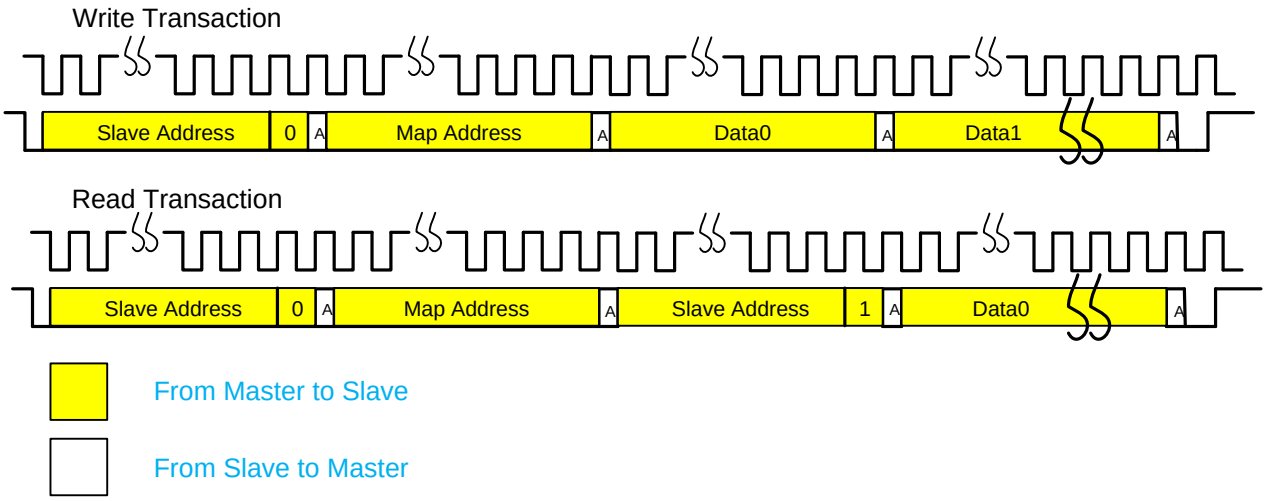
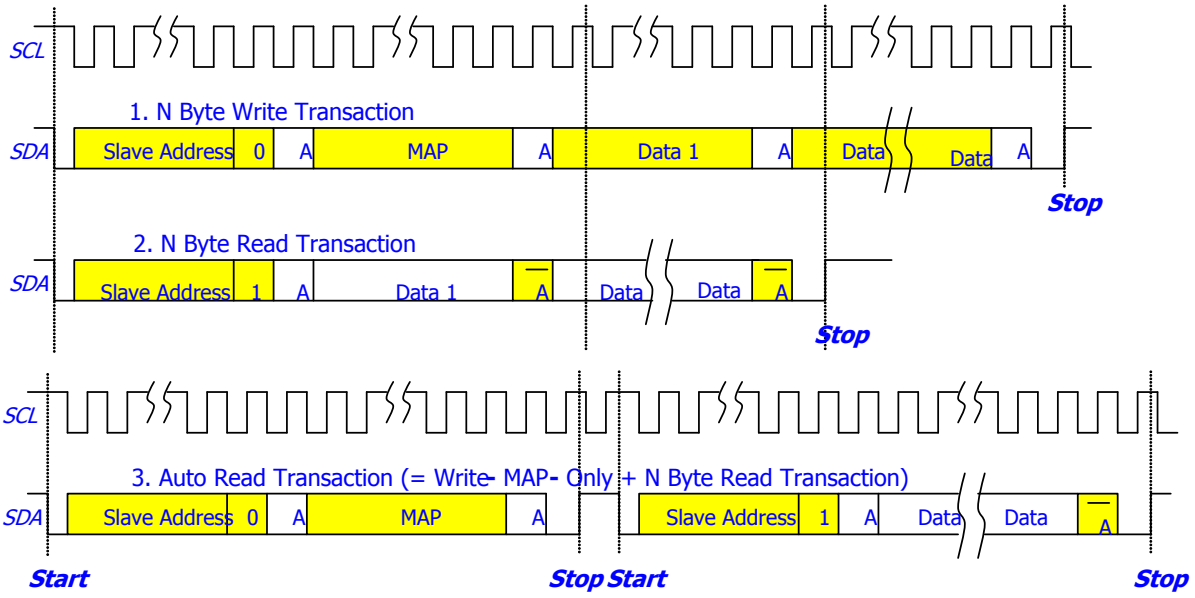
5.8 I²C interface

5.8.1 I²C master mode

I²C protocol timing





from master to slave

from slave to master

$A =$ acknowledge (SDA Low)

$\overline{A} =$ not acknowledge (SDA High)

MAP: Memory Address Pointer
(the target register address
in slave device)

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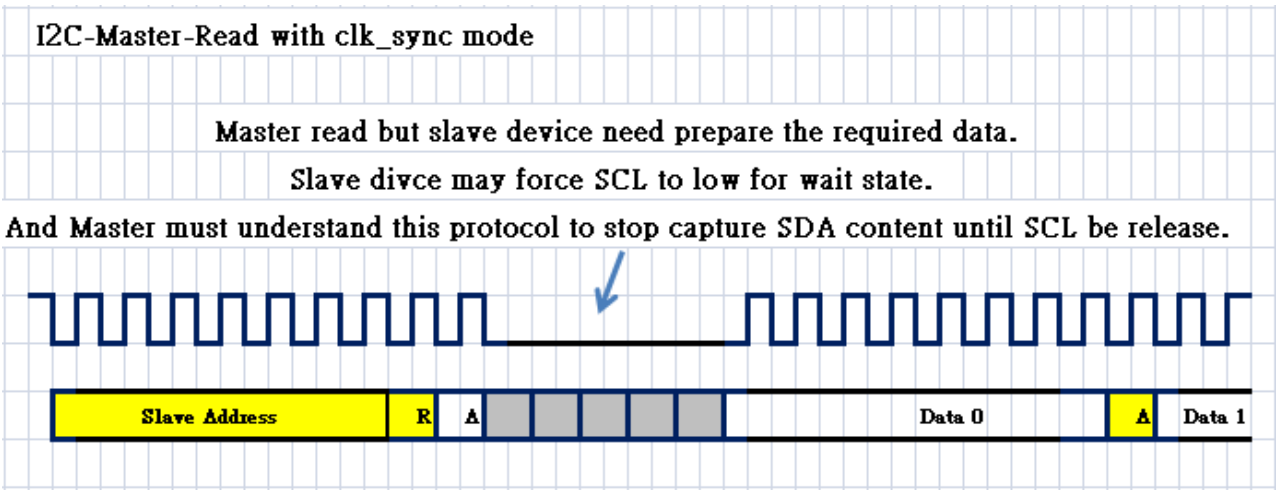
5.8.2 I2C-master read with clk_sync mode



5.8.3 I²C master device address and control register

Address: 0x80

Bits	R/W	Bit Mnemonic	Description	Default
7-1	R/W	SA_reg	The target slave device address.	0xA8 (POR)
0	R/W	SA_reg	1: read, 0: write	1'b0 (POR)

5.8.4 I²C master memory address pointer (map) register

Address: 0x81

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP_reg	The register low byte address of salve device to be read or written.	8'b0 (POR)

5.8.5 I²C master memory address pointer (map2) register

Address: 0x82

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP2_reg	The register high byte address of salve device to be read or written.	8'b0 (POR)

5.8.6 I²C master data register

Address: 0x83 ~ 0x92

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	data0~ data15	The data read from or written to the slave device.	8'b0 (POR)

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5.8.7 I²C Master Control and Status Register 0

Address: 0x93

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	i2c_ctrl_reg1	Data length of read/write command 8'h1: 1 byte, minimum length 8'h2: 2 bytes … 8'hFE: 254 bytes 8'hFF: 256 bytes, maximum length	0x14 (POR)

5.8.8 I²C master control and status register 1

Address: 0x94

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	i2c_start	Trigger I²C read/write command 0->1: trigger I²C read/write command. 1->0: I²C interface had completed current task. 0 : I²C interface is idle and ready for work. 1 : I²C interface is running.	1'b0 (POR)
6	R/W	i2c_reset	Reset I²C interface 0 : Not reset I²C interface 1 : Reset I²C interface	1'b0 (POR)
5	R/W	map_len	MAP length 0 : 8-bit MAP 1 : 16-bit MAP	1'b0 (POR)
4	R/W	clk_sync	Clock Synchronization 0: off 1: on, when slave pull-down SCLK, master would pause	1'b1 (POR)
3	R/W	fast_std	I²C speed mode 0 : Standard mode, 100kHz 1 : Fast mode, 400kHz	1'b0 (POR)
2	R/W	map_only	MAP only write command 0 : Write command. 1 : MAP only write command.	1'b0 (POR)
1	R/W	auto_rd	Auto read command 0 : Read command. 1 : Auto read command.	1'b1 (POR)
0	R	i2c_ctrl_reg2	Slave NACK error occur 1 : No error 2 : Slave NACK error occur	1'b0 (POR)

*Note: Write-MAP-Only: An operation which only writes the register MAP the salve device

5.8.9 I²C master download control and status register

Address: 0x95

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	I2c_mas_sel	I2C master/slave select	1'b1 (POR)
6	RO WO	Flag_8byte Flag_ready	Flag_8byte (RO): Flag to status I2C is transmitting at 1st 8 bytes data or 2nd	1'b0 (POR)

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			8 bytes data. If the flag index it's transmitting the 2nd 8 bytes data, then F/W can prepare the next 8 bytes data into 1st 8byte buffer. Flag_ready (WO): Flag to index F/W has prepared next data ready. After prepare done, F/W need set this bit to index the data had been written. If F/W didn't catch on when all data has been transmitted, the I2C clock would be keep low to till it ready.	
5:4	R/W	LD_BLOCK	Download to which block of SRAM. 00: Load to 1st 8KB block. 01: Load to 2nd 8KB block. 10: Load to 3rd 8KB block. 11: Load to 4th 8KB block.	2'b00 (POR)
3	RO	CHKSUM_ERR	Check sum Error 1. If in LD_PHASE, the check sum value was calculated by I2C load data. 2. If in CHK_PHASE, the check sum value was calculated by SRAM read content.	1'b0
2	RO	CHK_FINISH	CHECK phase done 1: finish download data CHECK	1'b0
1	R/W	CHK_PHASE	MCU select CHECK phase to read SRAM data for check-sum check. 1: enable (after disable LD_PHASE) 0: set 0 after complete	1'b0 (POR)
0	R/W	LD_PHASE	MCU select LOAD phase to access SRAM from download. 1: enable 0: set 0 after complete	1'b0 (POR)

5.8.10 I2C master clock period setting register

Address: 0x96

Bits	R/W	Bit Mnemonic	Description	Default
7	W	CHG_ENABLE	MCU can program I2C clock; 1'b1: enable	1'b0 (POR)
6	R/W	LD_SEL	MCU download select 1'b0 : SPI download 1'b1 : I2C download	1'b0 (POR)
5-0	W	CHG_FREQ	Set I2C-master clock period. The clock period=83.3*5*(CHG_FREQ+1) Ex: CHG_FREQ = 6'd48 I2C Clock Period=83.3*5*(48+1)=20408ns HW limitation CHG_FREQ >= 6'h3	6'h0 (POR)

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5.8.11 I²C slave mode

"7-bit slave address = 7'b0001000 to 7'b0001011"

CM6530N can serves as a slave device with bit rate up to 400Kbps (fast mode). External MCU can write data to CM6530N or read data from CM6530N (No Size limitation in I²C Interface). Since host side and MCU can both access to all the internal registers.

CM6530N will transfer an interrupt to internal MCU until the INT bit of I²C control register has been cleaned by internal MCU. The interrupt will be trigger when write transaction is done or detect read-slave-address.

The main usage of 2-wire slave bus is to become the interface between the CM6530N and an external micro control unit (EMCU).

5.8.12 I²C slave data register

Address: 30~33h

Bits	R/W	Bit Mnemonic	Description	Default
31:0	R/W	MCU_data0~F	The data received from or transmitted to master device. This register cannot be written when 2-wire slave serial bus status is busy.	0000h (POR)

5.8.13 I²C slave status register

Address: 34~35h

Bits	R/W	Bit Mnemonic	Description	Default
15			Reserved	1b
14:12	R		Reserved	0h
11	R/W	Thld_int_mask	Threshold interrupt mask: 1: mask; 0: non-mask ; default :0	0b (POR)
10	R	Write_data_ready	Interrupt happened, auto-cleared after read	0b (POR)
9	R/W	I2c_s_reset	0: 2-wire serial bus in normal operation (default) 1: 2-wire serial bus in reset state	0b (POR)
8	R/W	Dri_tran_st	**Initiated transaction status** 1: The last initiated transaction failed, write 1 to clear.	0b (POR)
7	R/W	Rd_tran_st	**Read transaction status** 1: a new read transaction received, write 1 to clear.	0b (POR)
6	R/W	Wr_tran_st	**Write transaction status** 1: a new write transaction received, write 1 to clear.	0b (POR)
5:1	R	Data_len	The data length of the last write transaction received, 00000: 1 byte (MAP only) 00001: 2 byte (MAP + 1 byte data) 00010: 3 byte (MAP + 2 byte data) 00011: 4 byte (MAP + 3 byte data) 00100: 5 byte (MAP + 4 byte data) … 01111: 16 byte (MAP + 15 byte data) 10000: 17 byte (MAP + 16 byte data) Others: Reserved	0b (POR)
0	R	busy	The 2-wire serial bus status, 0: idle, 1: busy	0b (POR)

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**Note: When I²C issue interrupt to MCU, MCU needs to read the data numbers that threshold data count specified. And waits another interrupt until the total data transfer completed.

5.8.14 I²C slave memory address pointer (map) register

Address: 36h

Bits	R/W	Bit Mnemonic	Description	Default
7:0	R/W	MCU_MAP	The memory addresses of the read or write transactions from MCU. Address 0 is reserved for initiated transaction.	00h (POR)

5.8.15 I²C slave status register

Address: 37h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	Sync_en	**Synchronization Enable** 1: enable (the synchronization selection bit will decide the method adopted). 0: disable (MCU and ARC should guarantee no data lost themselves).	1b (POR)
6	R/W	Int_polarity	The polarity control of pin INT_OUT (initiated transaction interrupt), 0: high active, 1: low active	0b (POR)
5:4	R/W	Slave_addr	Slave Device Address 00: select 0001000 (10h) as slave address 01: select 0001001 (12h) as slave address 10: select 0001010 (14h) as slave address 11: select 0001011 (16h) as slave address	01b (POR)
3	R/W	Sync_sel	**Synchronization Method Selection** 1: Data synchronization. When this bit is one, if the current transaction has not been serviced by ARC, the clock line of the 2-wire serial bus will be pulled low. Under this situation, the MCU cannot start a new transaction or continue the current read transaction until the clock line goes back to high. 0: Ready pin synchronization. If the MCU cannot support open drain 2-wire serial bus, this bit should be set to zero. In this instance, the MCU cannot start a new transaction or continue the current read transaction until the pin XSLAVE_RDY goes high to signal that the driver has serviced the current transaction. Driver should use “driver acknowledge” to signal the processing of the current transaction is completed.	1b (POR)
2	R/W	Int_mask	**Interrupt Mask** 0: interrupt will happen at a read/write transaction received or a driver initiated transaction failed 1: interrupt will not happen	0b (POR)
1	R/W	Dri_init_tran	**Driver initiated transaction** Write 1 to start Driver initiated transaction. This bit is cleared automatically, after ARC initiated transaction starts. The ARC initiated transaction should be issued only when the 2-wire slave serial bus is idle. Otherwise, it will be ignored. The ARC initiated transaction will cause pin INT_OUT to send out an interrupt for MCU. After MCU responded with a Write-MAP-Address-0-Only transaction and a subsequent read transaction, interrupt	0b (POR)

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			INT_OUT will be de-asserted. However, if the MCU does not act as what is expected (a write MAP-Address-0-Only transaction and a subsequent read transaction), the interrupt INT_OUT will be still de-asserted, but the ARC initiated transaction status is used to signal a fail status to ARC. In this case, the driver should consider to repeat the failed Driver initiated transaction again.	
0	R/W	ack	Driver Acknowledge means driver has processed the current transaction. Write 1 to acknowledge. This bit will be cleared automatically.	0b (POR)

I2C example for Master mode:

Write 2 bytes:

(Slave address = 92, MAP address = 01, Data = 55, AA)

Write 0x80 = 92 (Slave address)

Write 0x81 = 01 (MAP address)

Write 0x83~0x84 = 55 AA (Data register)

Write 0x93 = 02 (Data length 2 bytes)

Write 0x94 = 92 (I2C start)

Read 2 bytes:

(Slave address = 92, MAP address = 01)

Write 0x80 = 93 (Slave address)

Write 0x81 = 01 (MAP address)

Write 0x93 = 02 (Data length 2 bytes)

Write 0x94 = 92 (I2C start)

Read 0x83~0x84 (Data register)

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5.9 SPI interface

The SPI interface is used to transfer control data between the CM6530N and external codec.

In a SPI interface there is only one central clock source producing a reference clock to which SPI data processing is synchronized. This clock is often referred to as the MCU clock, e.g. for SPI clock 12 Mhz, when the MCU clock is equal to 48Mhz and SPI clock div4.

Example	MCU CLK 0xB5[2:0]	48M(3'b100)	24M(3'b011)	12M(3'b010)	6M(3'b001)	3M(3'b000)
SPI clock 0x3D[4:3]=00(div4)	SPI CLK	12M	6M	3M	1.5M	750k
SPI clock 0x3D[4:3]=01(div12)	SPI CLK	4M	2M	1M	500k	250k
SPI clock 0x3D[4:3]=10(div16)	SPI CLK	3M	1.5M	769k	375k	187.5k
SPI clock 0x3D[4:3]=11(div20)	SPI CLK	2.4M	1.2M	625k	300k	150k

5.9.1 SPI Registers Descriptions

Address: 38~3bh

Bits	R/W	Bit Mnemonic	Description	default
31-0	R/W	Data0~Data3	The data (which include address, r/w, and data bits) written to or read from the codec. The bits in this register should be interpreted according to the individual codec. The content of this register, after a write operation completes, has no meaning. The content of this register, after a read operation completes, should reference the document of individual codec to see how many bits in this register is valid.	0x0000 0000 (POR)

5.9.2 SPI Control Register 0

Address: 3ch

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	slv_mst	SPI master/slave mode 0: master mode 1: slave mode	1'b1 (POR)
6	R/W	long_mode	SPI slave address length 0: 1-byte address 1: 2-byte address	1'b1 (POR)
5	--	--	Reserved	1'b0 (POR)
4	--	--	Reserved	1'b0 (POR)
3	R/W	si_mode	Serial interface mode 0: normal SPI mode 1: Serial interface mode	1'b0 (POR)
2	R/W	si_mode_rs	Serial interface RS/A0 output 0: RS/A0==0 for 8th bit 1: RS/A0==1 for 8th bit	1'b0 (POR)
1	RO	flag_rd	Flag read 0: mcu can't read spi data 1:mcu need to read spi data	1'b0
0	RO	flag_wr	Flag write	1'b0

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			0: mcu can't write spi data 1:mcu need to write spi data	

5.9.3 SPI control register 1

Address: 3dh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	spi_start	Trigger SPI read/write command 0->1: trigger SPI read/write command 1->0: SPI interface had completed current task 0 : SPI interface is idle and ready for work 1 : SPI interface is running	1'b0 (POR)
6	R/W	spi_lh_edge	SPI CEN control 0: codec latch control data at SPI clock low (default) 1: codec latch control data at SPI clock high	1'b1 (POR)
5	R/W	Spi_flash_rd_wr	SPI Flash Read/Write 0:spi flash read (default) 1:spi flash write	1'b0 (POR)
4-3	R/W	frq_sel	SPI clock period 2'b00: by MCU clk div 4 2'b01: by MCU clk div 12 2'b10: by MCU clk div 16 2'b11: by MCU clk div 20	2'b0 (POR)
2	R/W	first_leading_bit	First data bit of 2-bit leading mode	1'b0(POR)
1	R/W	second_leading_bit	Second data bit of 2-bit leading mode	1'b0(POR)
0	R/W	leading_bit_mode	RA8815 2-bit leading mode 0: No leading bits 1: 2-bit leading for each transaction	1'b0 (POR)

5.9.4 SPI interrupt

Address: 3eh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	CPOL	Clock Polarity	1'b1(POR)
6	R/W	CPHA	Clock Phase	1'b1(POR)
5-4	R/W	CS_SEL	SPI CS Select 00: CS0 01: CS1 10: CS2(Default) 11: CS2	2'b10(POR)
3	RO	slv_hid	SPI slave flag to HID interrupt 0: access to internal register 1: flag to HID interrupt	1'b0 (POR)
2	RO	slv_rw	SPI slave read/write flag 0: read 1: write	1'b0 (POR)
1	R/W	slv_int_en	SPI slave interrupt 0: no interrupt 1: interrupt (Default) Ext MCU can program this bit to make slave mode interrupt	1'b1 (POR)
0	R/W	mst_int_en	SPI master interrupt enable 0: disable 1: enable (Default) Control HW to make master mode interrupt	1'b1 (POR)

**Note:

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1. Bit[1]: When SPI interface is in slave mode, SPI interrupt will happened when bit[1] ==1, which is written by external MPU via SPI. Interrupt (HID) would be cleaned once address 0x10 was written.
2. Bit[0]: When SPI interface is in master mode, SPI interrupt will happened when bit[0] ==1 and every SPI master command completed. Interrupt (HID) would be cleaned once address 0x10 was written.

5.9.5 SPI Control Register 3

Address: 3fh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	data_len	The data length of read/write, 0000_0000: Reserved 0000_0001: 1 bytes 0000_0010: 2 bytes 0000_0011: 3 bytes . . . 1111_1111:255 bytes	8'd0 (POR)

SPI example for master mode:

Write 3 bytes:

(Address = 92, DATA = 55,AA)

Write 0x38~0x3A = 92 55 AA (Data register)

Write 0x3F = 03 (Write 3 bytes length)

Write 0x3D = A0 (SPI start)

Read 3 bytes:

(Address = 92)

Write 0x38= 92 (Data register)

Write 0x3F = 03 (Read 3 bytes length)

Write 0x3D = 80 (SPI start)

Read 0x38~0x3A

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5.10GPIO

5.10.1 GPO data register

Address Offset: C0-C1h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPO_0_reg GPO_1_reg	GPO data register which represents	16'h0 (POR)

5.10.2 GPI data register

Address Offset: C2-C3h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R		GPI data register which represents	16'h0 (POR)

5.10.3 GPIO direction control register

Address Offset: C4-C5h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPOE_0 GPOE_1	GPIO output enable register which represents for pin XGPIO[15:0] 1: the corresponding pins are used as outputs 0: the corresponding pins are used as inputs	16'h0 (POR)

5.10.4 GPIO interrupt enable mask register

Address Offset: C6-C7h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_EN	GPIO_E, GPIO interrupt enable mask which represents for pins, XGPIO[15:0] 1: enable, 0: disable	16'h0 (POR)

5.10.5 GPIO debouncing register

Address Offset: C8-C9h
Default Value: 0000h (MSB -> LSB)

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_Deb	Enable the clock scale of millisecond (32 ms) for debouncing, default 1 1: enable, 0: disable	16'h0 (POR)

5.10.6 GPI remote choose

Address Offset: 0xE2~E3h

Bits	R/W	Bit Mnemonic	Description	default
15:0	R/W	GPI_RWL GPI_RWH	D0==1'b1:GPI[0] remote wake up enabled D1==1'b1:GPI[1] remote wake up enabled D2==1'b1:GPI[2] remote wake up	16'h0 (POR)

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			enabled D3==1'b1:GPI[3] remote wake up enabled D4==1'b1:GPI[4] remote wake up enabled D5==1'b1:GPI[5] remote wake up enabled D6==1'b1:GPI[6] remote wake up enabled D7==1'b1:GPI[7] remote wake up enabled D8==1'b1:GPI[8] remote wake up enabled D9==1'b1:GPI[9] remote wake up enabled D10==1'b1:GPI[10] remote wake up enabled D11==1'b1:GPI[11] remote wake up enabled D12==1'b1:GPI[12] remote wake up enabled D13==1'b1:GPI[13] remote wake up enabled D14==1'b1:GPI[14] remote wake up enabled D15==1'b1:GPI[15] remote wake up enabled	

5.10.7 GPIO pull-up/down

Address Offset: 0xE4

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	GPIO_PD0[7]	GPIO_7 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
6	R/W	GPIO_PD0[6]	GPIO_6 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD0[5]	GPIO_5 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD0[4]	GPIO_4 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD0[3]	GPIO_3 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD0[2]	GPIO_2 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD0[1]	GPIO_1 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD0[0]	GPIO_0 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

Address Offset: 0xE5

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	GPIO_PD1[7]	GPIO_15 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD1[6]	GPIO_14 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD1[5]	GPIO_13 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

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4	R/W	GPIO_PD1[4]	GPIO_12 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD1[3]	GPIO_11 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD1[2]	GPIO_10 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD1[1]	GPIO_9 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD1[0]	GPIO_8 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

Address Offset: 0xE6

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	GPIO_PD2[7]	GPIO23 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD2[6]	GPIO_22 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD2[5]	GPIO_21 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD2[4]	GPIO_20 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD2[3]	GPIO_19 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD2[2]	GPIO_18 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD2[1]	GPIO_17 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD2[0]	GPIO_16 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

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5.11 Arbitrary sine-tone generator

There are four (4) memory banks to store user defined waveform in CM6530N design. This function would generate waveform data that is desired to be heard from earphones. For example, when function keys were pressed or do other operations, user can predefine two different waveforms with 96K and 88.2K sampling rates and stores it in corresponding memory banks. The waveform data format must comply with the following specifications:

1. 16 bits PCM with 2's complement
2. First word must define waveform length (Length[9:0]= {byte1[2:0], byte0[7:0]})
3. Waveform length must less than 2046
4. Four memory banks

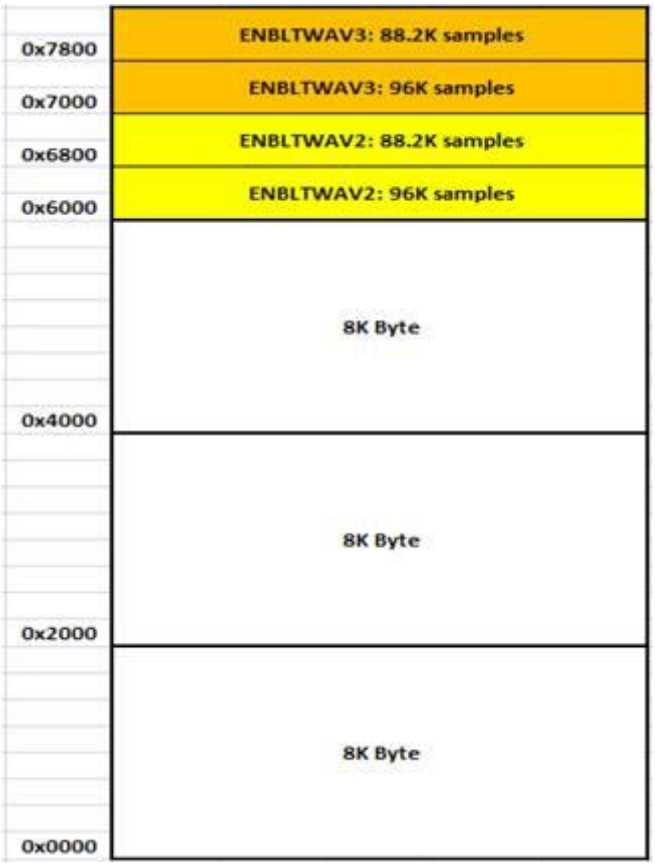
Bank1: 0x6000~0x67FF (Length: 0x6000~0x6001, Waveform data 0x6002~0x67FF)

Bank2: 0x6800~0x6FFF (Length: 0x6800~0x6801, Waveform data 0x6802~0x6FFF)

Bank3: 0x7000~0x77FF (Length: 0x7000~0x7001, Waveform data 0x7002~0x77FF)

Bank4: 0x7800~0x7FFF (Length: 0x7800~0x7801, Waveform data 0x7802~0x7FFF)

Generating sine-tone is based on a look-up table and the step size of look-up table for different sampling rates is adjusted automatically.



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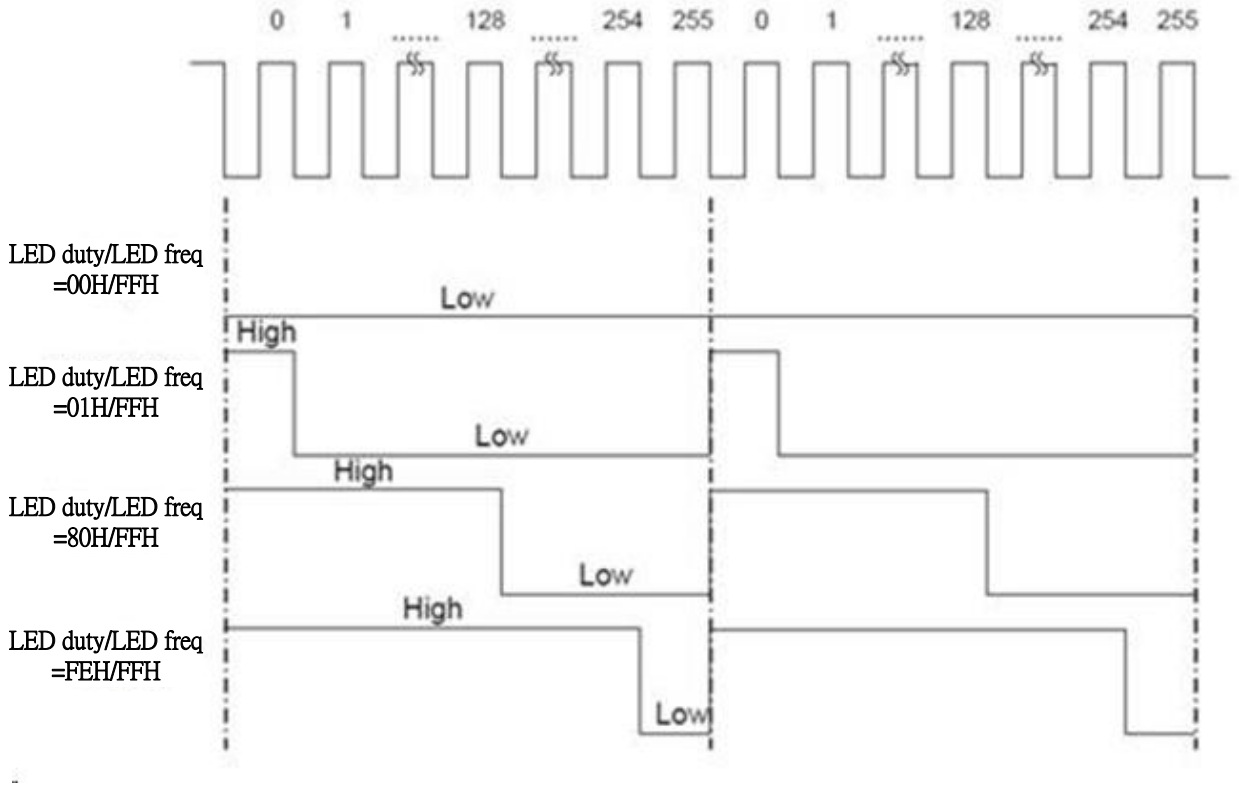
5.12 Tri-colored led control setting

PWM function is generated by LED counter and output the PWM signal to GPIO pin. The 8-bit counter counts modulus 256 controlled by LED freq, LED duty register. The LED unit register controls PWM resolution. When the LED freq register value is equal to the LED duty register (high), the PWM output also goes high. When the LED freq, LED duty register reaches zero, the PWM output is forced to go low. The low-to-high ratio (duty) of the PWM output is LED duty/LED freq.

LED duty	LED freq	LED unit (256 step)	PWM duty range
00H	FFH	00:10.5ms 01:5.45ms 10:2.73ms 11:1.36ms	00H/FFH ~FEH/FFH
01H	FFH		
80H	FFH		
FEH	FFH		

The Output Duty of PWM has different timings. Duty range is from 0/256~255/256.



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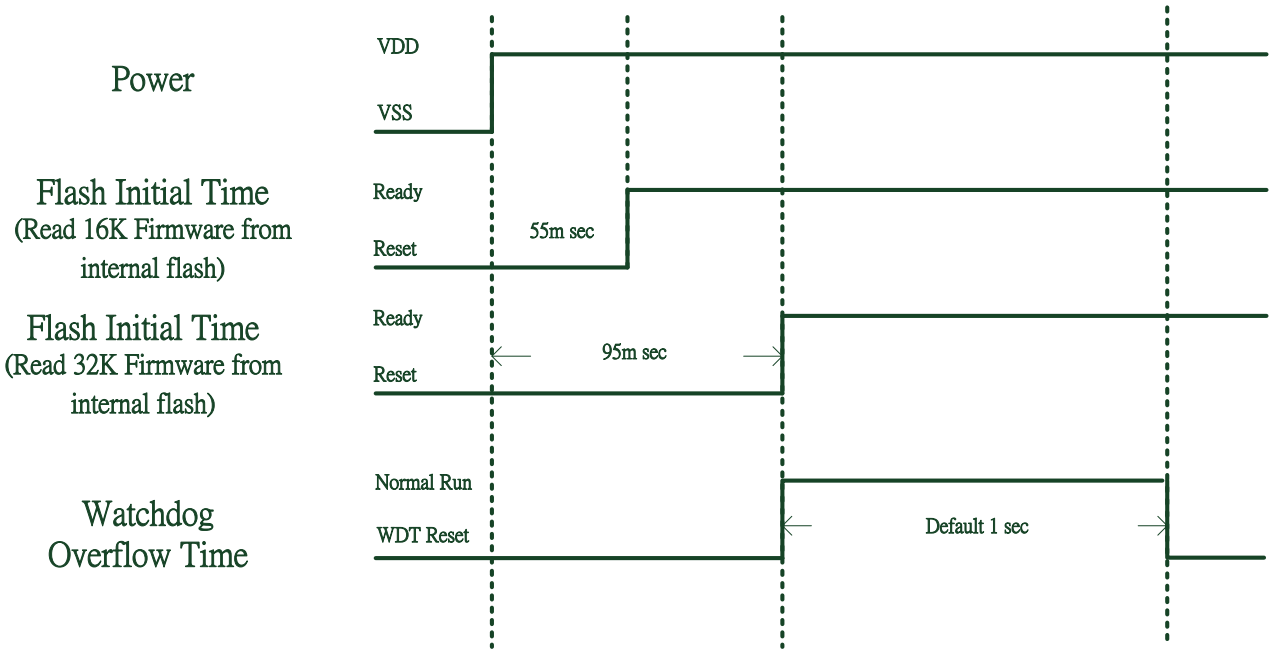
5.13 Reset



5.13.1 Watchdog reset timer

The watchdog timer is a 15-bit counter that is incremented every 24 or 384 clock cycles. It is used to provide the system supervision in case of software or hardware upset. If the software was not able to refresh the watchdog timer after 786336 or 12581376 clock cycles (65ms or 1s when using 12MHz clock), an internal reset is generated.

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6 Electrical characteristics

6.1 Absolute maximum ratings

Test conditions: DV50 = 5V, AV50 = 5V, DGND =0V, TA=+25oC

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-25	-	150	°C
Operating ambient temperature	T_A	-15	25	70	°C
Digital supply voltage(DV50)		4.5	5.0	5.5	V
Analog supply voltage(AV50)		4.5	5.0	5.5	V
I/O pin voltage	-	GND	-	3.3	V
ESD (Body mode)			±4000		V
ESD (Machine mode)			±200		V

6.2 Recommended operation conditions

Parameter	Symbol	Min.	Typ	Max.	Unit
Digital supply voltage(DV50)	-		5		V
Analog supply voltage(AV50)			5		V
Operating ambient temperature			25		°C
Crystal clock	-		12.000		MHz

6.3 Power consumption

Test Conditions: DGND =0V, TA=+25°C, MCU Clock = 12MHz.
Sample Rate=48kHz, 16Bits, Operation: HP-Out Playback + Microphone-In Recording, EQ disable, SPDIF out disable, Master volume = 0dB, Microphone Gain = 0dB

power consumption (CM6530N only)	PC (DV50=5V, AV50 = 5V)	Android Phone (DV50=5V, AV50 = 5V)	Unit
Quiescent(Normal working status without audio data transfer)	-	8.91mA	mA
Suspend	2.4mA	-	mA
Playback + Recording (crystal mode)	25mA	25mA	mA
Playback + Recording (non-crystal mode)	33mA	33mA	mA

power consumption (CM6530N+CM9600)	PC (DV50=5V, AV50 = 5V)	Android Phone (DV50=5V, AV50 = 5V)	Unit
Quiescent(Normal working status without audio data transfer)	-	8.91mA	mA
Suspend	2.4mA	-	mA
Playback + Recording (crystal mode)	35mA	35mA	mA
Playback + Recording (non-crystal mode)	43mA	43mA	mA

**Note: The CM9600 is a high performance, low power, dual I2S interface audio CODEC. Please refer to CM9600's datasheet to find out more information.
**Note: Power consumption for crystal mode is 8mA lower than non-crystal mode.

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6.4 DC characteristics

Test Conditions: DV50=5V, V_{DD} = 3.3V, DGND =0V, TA=+25°C, V_{DD} = 3.3V

Parameter	Symbol	Min.	Typ	Max.	Unit
Operation Voltage range	DVDD	4.5	5	5.5	
DC Input voltage range (GPIO,I2C,SPI,SPDIF)	DCVin	-0.3		5.5	V
Input High-level voltage (GPIO,I2C,SPI,SPDIF)	Vih	2	2		V
Input Low-level voltage (GPIO,I2C,SPI,SPDIF)	Vil		0.8	0.8	V
Output High-level voltage (GPIO,I2C,SPI,SPDIF)	Voh	2.4	-	3.6	V
Output Low-level voltage (GPIO,I2C,SPI,SPDIF)	Vol	0	-	0.4	V
Output source current (GPIO, I2C,SPI,SPDIF)	IOH		8		mA
Output sink current (GPIO, I2C,SPI,SPDIF)	IOL		8		mA
VREG33 driver current	IVREG			10	mA

**Note: DVDD18,AVDD36,AV42_DA,AV36_DAL,AV36_DAR without current drivecapacity

6.5 USB transceiver

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Regulator Voltage	XV33	XV33	3.0	3.3	3.6	V	CL =10uF
Driver Output Impedance including the 22ΩExternal Serial Resistor	RO	D+/D−	24		40	Ω	static, LOW or HIGH
Rise and Fall Times	tr/tf		3	10	19	ns	CL = 50 pF, driver mode
Rise/Fall Time Matching	MA_TRTF		90		110	%	CL = 50 pF, driver mode
Crossover Voltage	VXOVER		1.30	1.75	2.0	V	CL = 50 pF, driver mode
Differential Receiver Common-Mode Range	VCM_DREC		0.8		2.5	V	
Single-ended Receiver Threshold Voltage	VT_SREC		0.8		2.0	V	
Switchable Pull-up Resistor	RPU	VREG, D+		1.5		kΩ	

7 Package dimension

Model Number	Package	Operating Ambient Temperature	Supply Range
CM6530N	48-Pin QFN 6.5mm×5mm×0.85mm (Plastic)	-15°C to +70°C	DVdd = 5V, AVdd = 5V

Outline Dimensions *Dimensions shown in inches and (mm)

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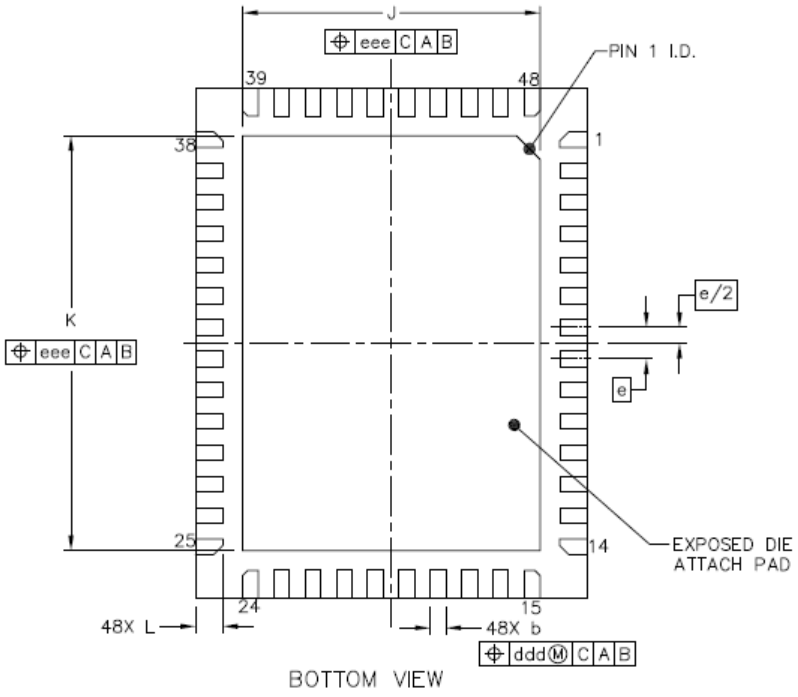
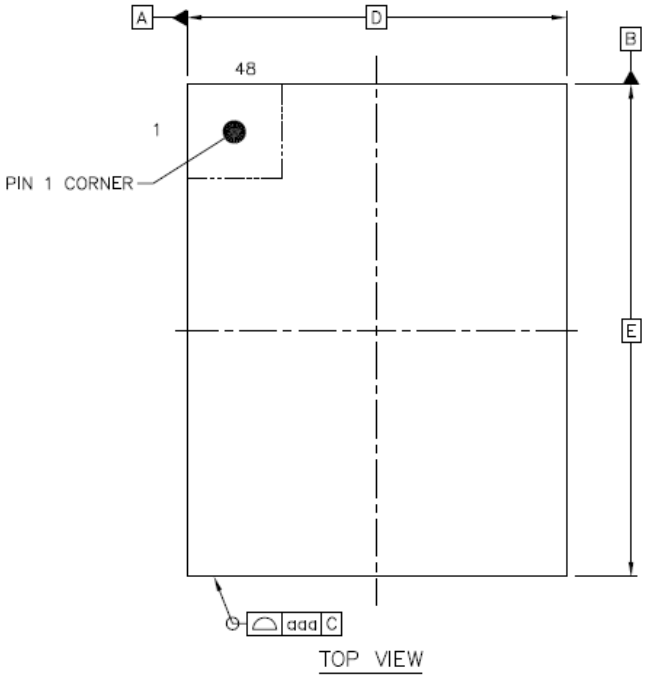
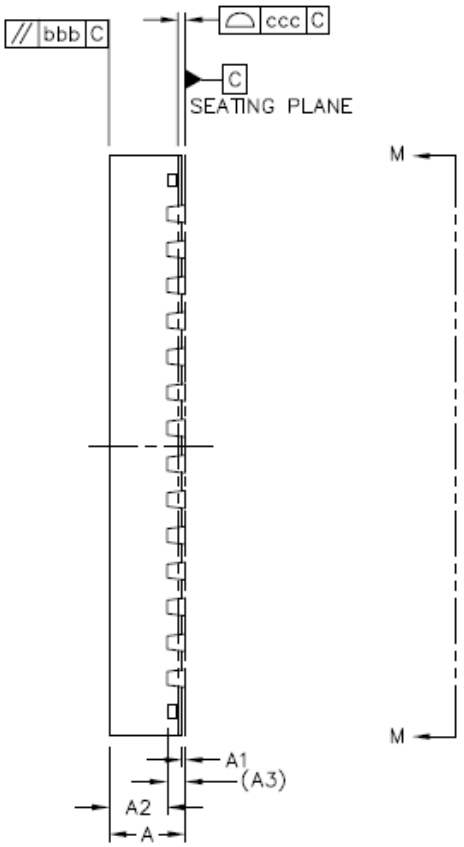
7.1 Package Dimension of CM6530N

48-Lead Thin Plastic Quad Flatpack (QFN)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		6.5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	3.7	3.8	3.9
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

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— End of Datasheet —

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