FOUNDER

# Embedded Tailor™ SD Flash
# MKDVXXCL

# Commercial Grade Specification

**Ver.1.0**
**Apr.2018**

**Revision History**

| Date | Rev. | Description |
|---|---|---|
| 2018/4/20 | 1.0 | Original version |
| 2019/2/15 | 2.0 | Operating Temperature |
| | | |

# CONTENTS

# 1. Introduction

MK Founder Tailor™ SD is an embedded storage solution designed in a LGA package form. The operation of SD is similar to an SD card which is an commercial standard.

Tailor™ SD consists of NAND flash and a high performance controller. 3.3V supply voltage is required for the NAND area (VCC).

Tailor™ SD is fully compliant with SD2.0 interface, which allows most of general CPU to utilize.

Tailor™ SD has high performance at a competitive cost, high quality and low power consumption.

# 2. Product List

| Part No. | Capacity | Package | Size |
|---|---|---|---|
| | | | |
| MKDV1GCL | 1Gb | LGA-8 | 6x8mm |
| MKDV2GCL | 2Gb | LGA-8 | 6x8mm |
| MKDV4GCL | 4Gb | LGA-8 | 6x8mm |
| MKDV8GCL | 8Gb | LGA-8 | 6x8mm |

# 3. Features

- Support up to 50Mhz clock frequency
- Support 1/4 bit mode
- Built-in HW ECC Engine and highly reliable NAND management mechanism
- Write speed up to class 6
- Smaller package LGA-8

# 4. Physical Characteristics

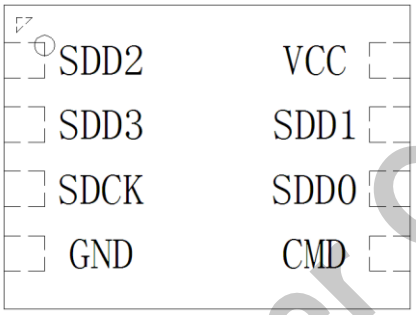
## 4.1. Temperature

1) Operation Conditions
Temperature Range: Ta = -20 to 85 degrees centigrade

2) Storage Conditions
Temperature Range: Tstg = −55 to 150 degrees centigrade

# 5. Pin Assignments

**TOP VIEW**




**PIN NAMES**

| | |
|---|---|
| SD0 toSD3 | I/O pins |
| CLK | Tailor™ SD clock signal |
| CMD | Tailor™ SD command signal |
| $V_{DD}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No Connection |

# 6. Usage

## 6.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

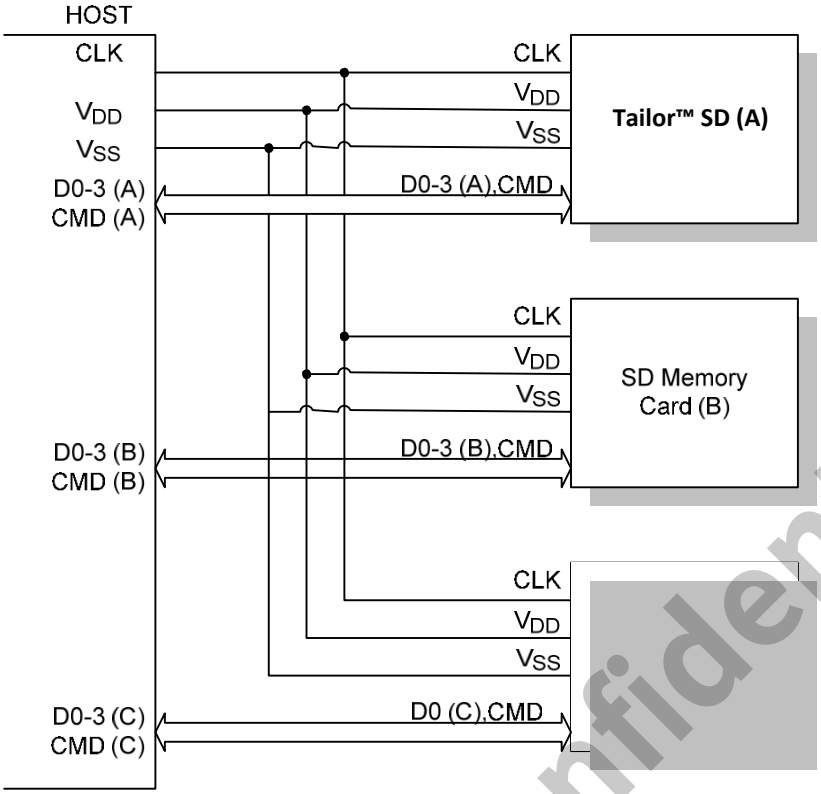
Multiplied SD cards connections are available to the host. Common $V_{DD}$, $V_{SS}$ and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each device from host.

This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

**Command**: Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the device. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

**Response**:Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

**Data**:Data can be transfer from the card to the host or vice versa. Data is transferred via the data lines.




| | |
|---|---|
| CLK | Host card Clock signal |
| CMD | Bi-directional Command/ Response Signal |
| DAT0 - DAT3 | 4 Bi-directional data signal |
| $V_{DD}$ | Power supply |
| $V_{SS}$ | GND |

## 6.2. Card Initialize

To initialize the Tailor™ SD, follow the following procedure is recommended example.

1) Supply Voltage for initialization.

Host System can apply the Operating Voltage from initialization to the card. Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to “Low” level. Then, issue CMD0. In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up

to “High” normally).

Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.

4) Apply the indicated operating voltage to the card.

Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared. (Bit 31 Busy = 1)  If response time out occurred, host can recognize not SD Card.

5) Issue the CMD2 and get the Card ID (CID).

Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)

6) Issue the CMD7 and move to the transfer state.

If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.

7) Issue the ACMD13 and poll the Card status as SD Memory Card.  Check SD_CARD_TYPE value. If significant 8 bits are “all zero”, that means SD Card. If it is not, stop initialization.

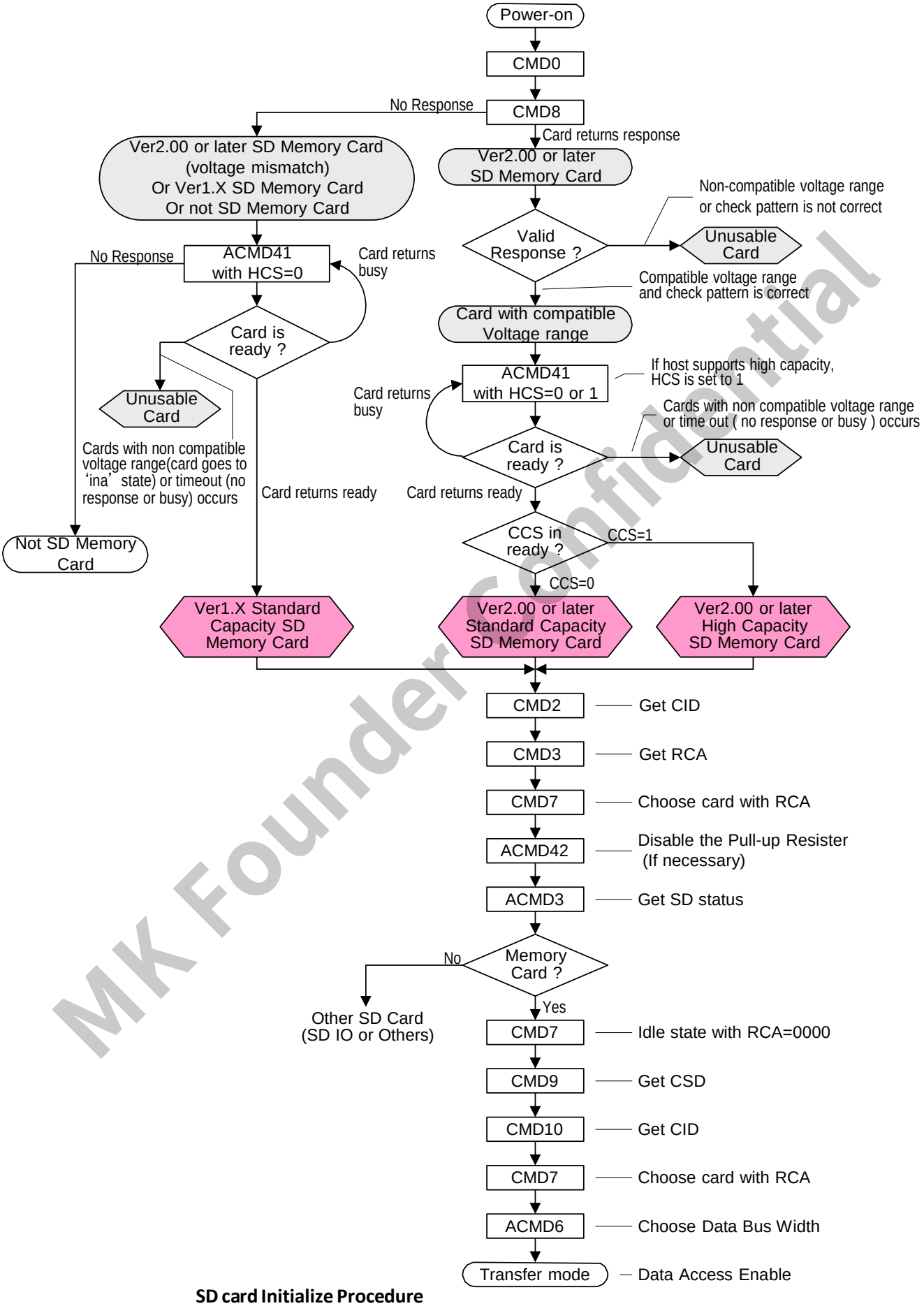
8) Issue CMD7 and move to standby state. Issue CMD9 and get CSD.

Issue CMD10 and get CID.

9) Back to the Transfer state with CMD7.

Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.




**SD card Initialize Procedure**

# 6.3 DC Characteristics

**DC Characteristics**

| Item | | Symbol | MIN. | MAX. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | 2.7 | 3.6 | V | |
| Input Voltage | High Level | $V_{IH}$ | $V_{DD}$×0.625 | $V_{DD}$+0.3 | V | |
| | Low Level | $V_{IL}$ | $V_{SS}$-0.3 | $V_{DD}$×0.25 | V | |
| Output Voltage | High Level | $V_{OH}$ | $V_{DD}$×0.75 | — | V | $I_{OH}$ = -2mA , $V_{DD}$=$V_{DD}$ min |
| | Low Level | $V_{OL}$ | — | $V_{DD}$×0.125 | V | $I_{OL}$ = 2mA , $V_{DD}$=$V_{DD}$ min |
| Standby Current | | $I_{CC1}$ | — | 30 | mA | $V_{DD}$ = 3.6V , Clock 25MHz |
| | | | — | 0.1 | | $V_{DD}$ = 3.3V, Clock STOP, Ta=25℃ |
| Operation Current (*) | Write | $I_{CC2}$ | — | 50 | mA | 3.3V / 25MHz, 50MHz |
| | Read | | — | 50 | | |
| Input Voltage Setup Time | | Vrs | — | 250 | ms | From 0V to VDD min |

*) Peak Current: RMS value over a 10usec period

**Peak Voltage and Leak Current**

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Peak voltage on all lines | | -0.3 | $V_{DD}$+0.3 | V | |
| Input Leakage Current for all pins | | -10 | 10 | uA | |
| Output Leakage Current for all outputs | | -10 | 10 | uA | |

**Signal Capacitance**

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Pull up Resistance | $R_{CMD}$ $R_{DAT}$ | 10 | 100 | kΩ | |
| Total bus capacitance for each signal line | $C_L$ | — | 40 | pF | 1 card $C_{HOST}$+$C_{BUS}$≦30pF |
| Card capacitance for signal pin | $C_{CARD}$ | — | 10 | pF | |
| Pull up Resistance inside card ( pin1 ) | $R_{DAT3}$ | 10 | 90 | kΩ | |
| Capacity Conneted to Power line | $C_C$ | — | 5 | uF | |

# 7. Internal Information

## 7.1 Registers

The Tailor™ SD has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status. DSR IS NOT SUPPORTED in this card.

There are two types of register groups.

MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR SD card Specific: SD Status

**SD card Registers**

| Resister Name | Bit Width | Description |
|---|---|---|
| OCR | 32 | Operation Conditions (VDU Voltage Profile and Busy Status |
| CID | 128 | Card Identification information |
| CSD | 128 | Card specific information |
| RCA | 16 | Relative Card Address |
| DSR | 16 | Not Implemented (Programmable Card Driver): Driver Stage Register |
| SCR | 64 | SD Memory Card's special features |
| SD Status | 512 | Status bits and Card features |

# 7.1.1 OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.

**OCR register definition**

| OCR bit | VDD voltage window | Initial | | | |
|---|---|---|---|---|---|
| | | 1Gb | 2Gb | 4Gb | 8Gb |
| 31 | Card power up status bit(busy) | “0” = busy “1” = | | | |
| 30 | Card Capacity Status | “0”= SD Memory Card | | | |
| 29-25 | reserved | All ‘0’ | | | |
| 24 | Switching to 1.8V Accepted(S18A) | 0 | | | |
| 23 | 3.6 - 3.5 | 1 | | | |
| 22 | 3.5 - 3.4 | 1 | | | |
| 21 | 3.4 - 3.3 | 1 | | | |
| 20 | 3.3 - 3.2 | 1 | | | |
| 19 | 3.2 - 3.1 | 1 | | | |
| 18 | 3.1 - 3.0 | 1 | | | |
| 17 | 3.0 - 2.9 | 1 | | | |
| 16 | 2.9 - 2.8 | 1 | | | |
| 15 | 2.8 - 2.7 | 1 | | | |
| 14 | Reserved | 0 | | | |
| 13 | Reserved | 0 | | | |
| 12 | Reserved | 0 | | | |
| 11 | Reserved | 0 | | | |
| 10 | Reserved | 0 | | | |
| 9 | Reserved | 0 | | | |
| 8 | Reserved | 0 | | | |
| 7 | Reserved for Low Voltage Range | 0 | | | |
| 6 | Reserved | 0 | | | |
| 5 | Reserved | 0 | | | |
| 4 | Reserved | 0 | | | |
| 3-0 | reserved | All ‘0’ | | | |

bit 23-4: Describes the SD Card Voltage

bit 31 indicates the card power up status. Value “1” is set after power up and initialization procedure has been completed.

## 7.1.2. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information. (Refer Appendix 3. for the detail) The Value of CID Register is vender specific.

**Table 11: CID Register**

| Field | Width | CID-slice | Initial Value | | | |
|---|---|---|---|---|---|---|
| | | | 1Gb | 2Gb | 4Gb | 8Gb |
| MID | 8 | [127:120] | TB | | | |
| OID | 16 | [119:104] | TBD | | | |
| PNM | 40 | [103:64] | TBD | TBD | TBD | -- |
| PRV | 8 | [63:56] | TB | | | |
| PSN | 32 | [55:24] | (a) (Product serial number) | | | |
| - | 4 | [23:20] | All “0b” | | | |
| MDT | 12 | [19:8] | (a) (Manufacture date) | | | |
| CRC | 7 | [7:1] | (b) (CRC) | | | |
| - | 1 | [0:0] | 1b | | | |

(a): Depends on the SD Card. Controlled by Production Lot.
(b) Depends on the CID Register

# 7.2.3. CSD Register

CSD is Card-Specific Data register provides information on 128bit width. Some field of this register can writable by PROGRAM_CSD (CMD27).

**CSD Register**

| Field | Width | Cell Type | CSD Slice | Initial Value | | | |
|---|---|---|---|---|---|---|---|
| | | | | 1Gb | 2Gb | 4Gb | 8Gb |
| CSD_STRUCTURE | 2 | R | [127:126] | 01b | | | |
| - | 6 | R | [125:120] | All “0b” | | | |
| TAAC | 8 | R | [119:112] | 0_0001_110b (1ms) | | | |
| NSAC | 8 | R | [111:104] | 00000000 | | | |
| TRAN_SPEED | 8 | R | [103:96] | 0_0110_010b | | | |
| CCC | 12 | R | [95:84] | 0101_1011_0101 | | | |
| READ_BL_LEN | 4 | R | [83:80] | 1001b | | | |
| READ_BL_PARTIAL | 1 | R | [79:79] | 0b | | | |
| WRITE_BLK_MISALIG | 1 | R | [78:78] | 0b | | | |
| READ_BLK_MISALIGN | 1 | R | [77:77] | 0b | | | |
| DSR_IMP | 1 | R | [76:76] | 0b | | | |
| - | 6 | R | [75:70] | All “0b” | | | |
| C_SIZE | 22 | R | [69:48] | TBD | TBD | TBD | -- |
| - | 1 | R | [47:47] | 0b | | | |
| ERASE_BLK_EN | 1 | R | [46:46] | 1b | | | |
| SECTOR_SIZE | 7 | R | [45:39] | 11_1111_1 | | | |
| WP_GRP_SIZE | 7 | R | [38:32] | 000_0000 | | | |
| WP_GRP_ENABLE | 1 | R | [31:31] | 0b | | | |
| - | 2 | R | [30:29] | 00b | | | |
| R2W_FACTOR | 3 | R | [28:26] | 010b | | | |
| WRITE_BL_LEN | 4 | R | [25:22] | 1001b | | | |
| WRITE_BL_PARTIAL | 1 | R | [21:21] | 0b | | | |
| - | 2 | R | [20:16] | All “0b” | | | |
| FILE_FORMAT_GRP | 1 | R | [15:15] | 0b | | | |
| COPY | 1 | R/W(1) | [14:14] | 0b | | | |
| PERM_WRITE_PROTE | 1 | R/W(1) | [13:13] | 0b | | | |
| TMP_WRITE_PROTEC | 1 | R/W | [12:12] | 0b | | | |
| FILE_FORMAT | 2 | R | [11:10] | 00b | | | |
| - | 2 | R | [9:8] | All “0b” | | | |
| CRC | 7 | R/W | [7:1] | (CRC) | | | |
| - | 1 | - | [0:0] | 1b | | | |

Cell Type: R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable

Note: Erase of one data block is not allowed in this card. This information is indicated by “ERASE_BLK_EN”. Host System should refer this value before one data block size erase.

### 7.1.4. RCA Register

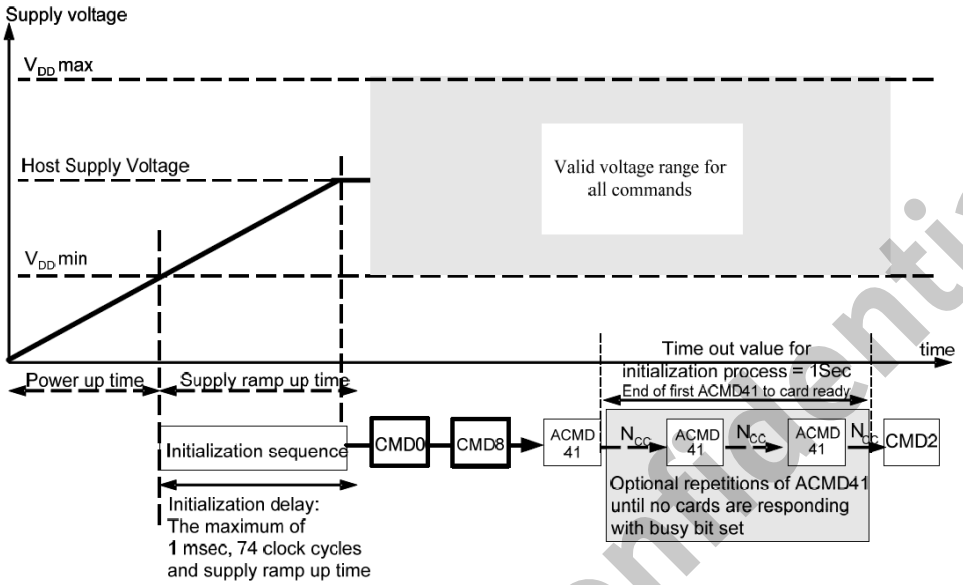
The writable 16bit relative card address register carries the card address in SD Card mode.

### 7.1.5. DSR Register

This register is not implemented on this car

# 8. Power Scheme

## 8.1. Power Up



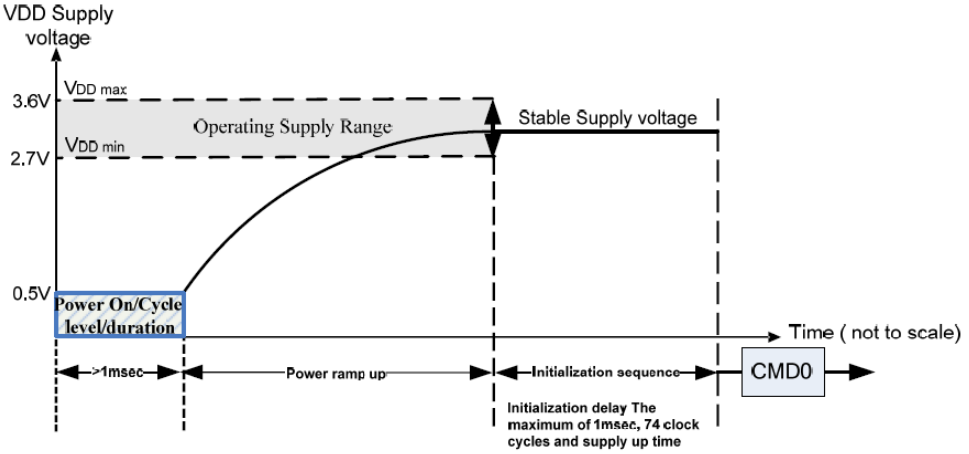

'Power up time' is defined as voltage rising time from 0 volt to VDD min.

'Supply ramp up time' provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the Tailor™ SD can accept the first command,

The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the Tailor™ SD with keeping CMD line to high.

## 8.2 Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



## 8.2.1 Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable Tailor™ SD hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

## 8.2.2 Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

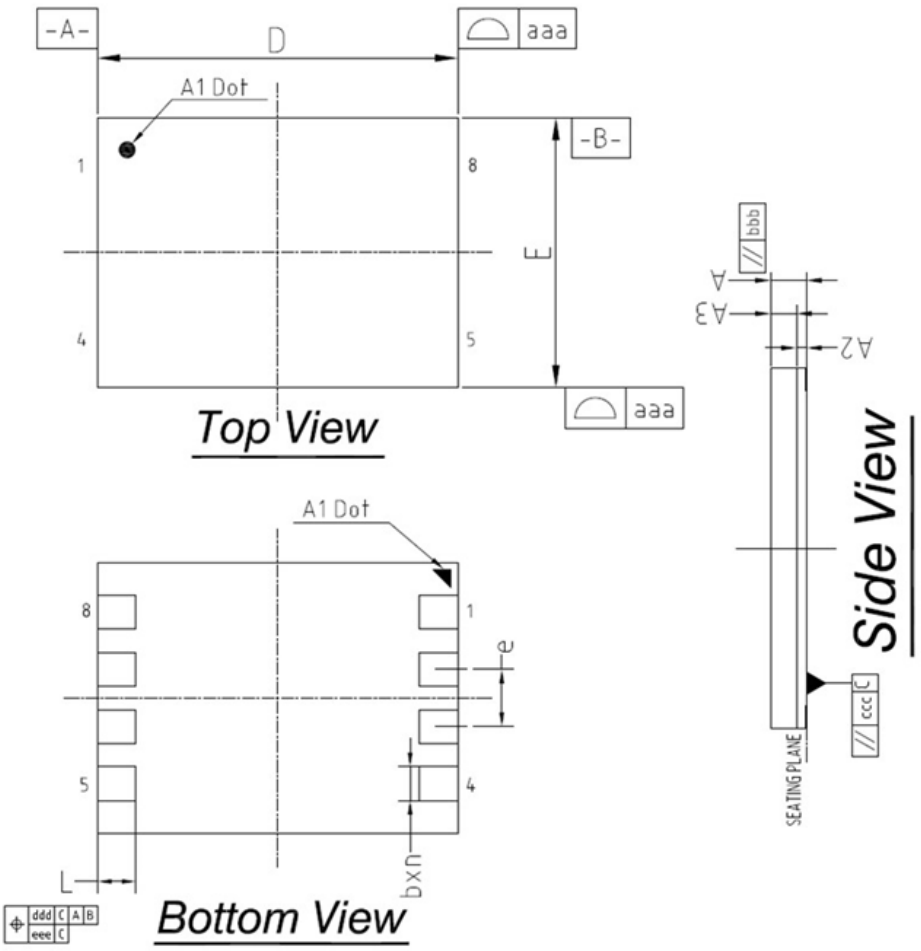
## 8.2.3 Power Supply Ramp Up

When the host shuts down the power, the VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

# 9. Package Dimensions

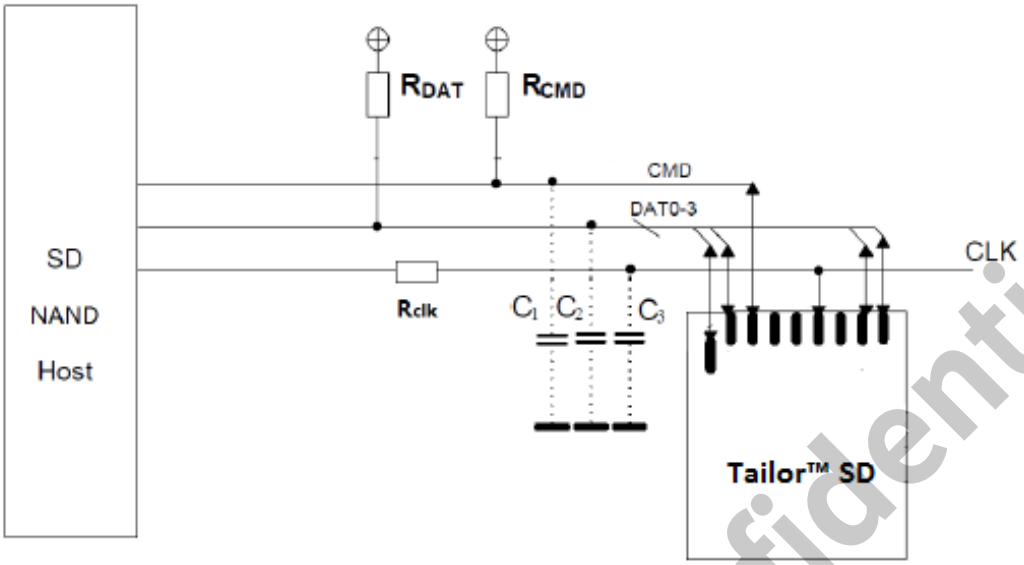
**Package Outline Drawing Information for LGA**




**LGA (8 x 6 x 0.8mm) Dimension Table**

| Symbol | Dimension (MM) | | | Dimension (MIL) | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.700 | 0.750 | 0.800 | 27.559 | 29.528 | 31.496 |
| A2 | 0.190 | 0.220 | 0.250 | 7.480 | 8.661 | 9.843 |
| A3 | 0.510 | 0.530 | 0.540 | 20.079 | 20.866 | 21.260 |
| L | 0.800 | 0.850 | 0.900 | 31.496 | 33.465 | 35.433 |
| b | 0.700 | 0.750 | 0.800 | 27.559 | 29.528 | 31.496 |
| e | | 1.270 | | | 50.000 | |
| n | | 8 | | | 8 | |
| D | 7.900 | 8.000 | 8.100 | 311.023 | 314.960 | 318.897 |
| E | 5.900 | 6.000 | 6.100 | 232.283 | 236.220 | 240.157 |
| aaa | | 0.100 | | | 3.937 | |
| bbb | | 0.150 | | | 5.906 | |
| ccc | | 0.100 | | | 3.937 | |
| ddd | | 0.150 | | | 5.906 | |
| eee | | 0.080 | | | 3.150 | |

# 10. Reference Design




RDAT and RCMD (10K~100 kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when Tailor™ SD is in a high-impedance mode.

The host shall pull-up all DAT0-3 lines by RDAT, even if the host uses the Tailor™ SD as 1 bit mode-only in SD mode. It is recommended to have 2.2uF capacitance on VDD.

Rclk reference 0~120 Ω

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