# Samwin®

SW47N65K2

N-channel Enhanced mode TO-247 MOSFET

Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 56mΩ)@V_{GS}=10V
- Low Gate Charge (Typ 103nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: LED, UPS, Charge, Servicer

**TO-247**

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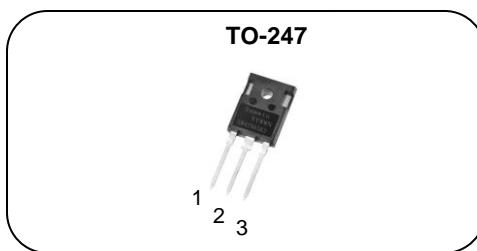
1. Gate 2. Drain 3. Source

BV_{DSS} : 650V
I_D : 47A
$R_{DS(ON)}$: 56mΩ

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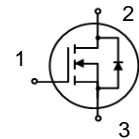
General Description

This power MOSFET is produced with super junction advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW T 47N65K2	SW47N65K2	TO-247	TUBE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to source voltage		650	V
I_D	Continuous drain current (@T_C=25ºC)		47*	A
	Continuous drain current (@T_C=100ºC)		30*	A
I_{DM}	Drain current pulsed	(note 1)	188	A
V_{GS}	Gate to source voltage		±30	V
E_{AS}	Single pulsed avalanche energy	(note 2)	1463	mJ
E_{AR}	Repetitive avalanche energy	(note 1)	118	mJ
dv/dt	MOSFET dv/dt ruggedness (@VDS=0~400V)		30	V/ns
dv/dt	Peak diode recovery dv/dt	(note 3)	20	V/ns
P_D	Total power dissipation (@T_C=25ºC)		338	W
	Derating factor above 25ºC		2.7	W/ºC
T_{STG}, T_J	Operating junction temperature & storage temperature		-55 ~ + 150	ºC
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.		300	ºC

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.37	ºC/W
R_{thja}	Thermal resistance, Junction to ambient	35	ºC/W

Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C		0.58		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V			1	uA
		V_{DS}=520V, T_C=125°C			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5		4.5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D=23A		56	72	mΩ
G_{fs}	Forward transconductance	V_{DS}=30V, I_D=23A		49		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=200V, f=1MHz		4515		pF
C_{oss}	Output capacitance			154		
C_{rss}	Reverse transfer capacitance			2.2		
$t_{d(on)}$	Turn on delay time	V_{DS}=325V, I_D=47A, R_G=25Ω, V_{GS}=10V (note 4,5)		52		ns
t_r	Rising time			100		
$t_{d(off)}$	Turn off delay time			252		
t_f	Fall time			102		
Q_g	Total gate charge	V_{DS}=520V, V_{GS}=10V, I_D=47A, I_g=5.5mA (note 4,5)		103		nC
Q_{gs}	Gate-source charge			25		
Q_{gd}	Gate-drain charge			37		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		1.2		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			47	A
I_{SM}	Pulsed source current				188	A
V_{SD}	Diode forward voltage drop.	I_S=47A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=20A, V_{GS}=0V, dI_F/dt=100A/us		445		ns
Q_{rr}	Reverse recovery charge			7.2		uC

※. Notes
1. Repeatitive rating : pulse width limited by junction temperature.
2. L =45.7mH, IAS =8A, VDD=50V, RG=25Ω, Starting TJ = 25°C
3. I_{SD} ≤ 20A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

### Fig. 1. On-state characteristics
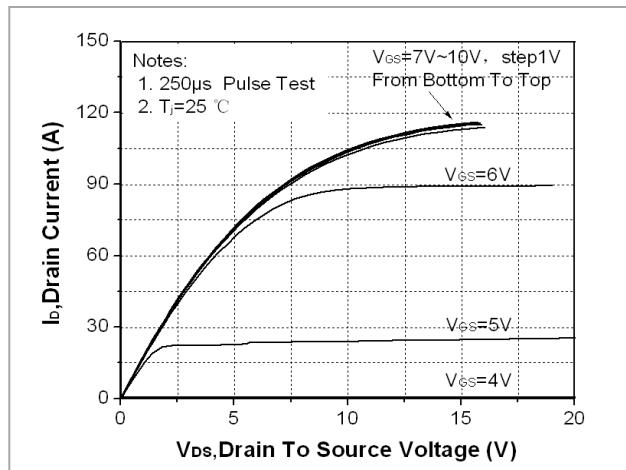
### Fig. 2. Transfer Characteristics
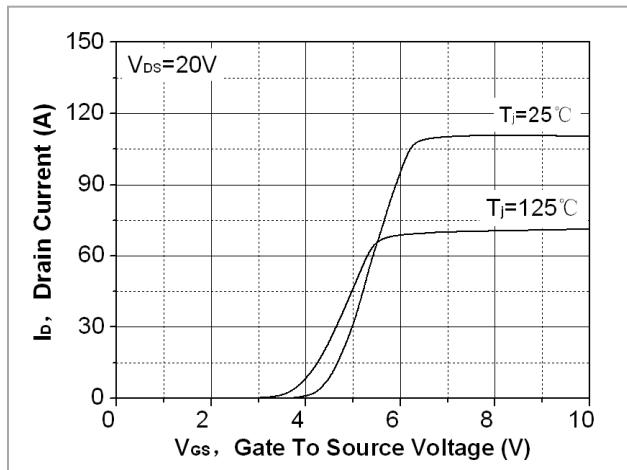
Fig. 3. On-resistance variation vs. drain current and gate voltage
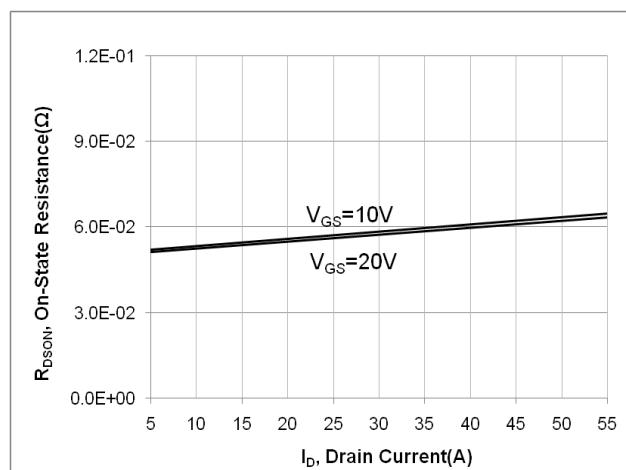

Fig. 4. On-state current vs. diode forward voltage
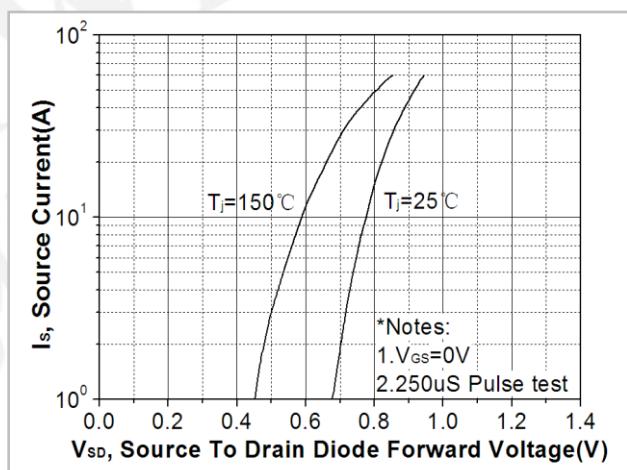

Fig 5. Breakdown voltage variation vs. junction temperature
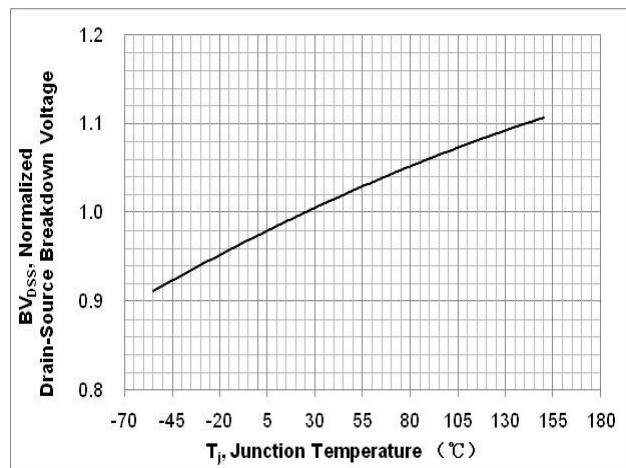

### Fig. 6. On-resistance variation vs. junction temperature
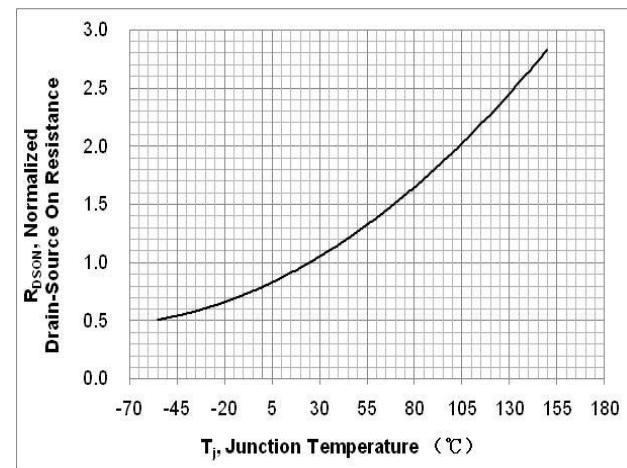
Fig. 7. Gate charge characteristics
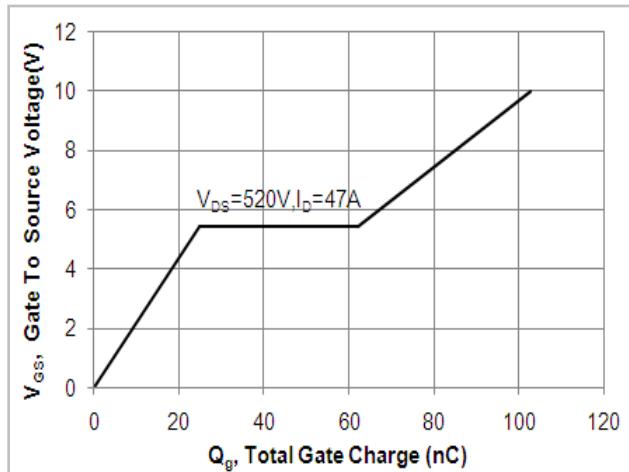

Fig. 8. Capacitance Characteristics
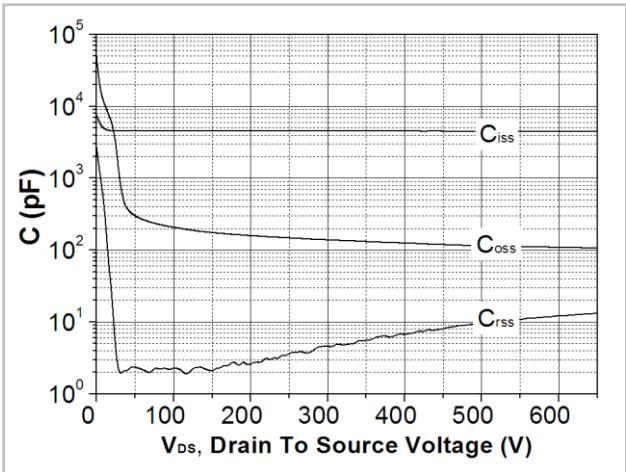
Fig. 9. Maximum safe operating area
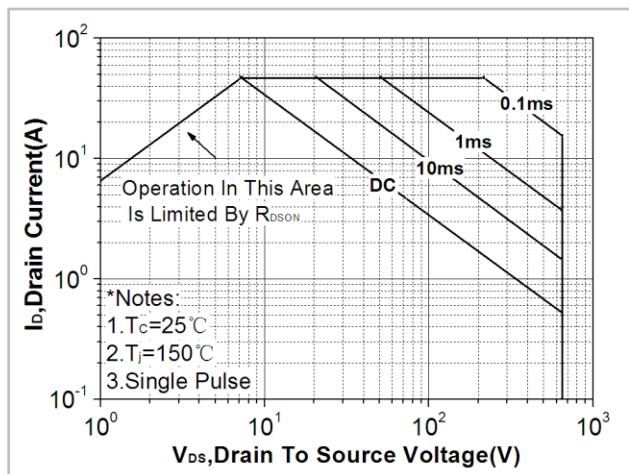
**Fig. 10. Transient thermal response curve**
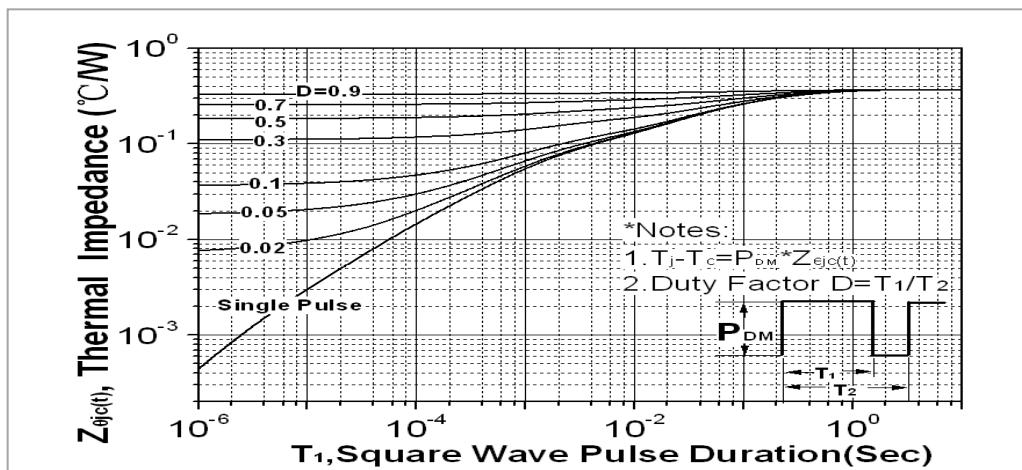
**Fig. 11. Gate charge test circuit & waveform**
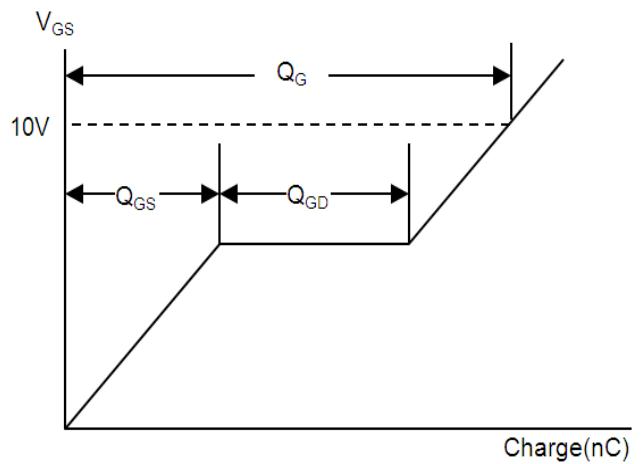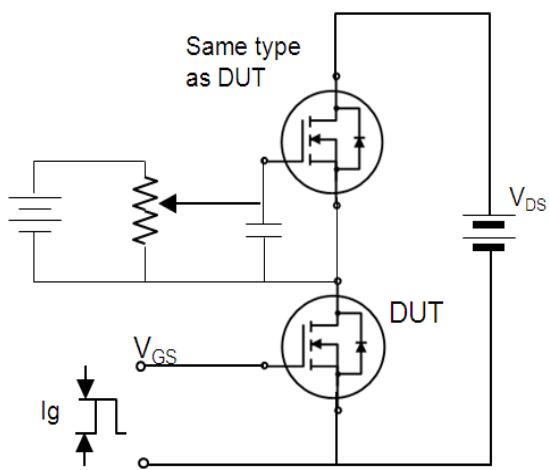

Fig. 12. Switching time test circuit & waveform
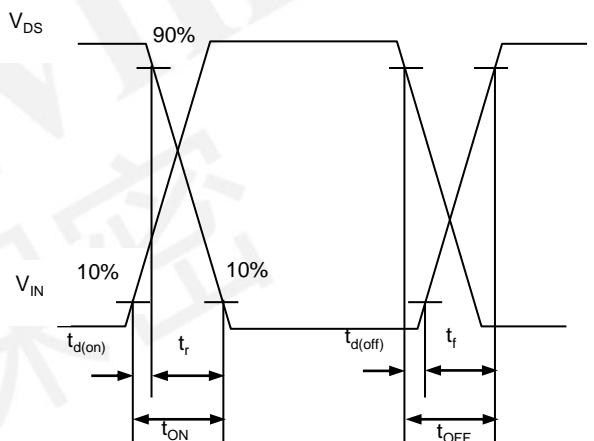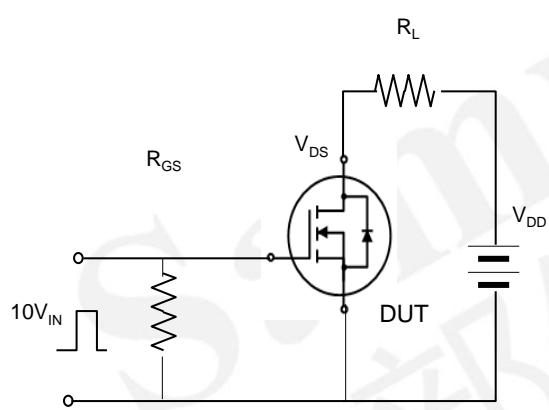
**Fig. 13. Unclamped Inductive switching test circuit & waveform**

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
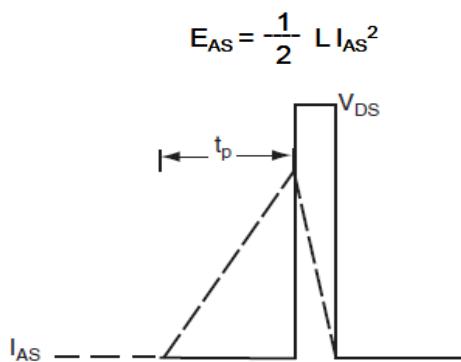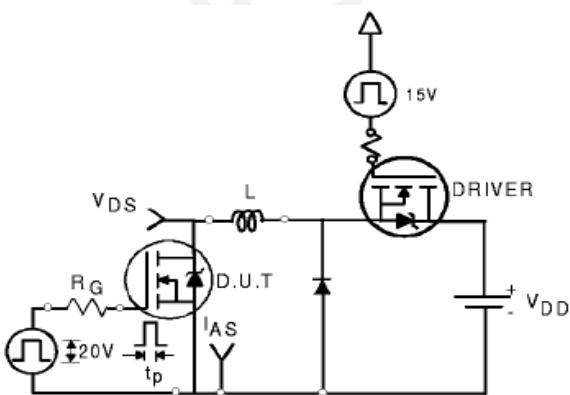
Fig. 14. Peak diode recovery dv/dt test circuit & waveform

*. dv/dt controlled by RG
*. Is controlled by pulse period
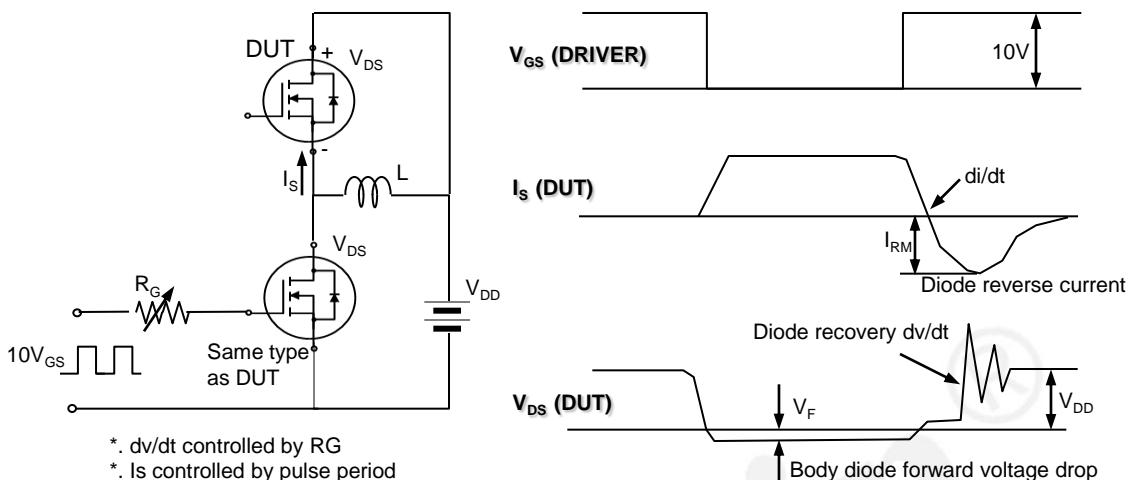
DISCLAIMER

* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.

* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.

* Qualification standards can also be found on the Web site (**http://www.semipower.com.**) ✉

* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**

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