

### General Description

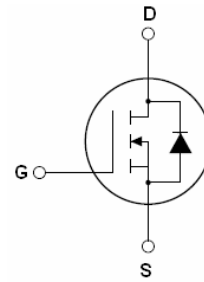
The 18N10. combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for power switching application.

### Features

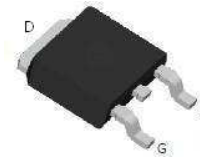
$V_{DSS}$	$R_{DS(ON)}$ @ 10V (typ)	$I_D$
100V	35m $\Omega$	18A

### Application

- Power switching application
- LED backlighting
- RoHS Compliant



Schematic Diagram



To-252

### Ordering Information

Part Number	Marking	Case	Packaging
18N10.	18N10.	TO-252	2500pcs/Reel

Table 1. Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ )

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-Source Voltage ( $V_{GS}=0V$ )	100	V
$V_{GS}$	Gate-Source Voltage ( $V_{DS}=0V$ )	$\pm 20$	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ\text{C}$	18	A
$I_{DM (pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	72	A
$P_D$	Maximum Power Dissipation ( $T_c=25^\circ\text{C}$ )	47	W
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	20	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ\text{C}$

Notes 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2.  $E_{AS}$  condition:  $T_J=25^\circ\text{C}$ ,  $V_{DD}=50V$ ,  $V_G=10V$ ,  $R_G=25\Omega$

**Table 2. Thermal Characteristic**

Symbol	Parameter	Value	Max	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	---	3.2	°C/W

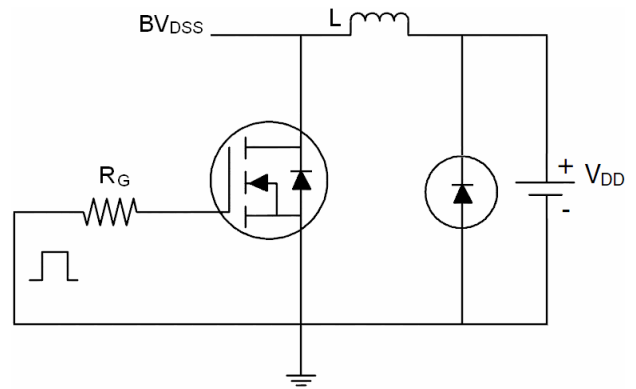
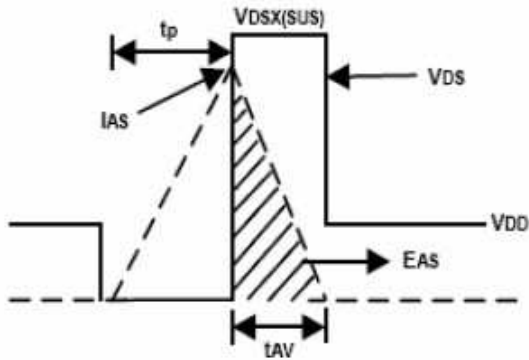
**Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current(Tc=25°C)	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	2.0	3.0	V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =1 A		38	55	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =1 A		35	45	mΩ
<b>Dynamic Characteristics</b>						
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =4.5A	5			S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V f=1.0MHz		1380		PF
C <sub>oss</sub>	Output Capacitance			88		PF
C <sub>rss</sub>	Reverse Transfer Capacitance			60		PF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =4.5A V <sub>GS</sub> =10V		26.8		nC
Q <sub>gs</sub>	Gate-Source Charge			6.4		nC
Q <sub>gd</sub>	Gate-Drain Charge			12.4		nC
<b>Switching Times</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =50V, R <sub>L</sub> =8.6Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω		7		nS
t <sub>r</sub>	Turn-on Rise Time			12		nS
t <sub>d(off)</sub>	Turn-Off Delay Time			24		nS
t <sub>f</sub>	Turn-Off Fall Time			11		nS
<b>Source-Drain Diode Characteristics</b>						
I <sub>SD</sub>	Source-Drain Current(Body Diode)			18		A
I <sub>SDM</sub>	Pulsed Source-Drain Current(Body Diode)			72		A
V <sub>SD</sub>	Forward On Voltage <sup>(Note 1)</sup>	T <sub>J</sub> =25°C, I <sub>SD</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
t <sub>rr</sub>	Reverse Recovery Time <sup>(Note 1)</sup>	T <sub>J</sub> =25°C, I <sub>F</sub> =4.5A di/dt=500A/μs		22		nS
Q <sub>rr</sub>	Reverse Recovery Charge <sup>(Note 1)</sup>			28		nC
t <sub>on</sub>	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

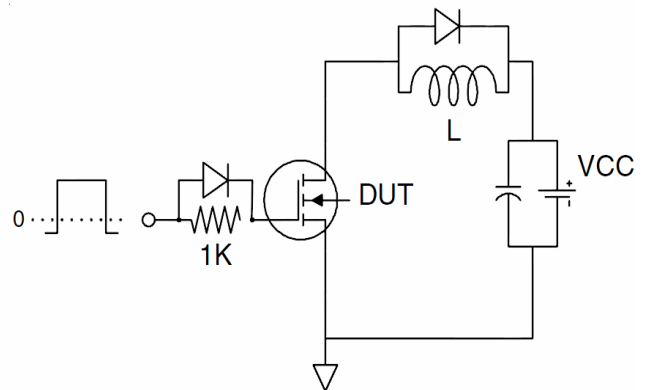
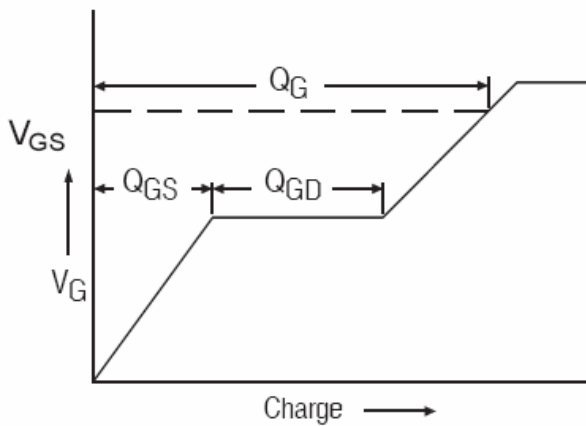
Notes 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, Starting T<sub>J</sub>=25°C

## Test Circuit

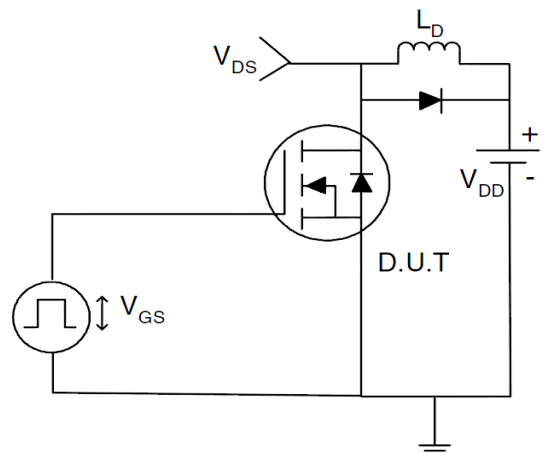
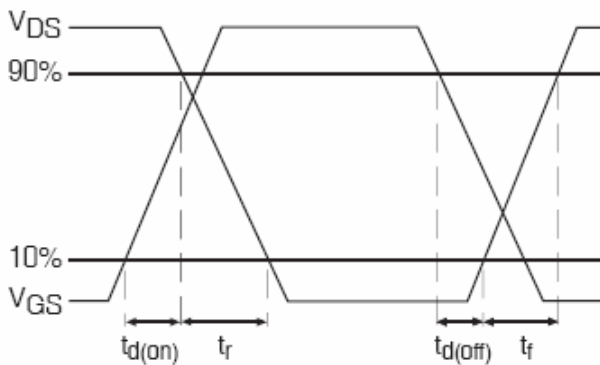
### 1) $E_{AS}$ Test Circuits



### 2) Gate Charge Test Circuit:



### 3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. On-Region Characteristics

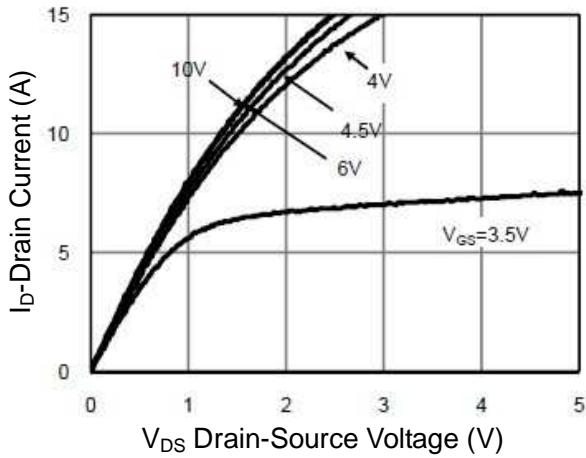


Figure 2: Transfer Characteristics

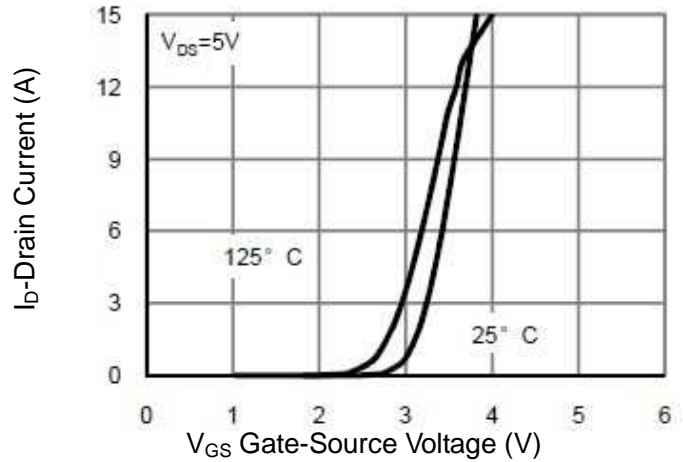


Figure3. ID vs Junction Temperature

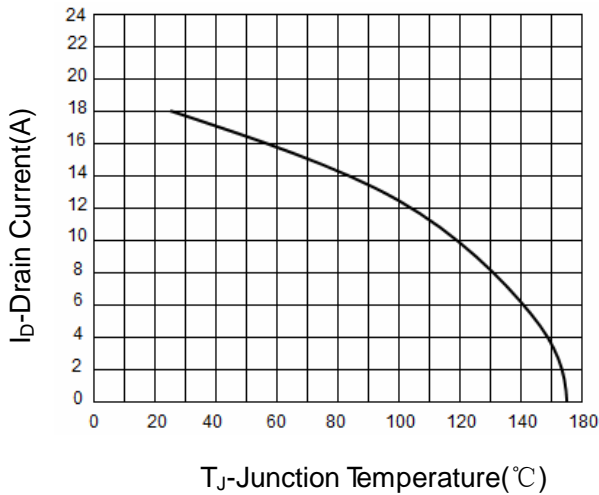


Figure4. On-Resistance vs. Junction Temperature

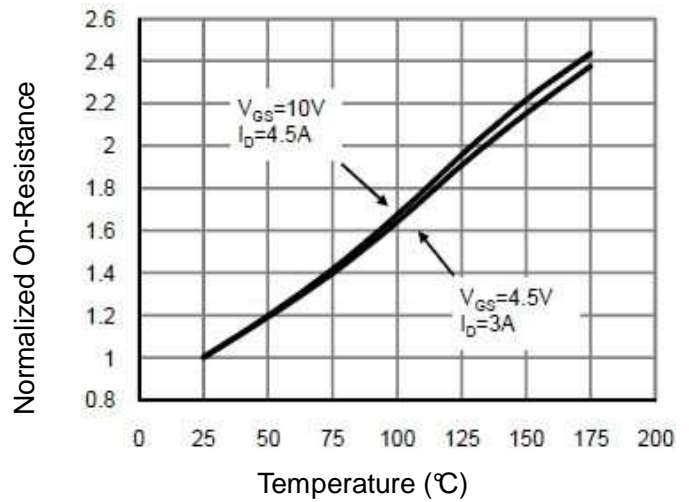


Figure5. On-Resistance vs. Gate-Source Voltage

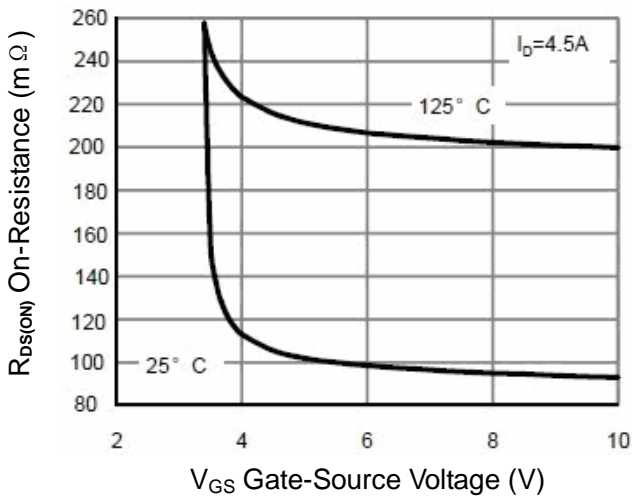


Figure6. Body-Diode Characteristics

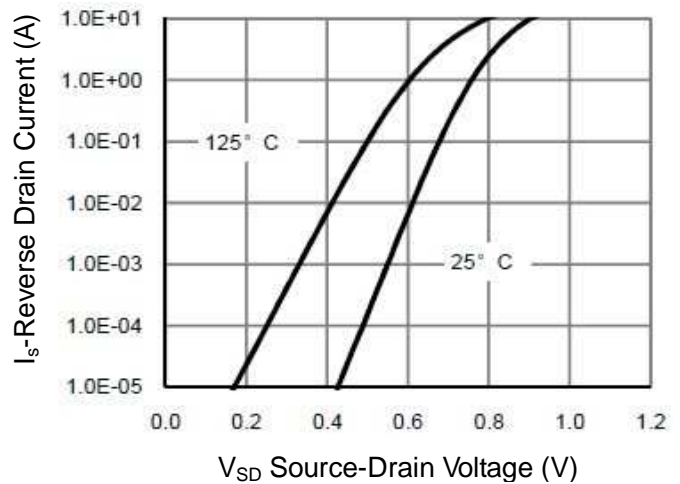


Figure7. Gate-Charge Characteristics

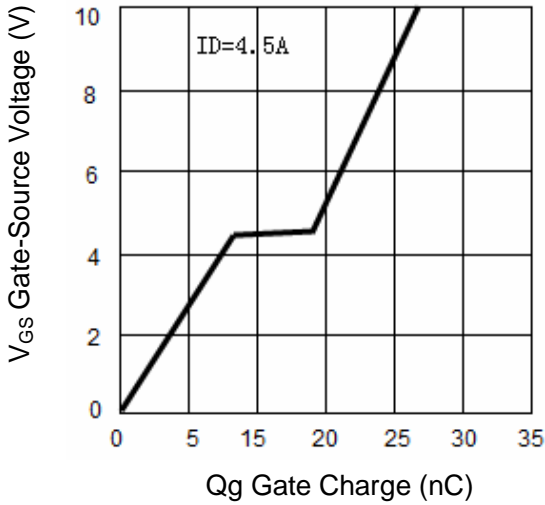


Figure 8. Capacitance Characteristics

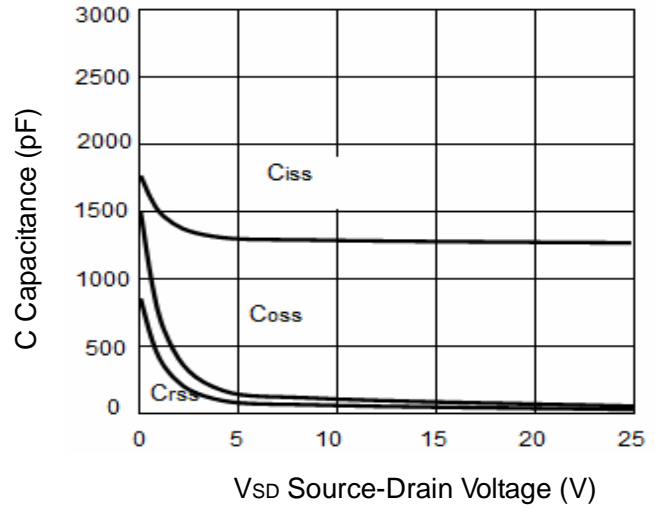


Figure 9. Maximum Forward Biased Safe Operating Area

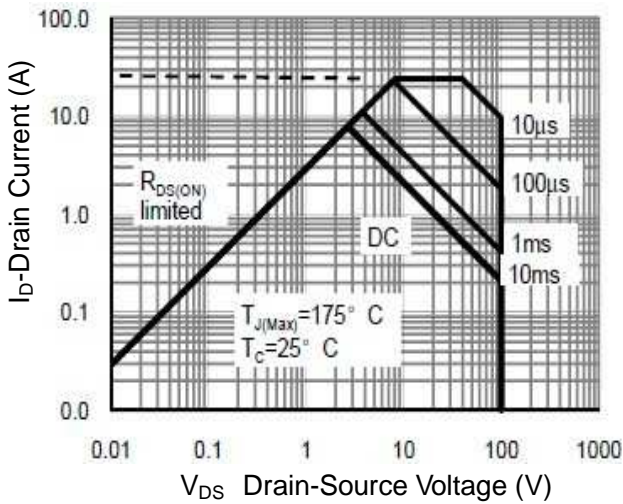


Figure10. Single Pulse Power Rating Junction-to-Case

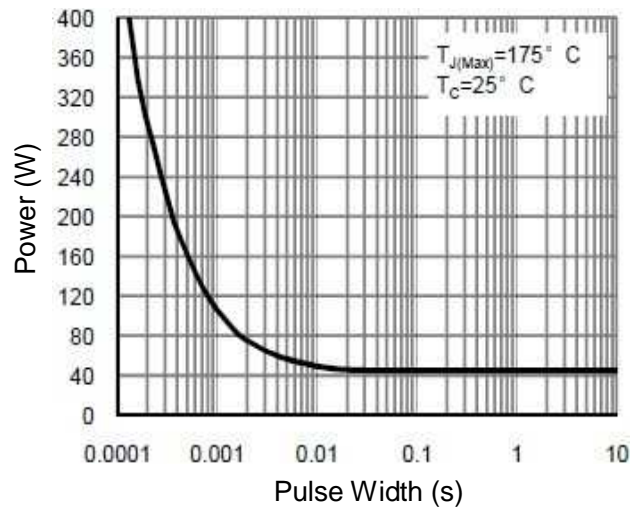
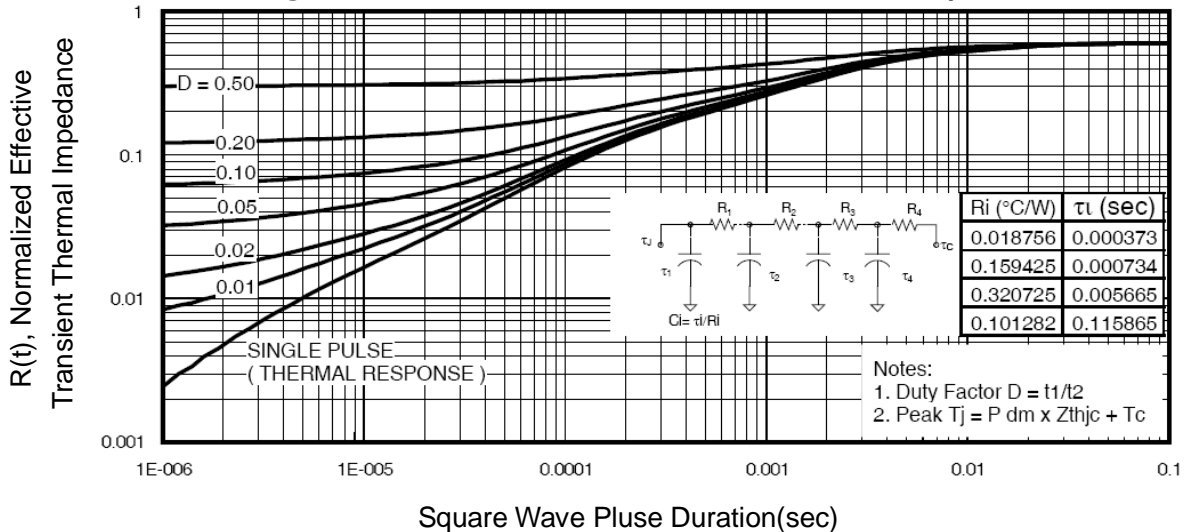
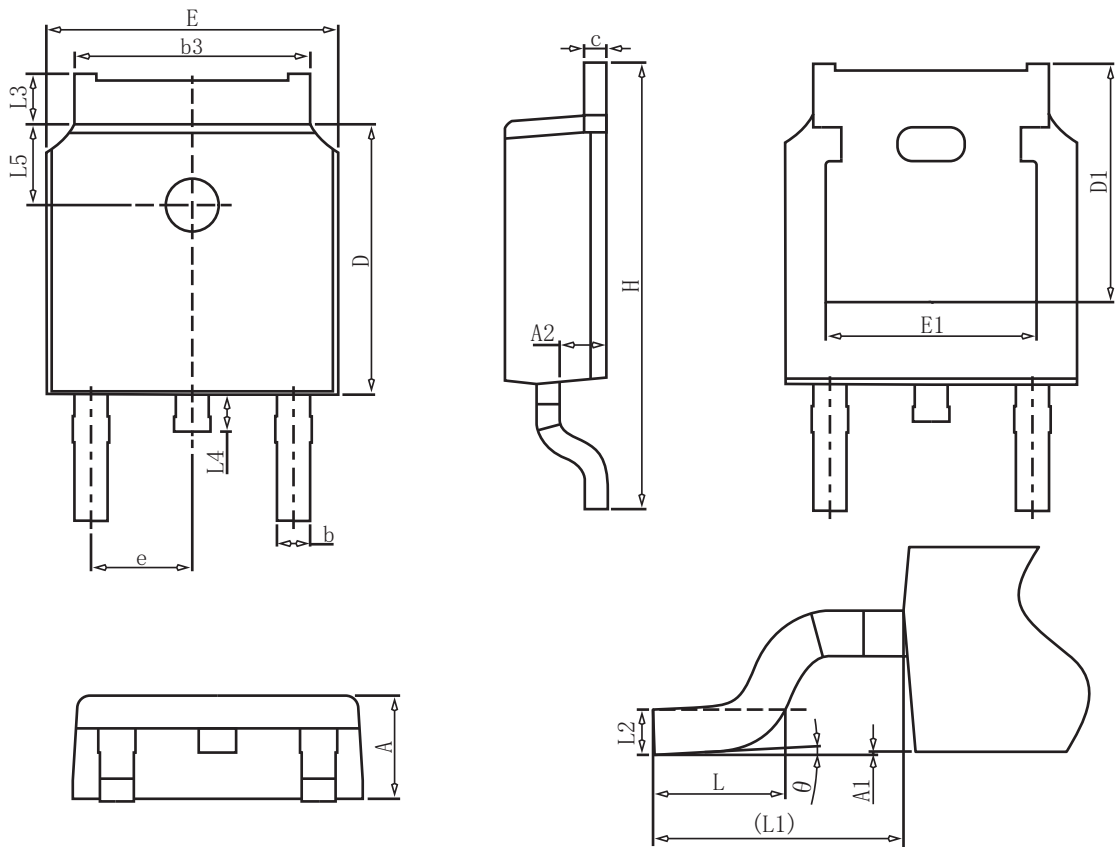


Figure11. Normalized Maximum Transient Thermal Impedance



**TO-252 Package information**



**COMMON DIMENSIONS**

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.80
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°

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