

Product Overview

The NSi810x devices are high reliability bidirectional isolators that are compatible with I²C interface. The NSi810x devices are AEC-Q100 qualified. The NSi810x devices are safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I²C clock of the NSi810x is up to 2MHz, and the common-mode transient immunity (CMTI) is up to 150kV/us. Wide supply voltage of the NSi810x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{RMS} Insulation voltage
- I²C Clock rate: up to 2MHz
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 qualified
- Suitable for hot swap applications
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
Enhanced system level ESD, EFT, Surge immunity
- Isolation Barrier Life: >60 years
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
SOIC-8 narrow body
SOIC-16 wide body

Safety Regulatory Approvals (pending)

- UL recognition: up to 5000V_{RMS} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval
IEC60950-1 standard
- DIN V VDE V 0884-10(VDE V 0884-10):
2006-12

Applications

- Power over Ethernet
- Isolated I²C, SMBus, or PMBus interface
- I²C level shifting
- Battery Management

Functional Block Diagrams

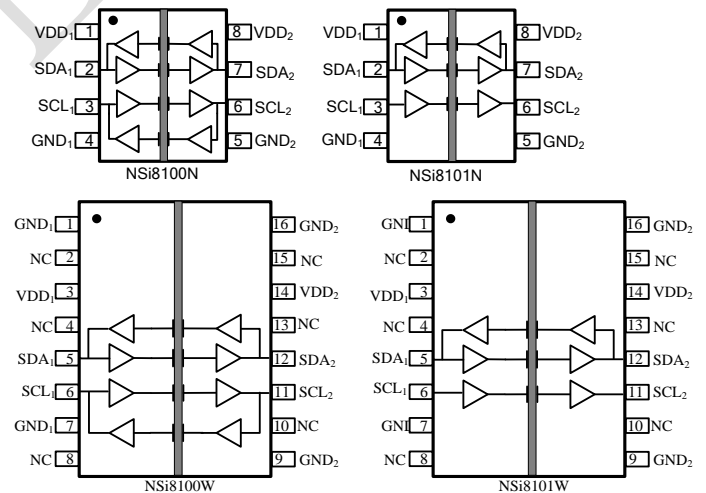


Figure1. NSi810x Functional Block Diagram

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CONFIDENTIAL

1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	SDA ₁ , SDA ₂ , SCL ₁ , SCL ₂	-0.4		VDD+0.4 ¹	V	
Maximum Input Pulse Voltage	SDA ₁ , SDA ₂ , SCL ₁ , SCL ₂	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±150	kV/us	
Output current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			5.3	kV	
Operating Temperature	T _{opr}	-40		125	°C	
Storage Temperature	T _{stg}	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

¹ The maximum voltage must not exceed 6.5V.

2.0 SPECIFICATIONS

2.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}		2.2		V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Start Up Time after POR	tr _{bs}		40		usec	
Common Mode Transient Immunity	CMTI	±100		±150	kV/us	
Side 1 Logic Level						
Input Threshold	V _{ILT1}	400			mV	Input Threshold at rising edge
	V _{IHT1}			600	mV	

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	V_{IT_HYS1}		100		mV	Input Threshold Hysteresis
Low Level Output Voltage	V_{OL1}	650		800	mV	$I_{OL} \leq 4mA$
Low-level output voltage to high-level input voltage threshold difference	ΔV_{OIT1}	70			mV	
Side 2 Logic Level						
Input Threshold	V_{ILT2}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS2}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH2}	2.0			V	
Low Level Input Voltage	V_{IL2}			0.8	V	
Low Level Output Voltage	V_{OL}			0.5	V	$I_{OL} \leq 30mA$

(VDD1=5V±10%, VDD2=5V±10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8100					
	$I_{DD1}(Q0)$		5.10	7.5	mA	All Input 0V
	$I_{DD2}(Q0)$		3.96	5.7	mA	
	$I_{DD1}(Q1)$		2.52	3.6	mA	All Input at supply
	$I_{DD2}(Q1)$		1.78	2.5	mA	
	$I_{DD1}(2M)$		3.83	5.7	mA	All Input with 2MHz, $C_L=15pF$
	$I_{DD2}(2M)$		2.78	4.2	mA	
	NSi8101					
	$I_{DD1}(Q0)$		2.85	4.2	mA	All Input 0V
	$I_{DD2}(Q0)$		2.66	4	mA	
	$I_{DD1}(Q1)$		2.42	3.6	mA	All Input at supply
	$I_{DD2}(Q1)$		1.57	2.4	mA	
	$I_{DD1}(2M)$		2.89	4.3	mA	All Input with 2MHz, $C_L=15pF$
	$I_{DD2}(2M)$		2.64	4	mA	
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		24.8	37.2	ns	See figure 2.6, $R1=1500\Omega$, $R2=500\Omega$, NO LOAD

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	t_{PHL12}		32.8	49.2	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PLH21}		24	36	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PHL21}		38	57	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
Pulse Width Distortion	PWD ₁₂		8	12	ns	$ t_{PHL12} - t_{PLH12} $
	PWD ₂₁		14	21	ns	$ t_{PHL21} - t_{PLH21} $
Falling Time	t_{f1}		10.6	15.9	ns	$C_L = 30\text{pF}$
	t_{f2}		22.8	34.2	ns	$C_L = 300\text{pF}$

(VDD1=3.3V \pm 10%, VDD2=3.3V \pm 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8100					
	$I_{DD1}(Q0)$		4.96	7.4	mA	All Input 0V
	$I_{DD2}(Q0)$		3.85	5.6	mA	
	$I_{DD1}(Q1)$		2.40	3.5	mA	All Input at supply
	$I_{DD2}(Q1)$		1.68	2.4	mA	
	$I_{DD1}(2M)$		3.69	5.6	mA	All Input with 2MHz, $C_L=15\text{pF}$
	$I_{DD2}(2M)$		2.67	4.2	mA	
	NSi8101					
	$I_{DD1}(Q0)$		2.79	4.2	mA	All Input 0V
	$I_{DD2}(Q0)$		2.58	3.9	mA	
	$I_{DD1}(Q1)$		2.60	3.9	mA	All Input at supply
	$I_{DD2}(Q1)$		1.50	2.3	mA	
	$I_{DD1}(2M)$		2.65	4	mA	All Input with 2MHz, $C_L=15\text{pF}$
	$I_{DD2}(2M)$		2.40	3.6	mA	
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		29	43.5	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD

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	t_{PHL12}		39.8	59.7	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PLH21}		30	45	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PHL21}		61	91.5	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
Pulse Width Distortion	PWD ₁₂		10.8	16.2	ns	$ t_{PHL12} - t_{PLH12} $
	PWD ₂₁		31	46.5	ns	$ t_{PHL21} - t_{PLH21} $
Falling Time	t_{f1}		15.6	23.4	ns	$C_L = 30\text{pF}$
	t_{f2}		32	48	ns	$C_L = 300\text{pF}$

(VDD1=2.5V \pm 10%, VDD2=2.5V \pm 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8100					
	$I_{DD1}(Q0)$		4.89	7.3	mA	All Input 0V
	$I_{DD2}(Q0)$		3.79	5.5	mA	
	$I_{DD1}(Q1)$		2.34	3.4	mA	All Input at supply
	$I_{DD2}(Q1)$		1.63	2.3	mA	
	$I_{DD1}(2M)$		3.61	5.4	mA	All Input with 2MHz, $C_L=15\text{pF}$
	$I_{DD2}(2M)$		2.59	4	mA	
	NSi8101					
	$I_{DD1}(Q0)$		2.75	4	mA	All Input 0V
	$I_{DD2}(Q0)$		2.54	3.8	mA	
	$I_{DD1}(Q1)$		2.57	3.9	mA	All Input at supply
	$I_{DD2}(Q1)$		1.47	2.2	mA	
$I_{DD1}(2M)$		2.57	3.9	mA	All Input with 2MHz, $C_L=15\text{pF}$	
$I_{DD2}(2M)$		2.29	3.5	mA		
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		33	49.5	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD

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	t_{PHL12}		52	78	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PLH21}		47	70.5	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
	t_{PHL21}		100	150	ns	See figure 2.6, R1=1500 Ω , R2=500 Ω , NO LOAD
Pulse Width Distortion	PWD_{12}		19	28.5	ns	$ t_{PHL12} - t_{PLH12} $
	PWD_{21}		53	79.5	ns	$ t_{PHL21} - t_{PLH21} $
Falling Time	t_{f1}		22	33	ns	$C_L = 30\text{pF}$
	t_{f2}		36	54	ns	$C_L = 300\text{pF}$

2.2. TYPICAL PERFORMANCE CHARACTERISTICS

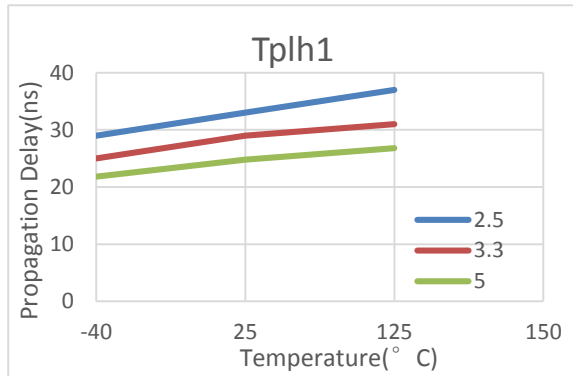


Figure 2.1 Rising Edge Propagation Delay Vs Temp

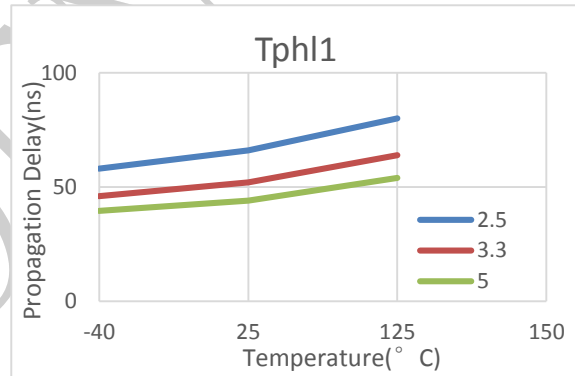


Figure 2.2 Falling Edge Propagation Delay Vs Temp

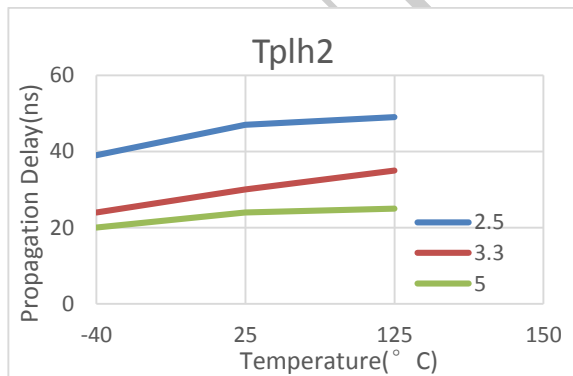


Figure 2.3 Rising Edge Propagation Delay Vs Temp

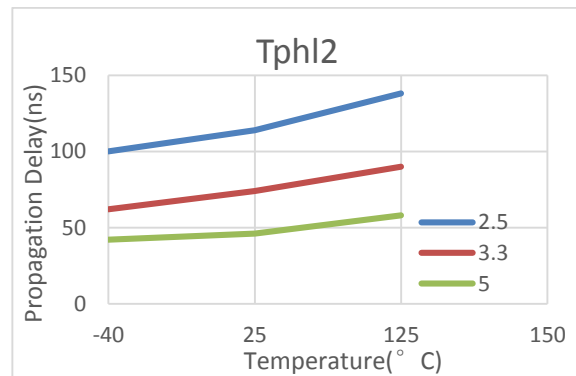


Figure 2.4 Falling Edge Propagation Delay Vs Temp

NSi8100/NSi8101

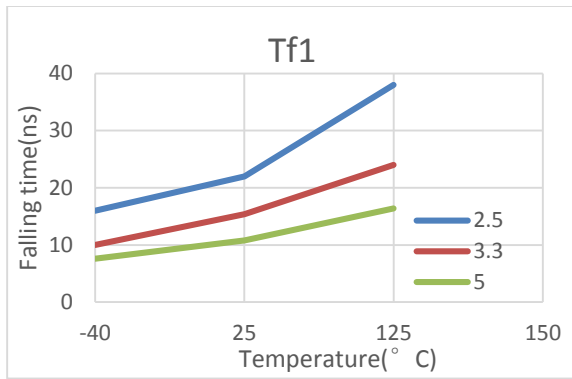


Figure 2.5 falling time(@27pF) Vs Temp

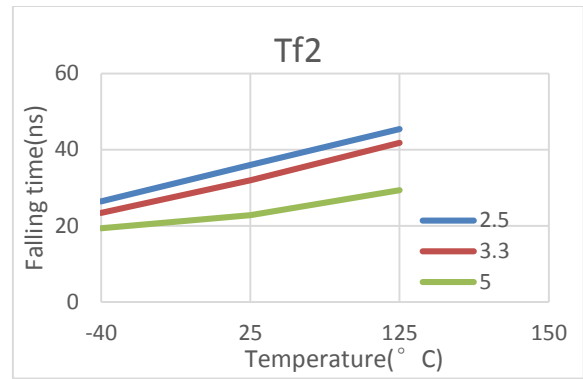


Figure 2.6 Falling time(@300pF) Vs Temp

2.3. PARAMETER MEASUREMENT INFORMATION

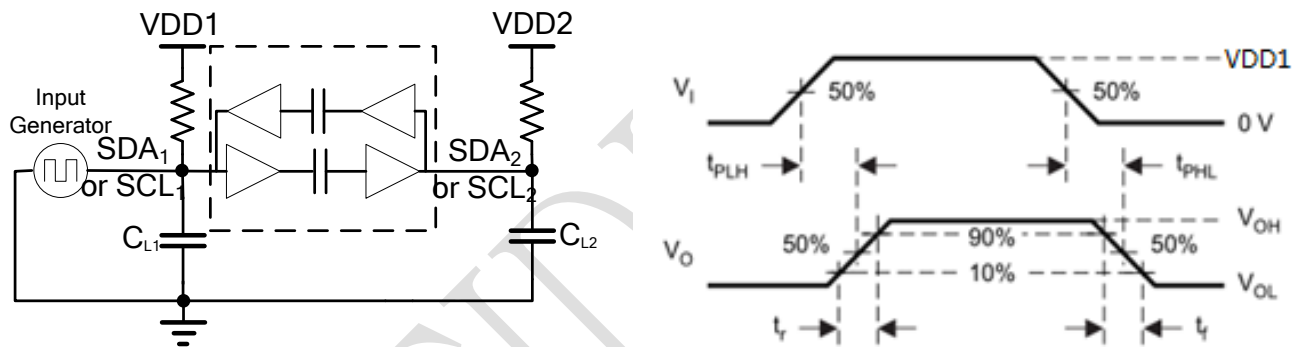


Figure 2.6 Switching Characteristic Test Circuit and Voltage Waveforms

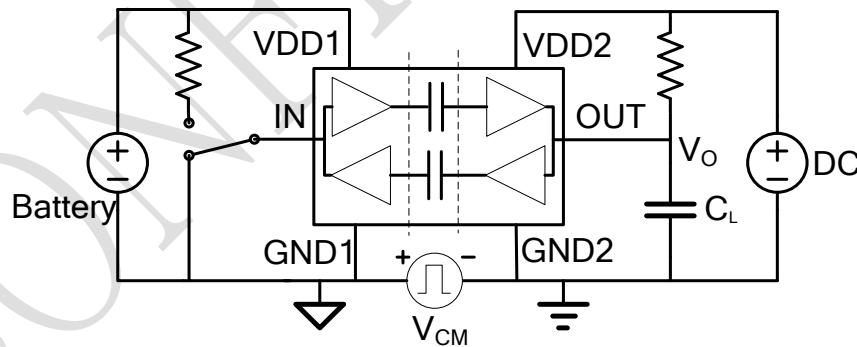


Figure 2.7 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value	Unit	Comments
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NSi8100/NSi8101

		SOIC-8	SOIC-16		
Minimum External Air Gap (Clearance)	L(I01)	4.0	7.8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	7.8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			

3.2. DIN VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

Description	Test Condition	Symbol	Value		Unit
			SOIC-8	SOIC-16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to III	I to IV	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	I to IV	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		V_{IORM}	565	800	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	1200	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	960	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	960	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	V_{IOTM}	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.6 \times V_{IOSM}$	V_{IOSM}	5384	5384	Vpeak
Isolation resistance	$V_{IO}=500V$	R_{IO}	$>10^9$	$>10^9$	Ω

NSi8100/NSi8101

Isolation capacitance	$f = 1\text{MHz}$	C_{IO}	0.6	0.6	pF
Input capacitance		C_I	2	2	pF
Total Power Dissipation at 25°C		P_s		1499	mW
Safety input, output, or supply current	$\theta_{JA} = 140\text{ }^\circ\text{C/W}$, $V_I = 5.5\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$, $T_A = 25\text{ }^\circ\text{C}$	I_s	160		mA
	$\theta_{JA} = 84\text{ }^\circ\text{C/W}$, $V_I = 5.5\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$, $T_A = 25\text{ }^\circ\text{C}$			237	mA
Case Temperature		T_s	150	150	°C

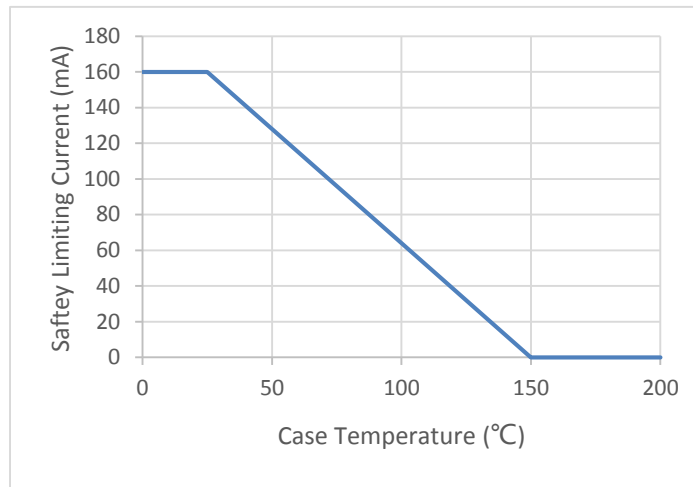


Figure 3.1 NSi8100N/NSi8101N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

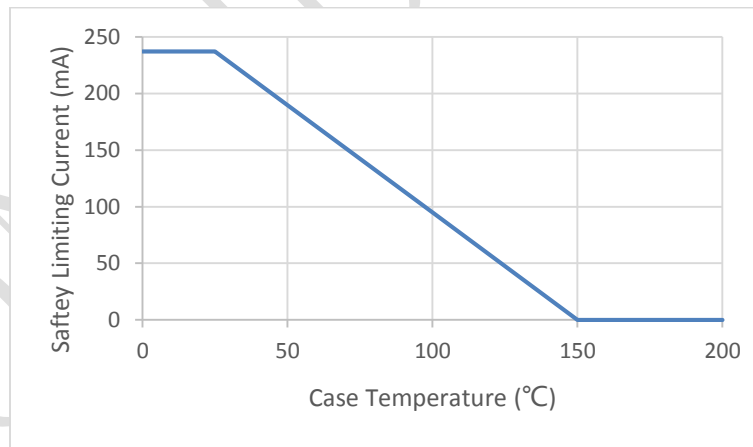


Figure 3.2 NSi8100W/NSi8101W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

3.3. REGULATORY INFORMATION

The NSi8100N/NSi8101N are approved or pending approval by the organizations listed in table.

UL	CSA	VDE	CQC
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V0884-10 (VDE V 0884-	Certified by CQC11-471543-2012

NSi8100/NSi8101

	IEC60950-1	10):2006-12 ²	GB4943.1-2011
Single Protection, 3750Vrms Isolation voltage	400V _{RMS} basic insulation working voltage	Basic Insulation 565Vpeak, V _{IOSM} =6000Vpeak	Basic insulation at 400V _{RMS} (565Vpeak)
File (E500602)	File (pending)	File (pending)	File (pending)

¹ In accordance with UL 1577, each NSi8100N/NSi8101N is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each NSi8100N/NSi8101N is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

The NSi8100W/NSi8101W are approved or pending approval by the organizations listed in table.

UL	CSA	VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	800V _{RMS} basic insulation working voltage 400V _{RMS} Reinforced insulation working voltage	Basic Insulation 800Vpeak, V _{IOSM} =5384Vpeak	Basic insulation at 800V _{RMS} (1131Vpeak) Reinforced insulation at 400V _{RMS} (565Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

¹ In accordance with UL 1577, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

4.0 FUNCTION DESCRIPTION

The NSi810x is a bidirectional isolator based on a capacitive isolation barrier technique. The NSi810x devices are compatible with I²C interface. Internally, the I²C interface is split into two unidirectional channels communicating in opposing directions via a dedicated capacitive isolation channel for each. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi8100 devices are high reliability dual-channel bidirectional isolators for clock and data lines while NSi8101 has a bidirectional data and a unidirectional clock channel. The NSi8100 is suitable for multi-master application while NSi8101 is useful in a single master application.

The Side 2 logic levels of NSi810x are standard I²C value, and the maximum load for side 2 is ≤ 400 pF. So multiple NSi810x devices connected to a bus by their Side 2 pins can communicate with each other and with other I²C compatible devices.

The Side 1 logic levels of NSi810x are not standard value. The output low level of NSi810x is 650mV, while low-level output voltage to high-level input voltage threshold is 50mV. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I²C bus.

The NSi810x devices are AEC-Q100 qualified. The NSi810x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I²C clock of the NSi810x is up to 2MHz, and the common-mode transient immunity (CMTI) is up to 150kV/us. Wide supply voltage of the NSi810x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The Table 4.1 shows the functional of NSi810x. The NSi810x is high impedance output when VDDIN is unready and VDDOUT is ready as shown in.

Table 4.1 Output status vs. power status

Input	VDD1	VDD2	Output	Comment
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NSi8100/NSi8101

status		status		
H	Ready	Ready	Z	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	Z	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

5.0 APPLICATION NOTE

5.1. PCB LAYOUT

The NSi810x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. The pull-up resistors required for both Side 1 and Side 2 buses. And the value of the resistors depend on the number of I²C devices on the bus.

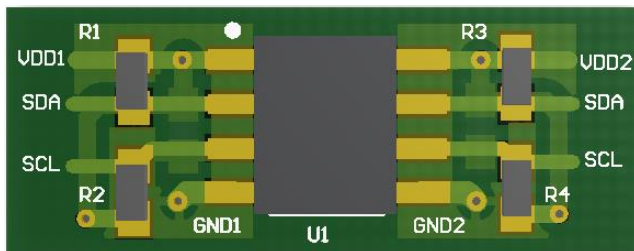


Figure5.1 Recommended PCB Layout — Top Layer



Figure5.2 Recommended PCB Layout — Bottom Layer

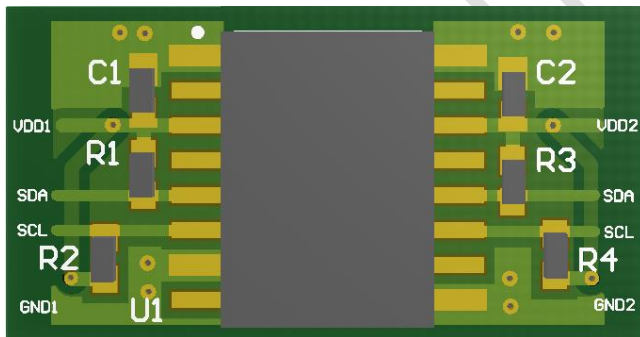


Figure5.3 Recommended PCB Layout — Top Layer

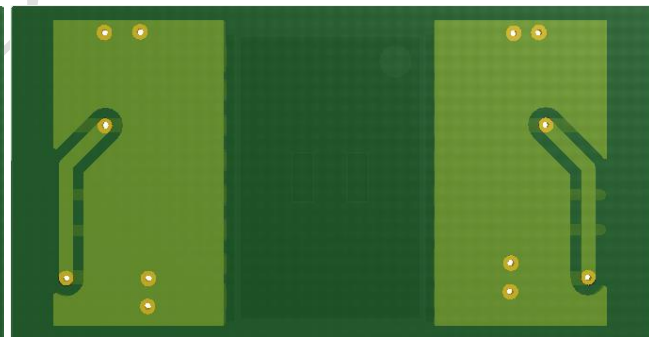


Figure5.4 Recommended PCB Layout — Bottom Layer

6.0 PACKAGE INFORMATION

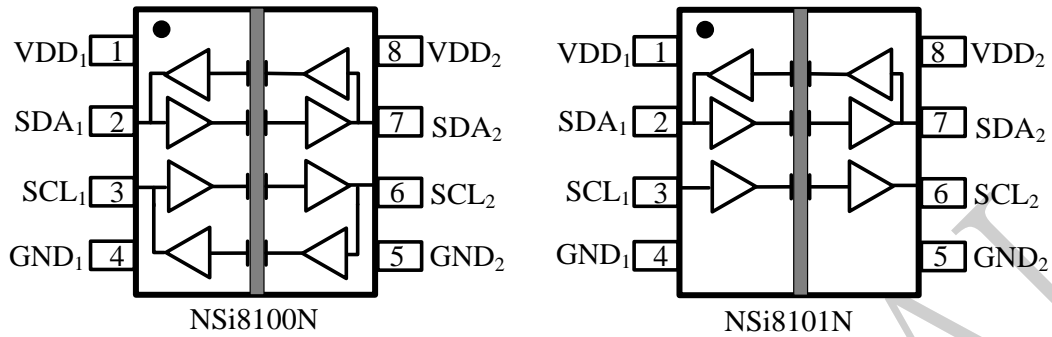


Figure 6.1 NSi8100N/NSi8101N Package

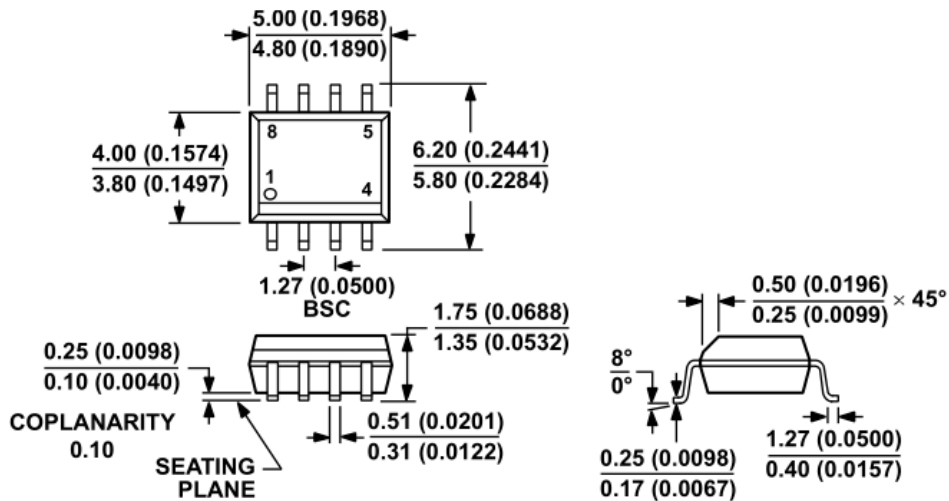


Figure 6.3 SOIC8 Package Shape and Dimension

Dimensions shown in millimeters and (inches)

Table 6.1 NSi8100N/ NSi8101N Pin Configuration and Description

<i>NSi8100N</i> <i>PIN NO.</i>	<i>NSi8101N</i> <i>PIN NO.</i>	<i>SYMBOL</i>	<i>FUNCTION</i>
1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	SDA ₁	Serial data input /output, Side 1
3	3	SCL ₁	Serial clock input /output, Side 1
4	4	GND ₁	Ground 1, the ground reference for Isolator Side 1
5	5	GND ₂	Ground 2, the ground reference for Isolator Side 2
6	6	SCL ₂	Serial clock input /output, Side 2
7	7	SDA ₂	Serial data input /output, Side 2
8	8	VDD ₂	Power Supply for Isolator Side 2

NSi8100/NSi8101

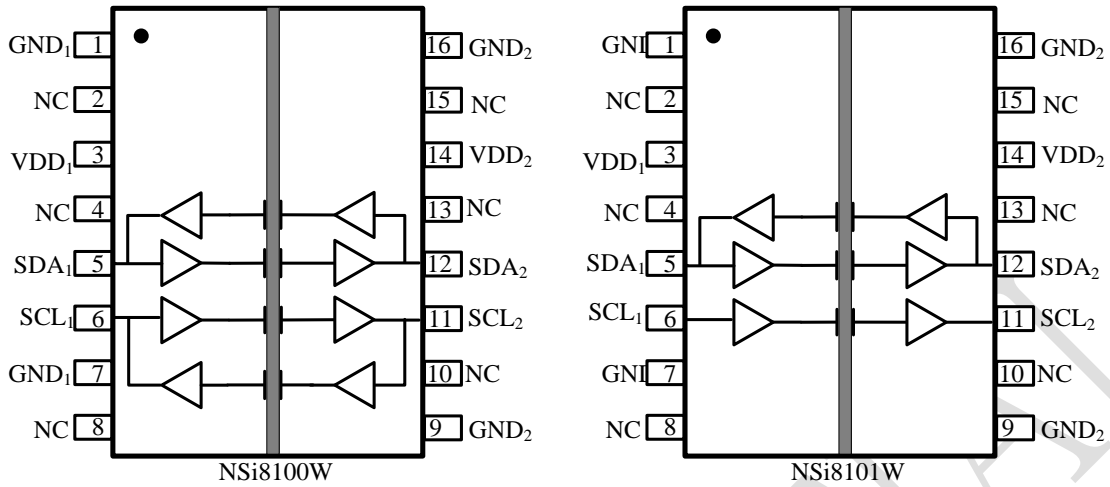


Figure 6.2 NSi8100W/ NSi8101W Package

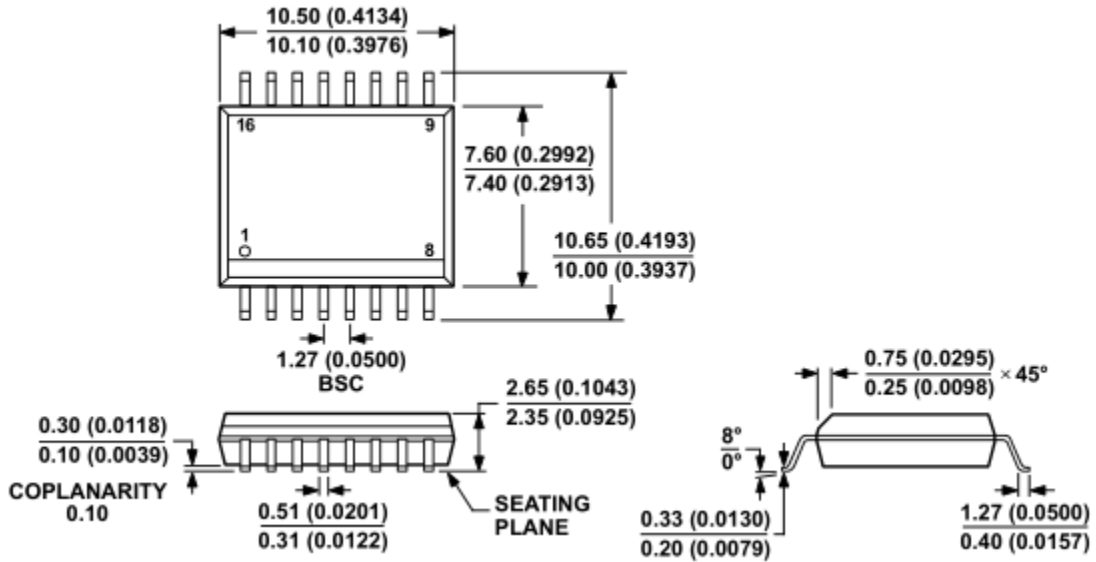


Figure 6.6 SOIC16 Package Shape and Dimension
Dimensions shown in millimeters and (inches)

Table 6.2 NSi8100W/ NSi8101W Pin Configuration and Description

NSi8100W PIN NO.	NSi8101W PIN NO.	SYMBOL	FUNCTION
1	1	GND ₁	Ground 1, the ground reference for Isolator Side 1
2	2	NC	No Connection.
3	3	VDD ₁	Power Supply for Isolator Side 1
4	4	NC	No Connection.
5	5	SDA ₁	Serial data input /output, Side 1
6	6	SCL ₁	Serial clock input /output, Side 1
7	7	GND ₁	Ground 1, the ground reference for Isolator Side 1

NSi8100/NSi8101

8	8	NC	No Connection.
9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	10	NC	No Connection.
11	11	SCL ₂	Serial clock input /output, Side 1
12	12	SDA ₂	Serial data input /output, Side 1
13	13	NC	No Connection.
14	14	VDD ₂	Power Supply for Isolator Side 2
15	15	NC	No Connection.
16	16	GND ₂	Ground 2, the ground reference for Isolator Side 2

7.0 ORDER INFORMATION

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Clock Rate (MHz)	Temperature	Automotive	Package
NSi8100N	3.75	2	2	2	-40 to 125 °C	NO	SOIC8
NSi8100NQ	3.75	2	2	2	-40 to 125 °C	YES	SOIC8
NSi8101N	3.75	2	1	2	-40 to 125 °C	NO	SOIC8
NSi8101NQ	3.75	2	1	2	-40 to 125 °C	YES	SOIC8
NSi8100W	5	2	2	2	-40 to 125 °C	NO	WB SOIC16
NSi8101W	5	2	1	2	-40 to 125 °C	NO	WB SOIC16

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ° C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

8.0 REVISION HISTORY

Revision	Description	Date
1.0	Original	2017/11/15
1.1	Change to Ordering information	2018/3/26
1.2	Add maximum operation current specification.	2018/6/20
1.3	Change block diagram	2018/7/28
1.4	Change "Start Up Time after POR" specification to 40us	2018/8/25
1.5	Add "Maximum Input Pulse Voltage"	2018/10/9
1.6	Change to Ordering information	2018/12/20

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[3E](#) [IL3685E](#) [IL514E](#)