Product Preview

Low Voltage 2.5V and 3.3V CMOS PLL Clock Driver

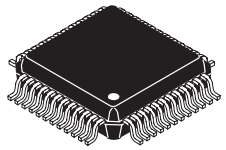
MPC9600

LOW VOLTAGE CMOS PLL CLOCK DRIVER

The MPC9600 is a low voltage 2.5V and 3.3V compatible, 1:21 PLL based clock driver and fanout buffer. With output frequencies up to 200 MHz, output skews of 150 ps and part–to–part skews of 300 ps the device meets the needs of the most demanding clock tree applications.

Features:

- Multiplication of input frequency by 2, 3, 4 and 6
- Distribution of output frequency to 21 outputs organized in three output banks: QA0-QA6, QB0-QB6, QC0-QC6, each fully selectable
- Fully integrated PLL
- Selectable output frequency range is 50 to 100 MHz and 100 to 200 MHz
- Selectable input frequency range is 16 to 33 MHz and 25 to 50 MHz
- LVCMOS outputs
- Outputs disable to high impedance (except QFB)
- LVCMOS or LVPECL reference clock options
- 48 lead QFP packaging
- ±50 ps cycle-to-cycle jitter
- 150 ps maximum output-to-output skew
- 300 ps maximum device-to-device skew



FA SUFFIX
48–LEAD LQFP PACKAGE
CASE 932–03

The MPC9600 is fully 2.5V and 3.3V compatible. The MPC9600 has the capability to generate clock signals of 50 to 200 MHz from clock sources of 16 to 50 MHz. The internal PLL is optimized for this frequency range and does not require external loop filter components. QFB provides an output for the external feedback path to the feedback input FB_IN. The QFB divider ratio is configurable and determines the PLL frequency multiplication factor when QFB is directly connected to FB_IN. The MPC9600 is optimized for minimizing the propagation delay between the clock input and FB_IN.

Three output banks of 7 outputs each bank can be individually configured to divide the VCO frequency by 2 or by 4. Combining the feedback and output divider ratios, the MPC9600 is capable to multiply the input frequency by 2, 3, 4 and 6.

The reference clock is selectable either LVPECL or LVCMOS. The LVPECL reference clock feature allows the designer to use LVPECL fanout buffers for the inner branches of the clock distribution tree. All control inputs accept LVCMOS compatible levels. The outputs provide low impedance LVCMOS outputs capable of driving parallel terminated 50Ω transmission to $V_{TT}=V_{CC}/2$. For series terminated lines the MPC9600 can drive two lines per output giving the device and effective total fanout of 1:42. With guaranteed maximum output-to-output skew of 150 ps, the MPC9600 PLL clock driver meets the synchronization requirements of the most demanding systems.

The V_{CCA} analog power pin doubles as a PLL bypass select line for test purpose. When the V_{CCA} is driven to GND the reference clock will bypass the PLL and will drive the outputs (except QFB) into a high impedance state.

The device is packaged in a 48-lead LQFP package to provide optimum combination of board density and performance.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

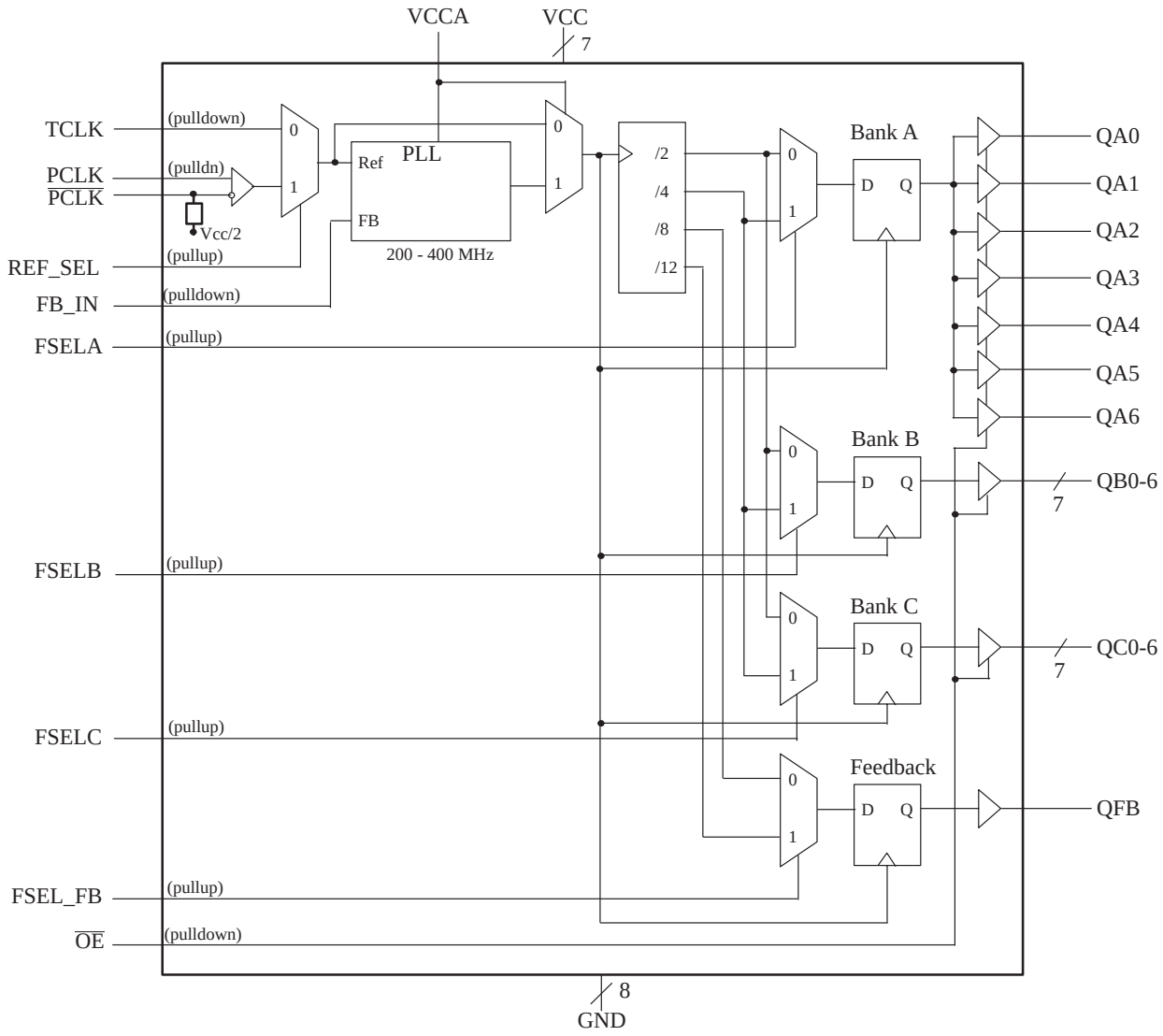


Figure 1. MPC9600 Logic Diagram

PIN CONFIGURATION

Pin	I/O	Type	Description
PCLK, PCLK	Input	PECL	Differential reference clock frequency input
TCLK	Input	LVCMOS	Reference clock input
FB_IN	Input	LVCMOS	PLL feedback clock input
QAn	Output	LVCMOS	Bank A outputs
QBn	Output	LVCMOS	Bank B outputs
QCn	Output	LVCMOS	Bank C outputs
QFB	Output	LVCMOS	Differential feedback output
REF_SEL	Input	LVCMOS	Reference clock input select
FSELA	Input	LVCMOS	Selection of bank A output frequency
FSELB	Input	LVCMOS	Selection of bank B output frequency
FSELC	Input	LVCMOS	Selection of bank C output frequency
FSEL_FB	Input	LVCMOS	Selection of feedback frequency
OE	Input	LVCMOS	Output enable
VCCA		Power supply	Analog power supply and PLL bypass
VCC		Power supply	Core power supply
GND		Ground	Ground

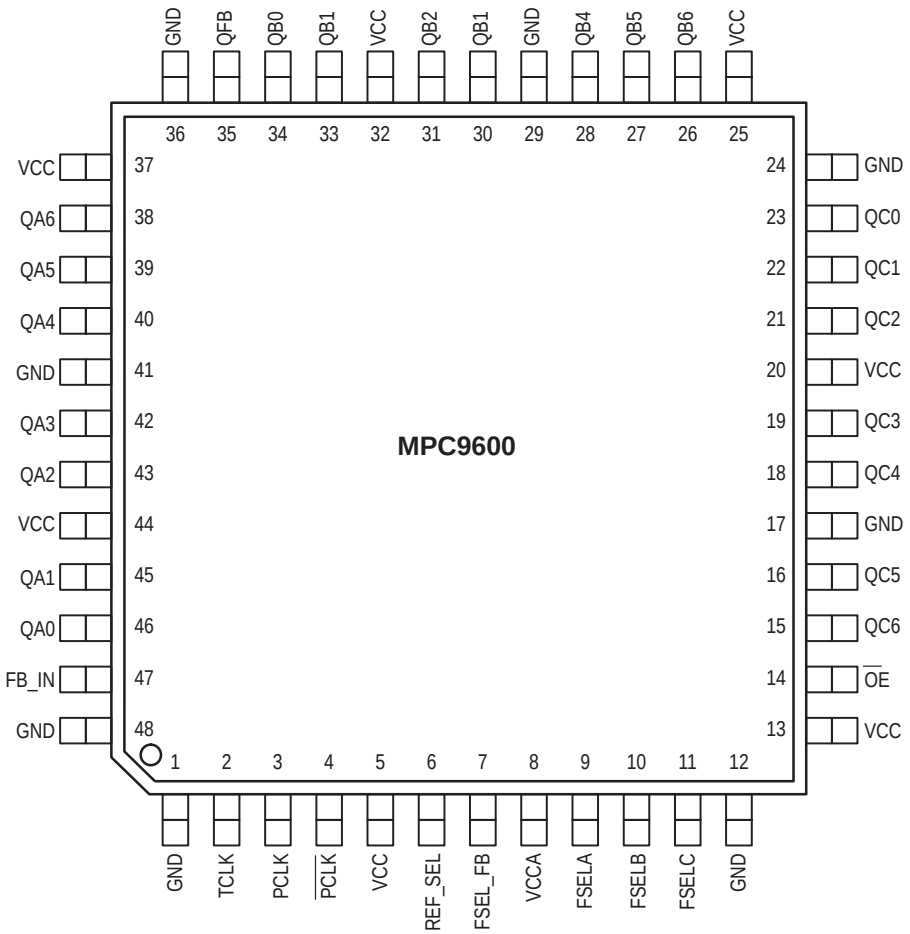


Figure 2. 48 Lead Package Pinout (Top View)

FUNCTION TABLE (CONTROLS)

Control Pin	0	1
REF_SEL	TCLK	PCLK
VCCA	PLL Bypass	PLL Power
OE	Outputs Enabled	Outputs Disabled (except QFB)
FSELA	Output Bank A at VC0/2	Output Bank A at VCO/4
FSELB	Output Bank B at VC0/2	Output Bank B at VCO/4
FSELC	Output Bank C at VC0/2	Output Bank C at VCO/4
FSEL_FB	Feedback Output at VCO/8	Feedback Output at VCO/12

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	-0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage[a] PCLK, PCLK	 500		 1000	 mV	 LVPECL
V_{CMR}[b]	Common Mode Range[c] PCLK, PCLK	 V_{CC}-1.4		 V_{CC}-0.6	 V	 LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[d]
V_{OL}	Output Low Voltage			0.55	V	I_{OL}= 24mA
I_{IN}	Input Current			±120	µA	
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		25		pF	Per Output
I_{CCA}	Maximum PLL Supply Current		15	20	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins

a. Pending characterization
b. V_{CMR} is the difference from V_{CC} and the most positive side of the differential input signal. Normal operation is obtained when the “high” input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
c. Pending characterization
d. The MPC9600 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT} = V_{CC}/2$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency FSEL_FB=1 FSEL_FB=0	 16 25		 33 50	 MHz MHz	
f_{MAX}	Maximum Output Frequency FSEL_FB=1 FSEL_FB=0	 100 50		 200 100	 MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_{PD}	Propagation Delay Input to QFB (PLL locked)	X -100	X	X+100	ps	
$t_{sk(o)}$	Output-to-output Skew			150	ps	
$t_{sk(pp)}$	Part-to-part Skew			300	ps	
t_{PW}	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.0V
$t_{PLZ, HZ}$	Output Disable Time				ns	
t_{PZL}	Output Enable Time				ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter (Peak-to-Peak)		±50			
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. AC characterisitics apply for parallel output termination of 50Ω to $V_{TT} = V_{CC}/2$

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		V_{CC} + 0.3	V	LVCMOS[a]
V_{IL}	Input low voltage	-0.3		0.7	V	LVCMOS[b]
V_{PP}	Peak-to-peak input voltage PCLK, PCLK	500		1000	mV	LVPECL
V_{CMR}[c]	Common Mode Range PCLK, PCLK	V_{CC}-1.4		V_{CC}-0.6	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	I_{OH}=-15 mA[d]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15 mA
I_{IN}	Input Current				µA	
C_{IN}	Input capacitance				pF	
C_{PD}	Power Dissipation Capacitance				pF	Per Output
I_{CCA}	Maximum PLL Supply Current				mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins

a. The MPC9600 inputs are CMOS-type inputs with a threshold of 30% of V_{CC}
b. The MPC9600 inputs are CMOS-type inputs with a threshold of 30% of V_{CC}
c. V_{CMR} is the difference from V_{CC} and the most positive side of the differential input signal. Normal operation is obtained when the “high” input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
d. The MPC9600 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT} = V_{CC}/2$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

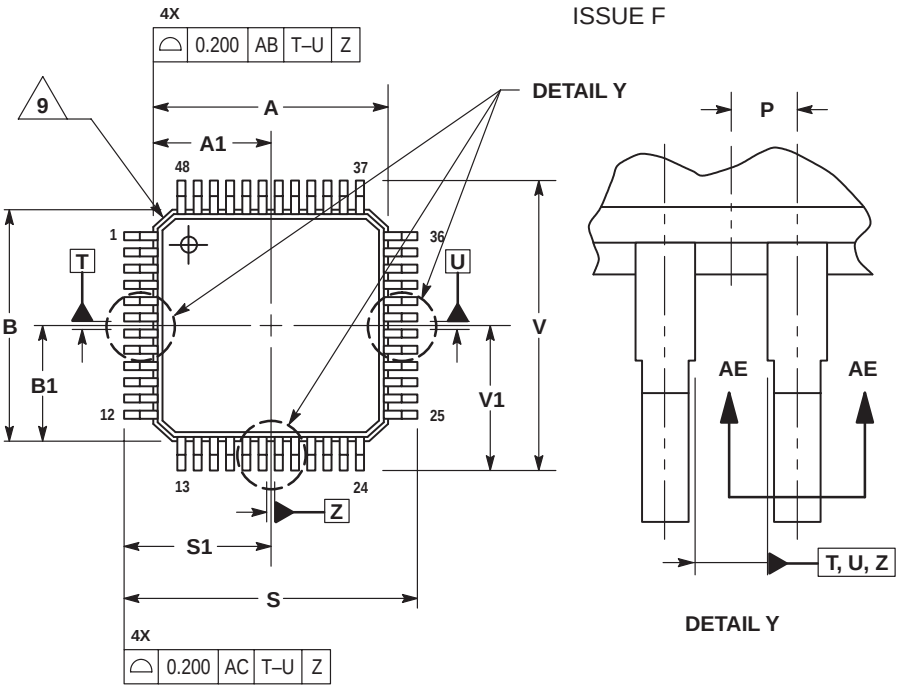
AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency FSEL_FB=1 FSEL_FB=0	 16 25		 33 50	 MHz MHz	
f_{MAX}	Maximum Output Frequency FSEL_FB=1 FSEL_FB=0	 100 50		 200 100	 MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_{PD}	Propagation Delay Input to QFB (PLL locked)	X -100	X	X+100	ps	
$t_{sk(o)}$	Output-to-output Skew			150	ps	
$t_{sk(pp)}$	Part-to-part Skew			300	ps	
t_{PW}	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.5 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time				ns	
t_{PZL}	Output Enable Time				ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter (Peak-to-Peak)		±50			
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. AC characterisitics apply for parallel output termination of 50Ω to $V_{TT} = V_{CC}/2$

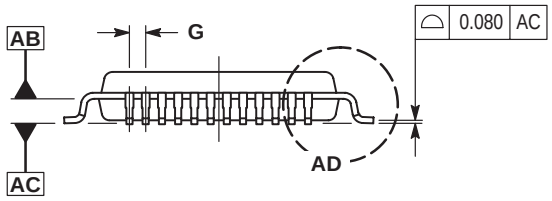
OUTLINE DIMENSIONS

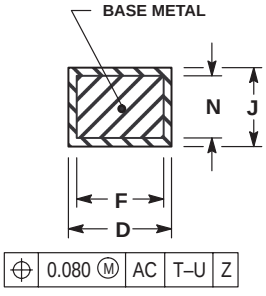
FA SUFFIX
LQFP PACKAGE
CASE 932–03
ISSUE F



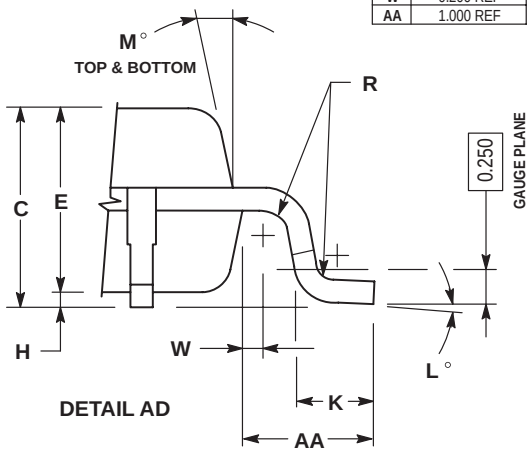
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12 °REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





SECTION AE–AE



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