Photolink- Fiber Optic Receiver
EAPLRBA2

Features

- •High speed signal transmission(25Mbps NRZ Signal)
- • High PD sensitivity optimized for red light
- • Data : NRZ signal
- • Low power consumption for extended battery life
- • Built-in threshold control for improved noise Margin
- • The product itself will remain within RoHS compliant version
- • Receiver sensitivity: up to −27dBm (Min. for 25Mbps)

Description

The optical receiver is packaged with custom optic data link interface, integrated on a proprietary CMOS PDIC process.
The unit functions by converting optical signals into electric ones.
The unit is operated at 3.0 ~ 5.5 V and the signal output interface is TTL compatible with high performance at low power consumption.

Applications

- • Digital Optical Data-Link
- • Dolby AC-3 Digital Audio Interface
- • HDMI Digital (192kHz) Audio Interface

Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 ~ +5.5	V
Output Voltage	Vout	Vcc +0.3	V
Storage Temperature	Tstg	-40 to 85	ºC
Operating Temperature	Topr	-20 to 70	ºC
Soldering Temperature	Tsol	260*	ºC
Human Body Model ESD	HBM	2000	V
Machine Model ESD	MM	100	V

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	Vcc	-	3.0	3.3	5.50	V

Electro-Optical Characteristics (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Peak sensitivity wavelength	λp	-	650	-	nm	-
Maximum receiver power	Pc,max	-	-	-14	dBm	Refer to Fig.1
Minimum receiver power	Pc,min	-27	-	-	dBm	Refer to Fig.1
Dissipation current	Icc	-	3	6	mA	Refer to Fig.2
High level output voltage	VOH	3.0	3.2	-	V	Refer to Fig.3
Low level output voltage	VOL	-	0.2	0.4	V	Refer to Fig.3
Rise time	tr	-	10	14	ns	Refer to Fig.3
Fall time	tf	-	10	14	ns	Refer to Fig.3
Propagation delay Low to High	tPLH	-	-	80	ns	Refer to Fig.3
Propagation delay High to Low	tPHL	-	-	80	ns	Refer to Fig.3
Pulse Width Distortion	Δtw	-15	-	+15	ns	Refer to Fig.3
Jitter	Δtj	-	1	5	ns	Refer to Fig.3, Pc=-14dBm
Jitter Transfer rate	Δtj T	-	5	10	ns	Refer to Fig.3, Pc=-27dBm
		0.1	-	25	Mb/s	NRZ signal

Measuring Method

*Fig.1 Measuring Method of Maximum and Minimum Input Power that Receiver Unit Need

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┌──────────────────┐
│  Control Circuit │
└────────┬─────────┘
         │
         ▼
┌──────────────────┐   Standard plastic optic fiber cable   ┌──────────────────┐
│   Transmitter    │◁═══════════════════════════════════════▷│ EAPLRAA8 Receiver│
└──────────────────┘                                         │      Unit        │
                                                             └──────────────────┘

                                                             ┌──────────────────┐
                                                             │Optical Power Meter│
                                                             └──────────────────┘
```
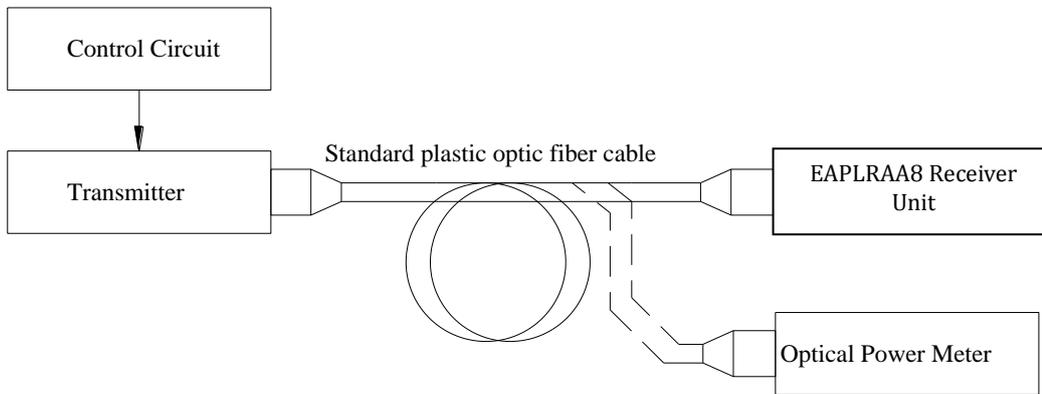
*Fig.2 Measuring Method of Dissipation Current

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┌──────────────────────────┐   Standard plastic optic fiber cable   ┌──────────────────────┐
│ Standard Transmitter unit│◁═══════════════════════════════════════▷│  EAPLRAA8 Receiver   │
└──────────────────────────┘                                         │        Unit          │
   Vin      Vcc      GND                                          Vcc        GND      Vout
                                                                      0.1uF
                                                                      47uH
                                                                       (A)
Signal
Input                                                                 3.3V
```

25Mbps NRZ "0101" successive signal input
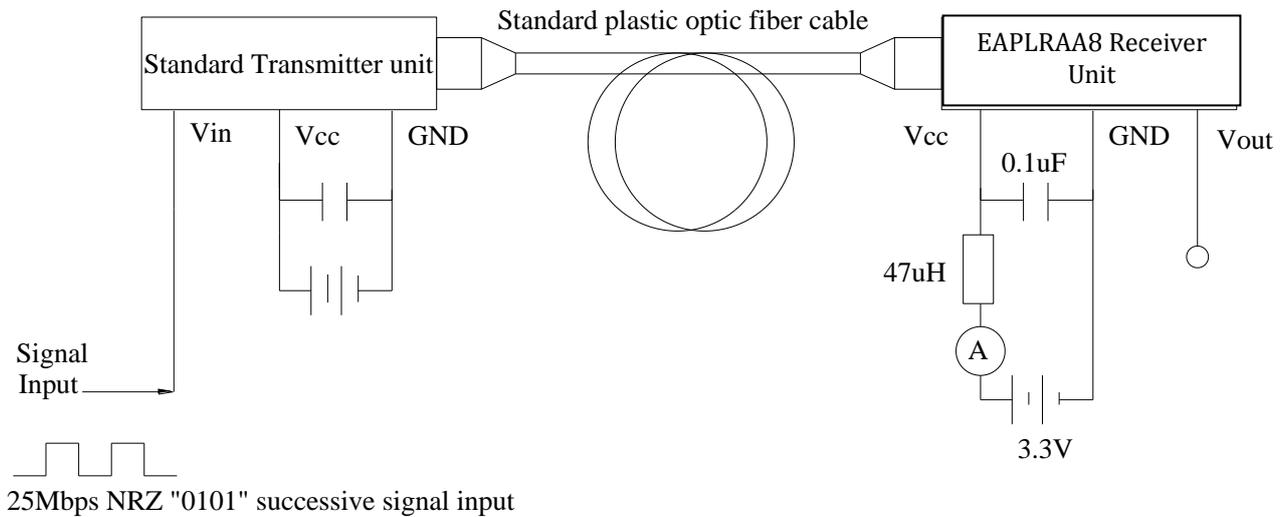
*Fig.3 Measuring Method of Output Voltage, Pulse and Jitter

Standard plastic optic fiber cable

Standard Transmitter Unit

EAPLRAA8 Receiver Unit

Vin   Vcc   GND

Vcc   GND   Vout

47uH   0.1uF

A

3V

Signal Input

16 Mbps NRZ "0101" successive signal input

T_{PLH} T_{PHL}

Input   50%

Output   50%

$\triangle tj1$ $\triangle tj2$ $\triangle t_w = T_{PHL} - T_{PLH}$

CH1

CH2
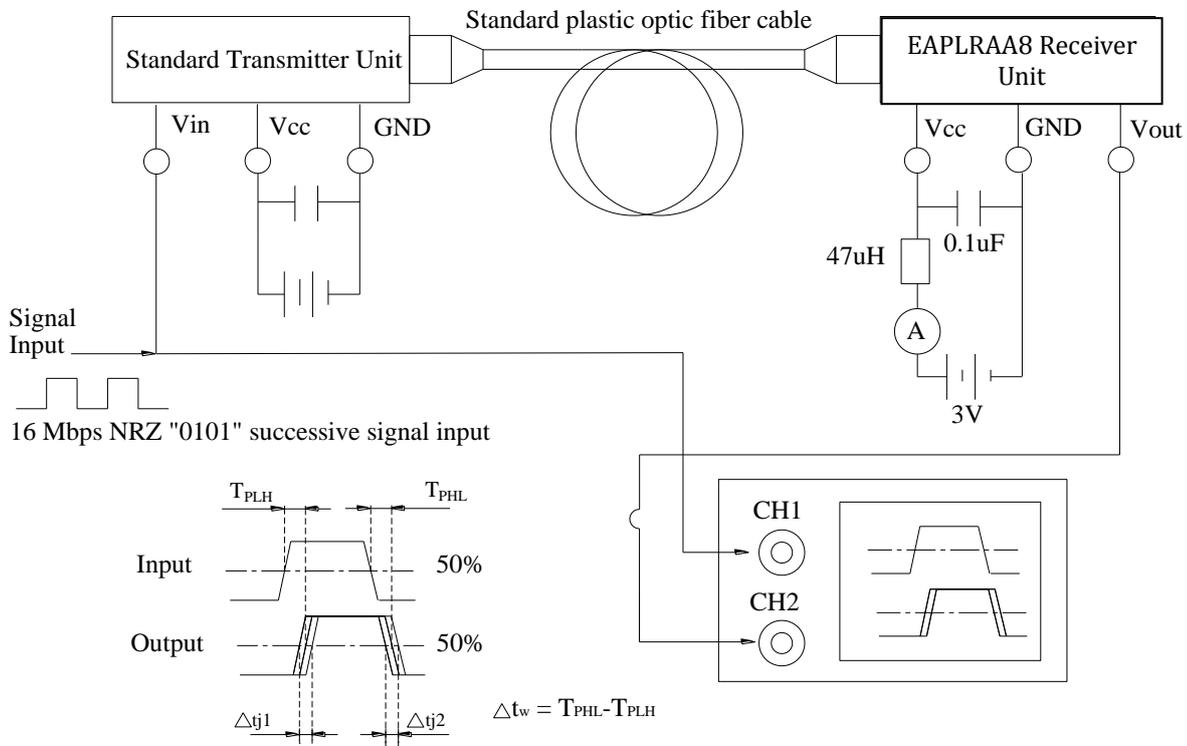
Application Circuit

(1) General application circuit

C1

Vcc   GND   Vout

L2   Vcc

C1:0.1uF
L2:47uH
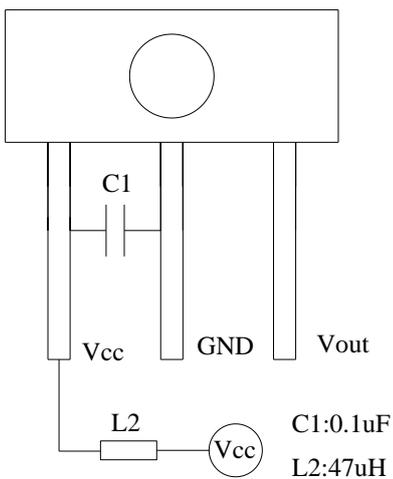
Note: 1.For having good coupling, the C1 capacitor must be placed within 7mm
2. For having good signal waveform, the Vout –GND circuit capacitor shall be smaller than 30pF.

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Typical Electro-Optical Characteristics Curves

*Fig.4 Power supply voltage vs. Minimum receiver power
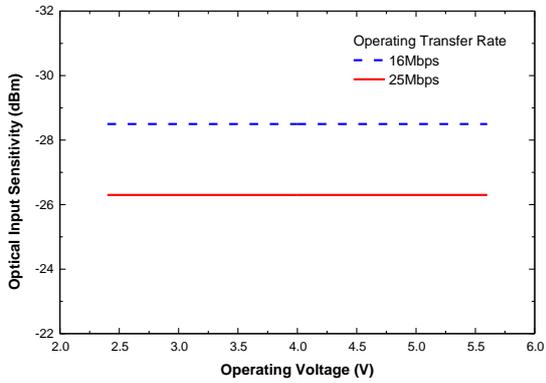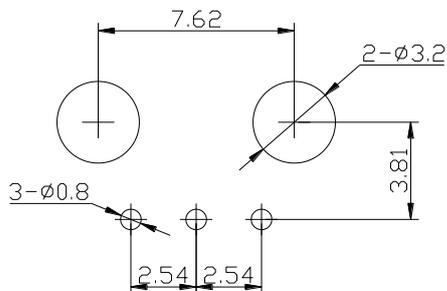
*Fig.5   Transfer rate vs. Minimum receiver power
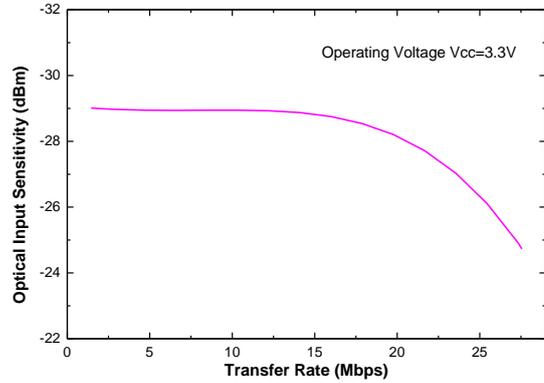
Note: Before using the   EAPLRBA2 device, please confirm the minimum sensitivity at different operating voltage and transmission rate.

Package Dimension

9.70±0.20

11.50±0.20

Cavity number

EL
PLR
T 9

Ø3.40
Ø2.40

23.30

4.95
5.65
10.00

6.00

3-0.50±0.05

2.54±0.20   2.54±0.20

3 | 2 | 1

7.62±0.10

13.50
2.90
5.45
4.05

1.55

2.70
4.70

8.51±0.40

3.00
0.40±0.03

PIN FUNCTION
1.Vout
2.GND
3.Vcc
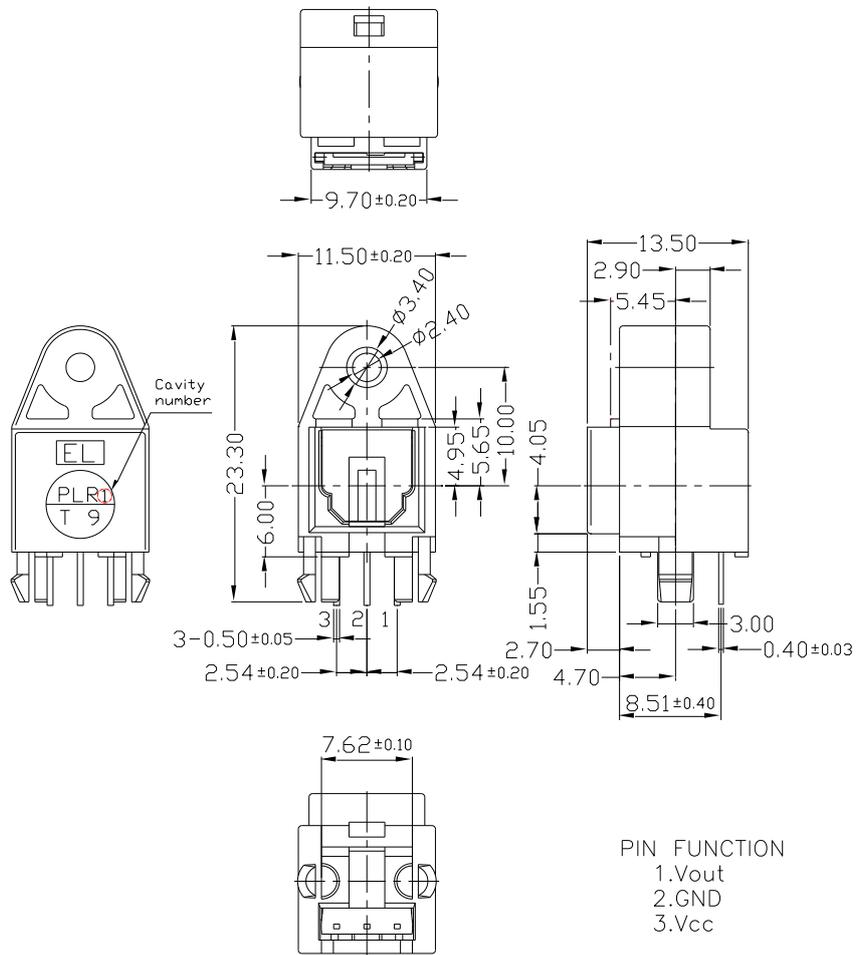
Note: Tolerances unless mentioned ±0.3mm. Unit = mm

PCB Layout for Electrical Circuit

7.62

2-Ø3.2

3.81

3-Ø0.8

2.54   2.54

Note: General Tolerance :±0.2mm, Substrate Thickness:1.6mm, Unit = mm

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Moisture Resistant Packing Materials

Label Explanation

- CPN: Customer's Product Number
- P/N: Product Number
- QTY: Packing Quantity
- CAT: Luminous Intensity Rank
- HUE: Dom. Wavelength Rank
- REF: Forward Voltage Rank
- LOT No: Lot Number
- X: Month
- Reference: Identify Label Number

Packing Quantity Specification

1. 50 pcs/tube
2. 20 tube/box

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Notes

1. Above specification may be changed without notice. EVERLIGHT Americas will reserve authority on material change for above specification.
2. .When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT Americas assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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Application Notes: EAPLRBA2 PCB layout for motherboard integration

To achieve better jitter and low input optical power performances, several PCB layout guidelines must be followed. These guidelines ensure the most reliable EAPLRBA2 POF performance for the motherboard integration. Failed to implement these PCB guidelines may affect the EAPLRBA2 jitter and low input power performances.

1. Careful decoupling of the power supplies is very important. Place a 0.1uf surface mount (size 805 or smaller) capacitor as close as (less than 2cm) to the POF Vdd and Gnd leads. The 0.1uf act as a low impedance path to ground for any stray high frequency transient noises.

2. To reduce the digital noises form the digital IC on the motherboard, the planar capacitance formed by an isolated Vcc and Gnd planes is critical. The POF device must be mounted directly on these two planes to reduce the lead parasitic inductance.

3. The isolated Vdd and Gnd planes must be connected to the main Vcc and Gnd (digital) planes at a single point using ferrite beads. The beads are used to block the high frequency noises from the digital planes while still allowing the DC connections between the planes
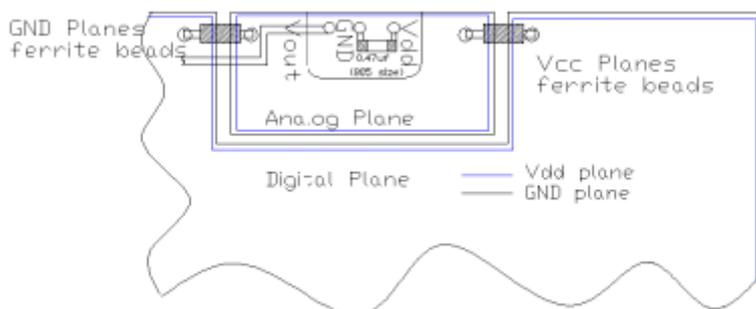
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