SEMTECH
GENNUM PRODUCTS

3Gb/s SDI Demo Board: Altera Version

User Guide

Version	ECR	Date	Changes and / or Modifications
1	158228	June 2012	Correction in Table 7-1: Bill of Materials.
0	152180	July 2009	New document.

Contents

1. Overview

The 3Gb/s SDI Demo Board is designed to demonstrate the functionality, flexibility and implementation simplicity of Gennum's 3G/HD/SD SDI devices. The Demo Kit consists of a 3Gb/s SDI Demo Board, FPGA source code and PC software. Paired with Altera's Demo Boards, it makes a versatile demo/evaluation platform for Gennum's 3Gb/s products. It is expected to help the users in system design with Gennum 3Gb/s devices.

The purpose of this document is to describe the functionalities and contents of Gennum's 3Gb/s SDI Demo Board for the Altera DK-DEV-3C120N and DK-START-3C25N Cyclone III development boards. Also included are a Quick Start Guide and an Advanced User Guide.

The Schematics, Board Layout and the Bill of Materials are given in the Appendix section at the end of this document.

1.1 Features

- Three 3G-SDI inputs with associated GS2974B Equalizers connected to two Gennum GS2970 Receivers
- One 3G-SDI loop-through output
- Two Gennum GS2970 Transmitters
- External Sync input followed by a Gennum GS4911B Clock and Timing Generator
- Provision for a Gennum GO2921 Optical Transceiver (not supplied with the board)
- Two AES inputs for audio embedding
- Two AES outputs for audio de-embedding
- A standard Gennum SPI header
- HSMC Connector Interface to Altera FPGA Board
- Pass-through Mode
- Dual-Link to 3Gb/s conversion
- 3Gb/s to Dual-Link conversion
- Stand alone Video Test Pattern Generator (Both Genlock or Free-run)
- Audio embedding and de-embedding

1.2 Featured Devices

GS2970 SD/HD/3G SDI Receiver complete with SMPTE Audio and Video Processing

GS2972 SD/HD/3G SDI Transmitter complete with SMPTE Audio and Video Processing

GS2974B Adaptive Cable Equalizer

GS2978 Multi-rate Dual Slew Rate Cable Driver

GS4911B HD/SD/Graphics Clock and Timing Generator with GENLOCK

2. Hardware

When you receive the 3Gb/s SDI Demo Board RDK (Reference Design Kit), the kit includes:

- A 3Gb/s SDI Demo Board
- A Gennum Serial Peripheral Interface (SPI) USB Dongle

2.1 3Gb/s SDI Demo Board

Figure 2-1 shows the top side of the 3Gb/s SDI Demo Board:

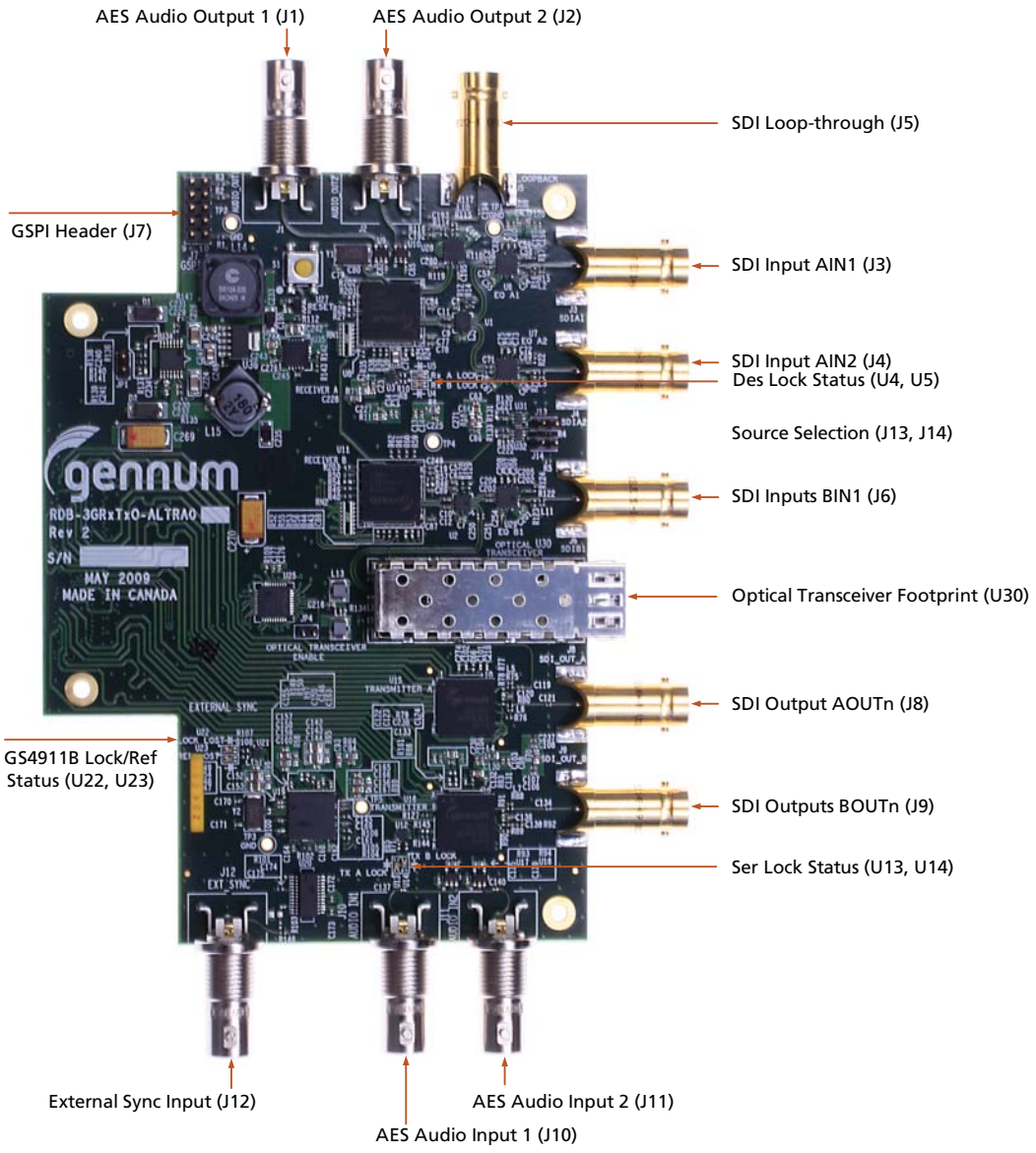

Figure 2-1: Top Side of the 3Gb/s SDI Demo Board

Figure 2-2 show the bottom side of the 3Gb/s SDI Demo Board:

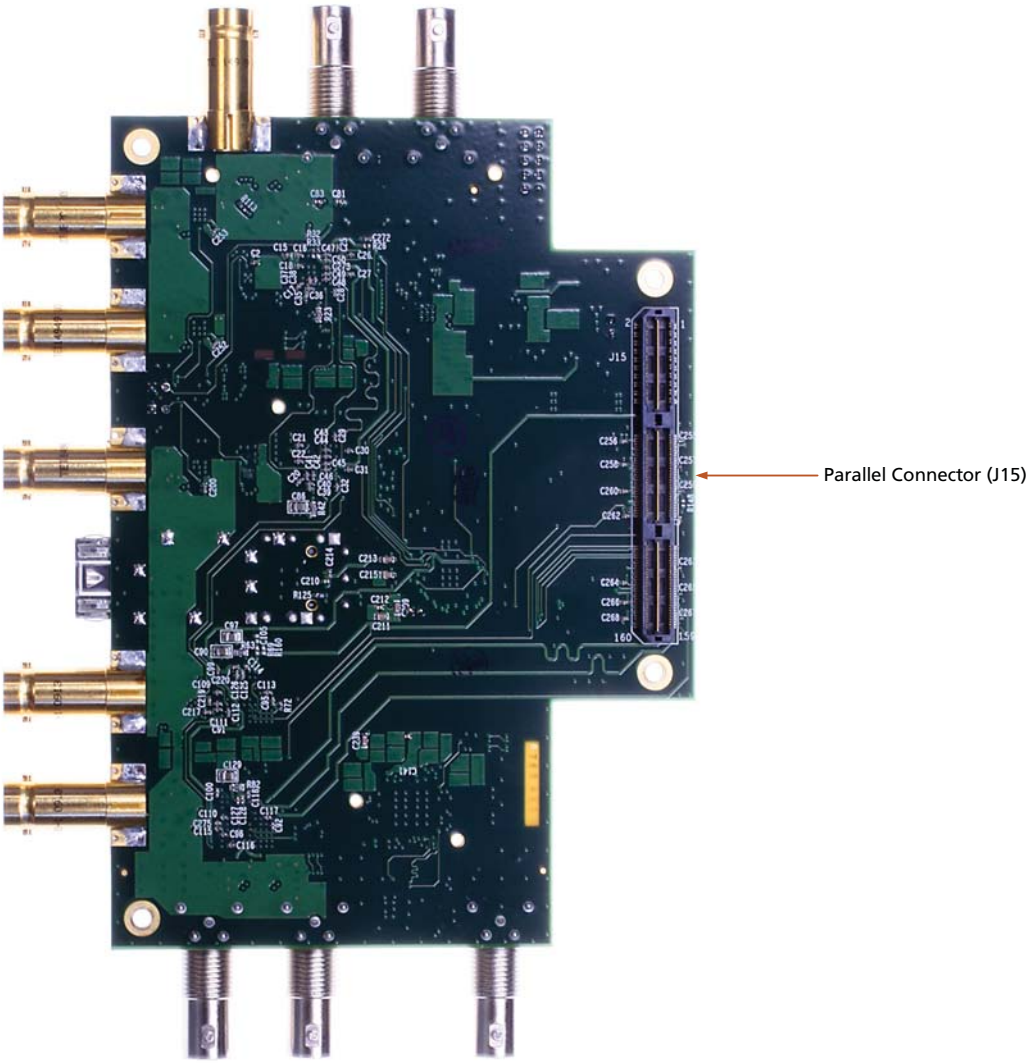

Figure 2-2: Bottom side of the 3Gb/s SDI Demo Board

Figure 2-3 shows the Gennum SPI USB Dongle Board:

Figure 2-3: Gennum USB Dongle

Figure 2-4 shows a block diagram of the features and signal flow of the 3G/s SDI Demo Board:

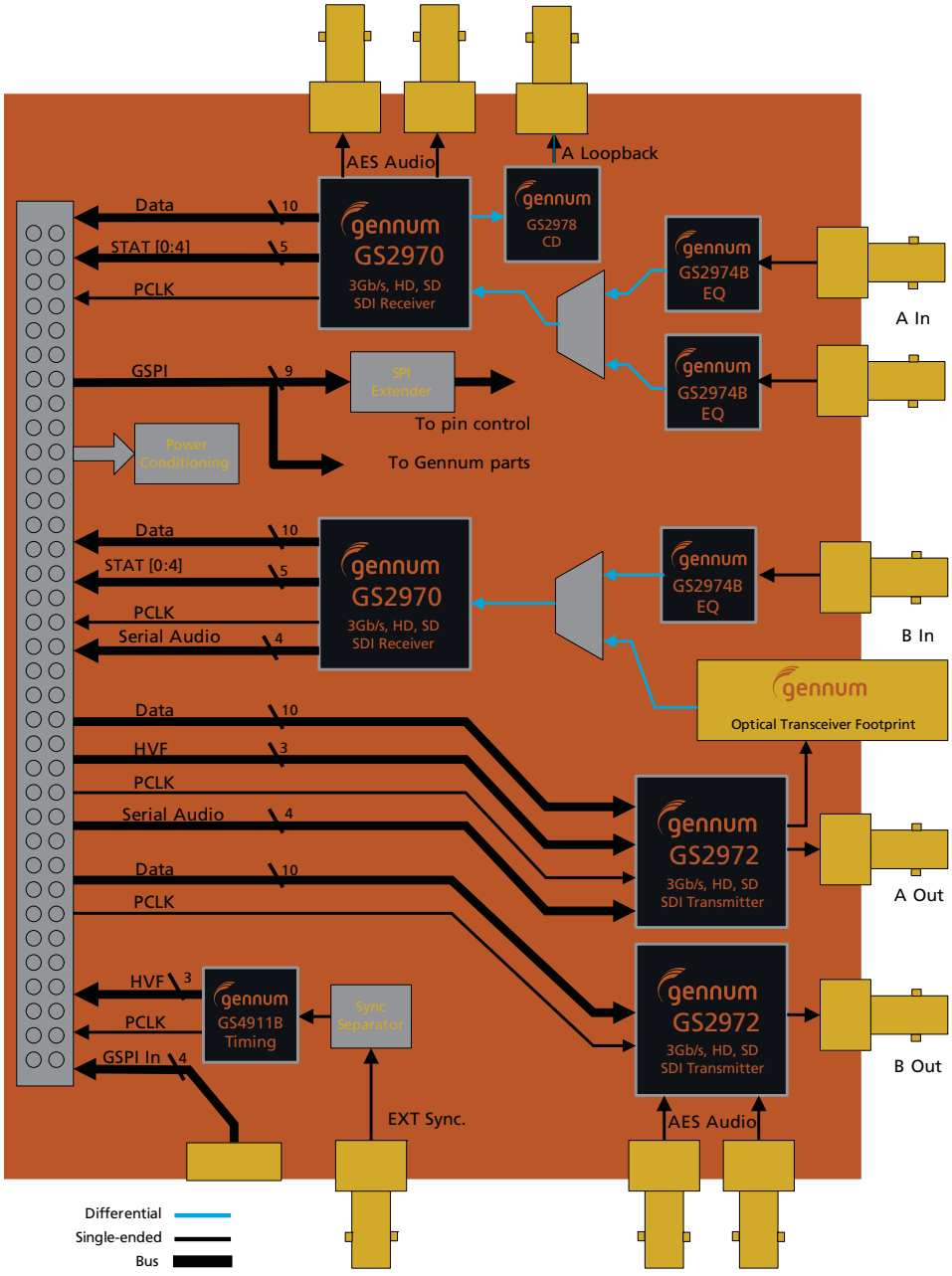

Figure 2-4: Block Diagram of the 3Gb/s SDI Demo Board

Table 2-1: 3Gb/s SDI Demo Board Legend

Description	Label
SDI Input AIN1	J3
SDI Input AIN2	J4
SDI Input BIN1	J6

Table 2-1: 3Gb/s SDI Demo Board Legend

Description	Label
SDI Output AOUTn	J8
SDI Output BOUTn	J9
GSPI Header	J7
AES Audio Input 1	J10
AES Audio Input 2	J11
Parallel Connector	J15
SDI Loop-through	J5
AES Audio Output 1	J1
AES Audio Output 2	J2
Receiver Lock Status Indicators	U4, U5
Transmitter Lock Status Indicators	U13, U14
Video Source Selection Jumpers	J13, J14
External Sync Input	J12
GS4911B Lock/Ref Status	U22, U23

2.2 Mother Boards

NOTE: The following hardware is *not* included in the Gennum RDK.

Gennum's 3Gb/s SDI Demo Board was designed to mate with Altera demo boards through a HSMC connector. Two boards were targeted; the DK-DEV-3C120N and the smaller DK-START-3C25N. Gennum's RDK comes with programming files, source code and Quartus project for both boards. Other Altera demo boards may work with the Gennum 3Gb/s SDI Demo Board, but other boards were not tested with the Gennum 3Gb/s SDI Demo Board.

Figure 2-5 and Figure 2-6 show the Altera DK-DEV-3C120N and DK-START-3C25N Development Boards. The DIP switch, Demo Board interface connector, push buttons and LEDs are indicated in these figures:

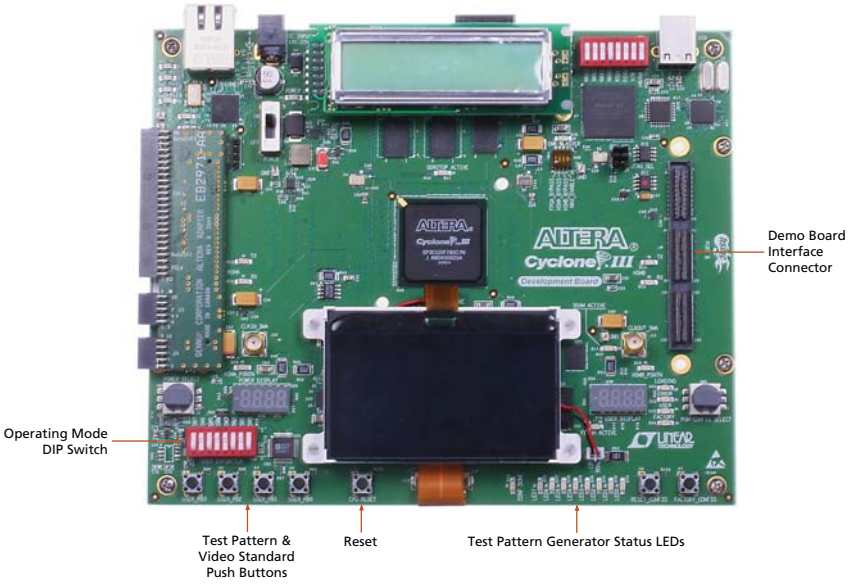

Figure 2-5: Altera DK-DEV-3C120N Development Board

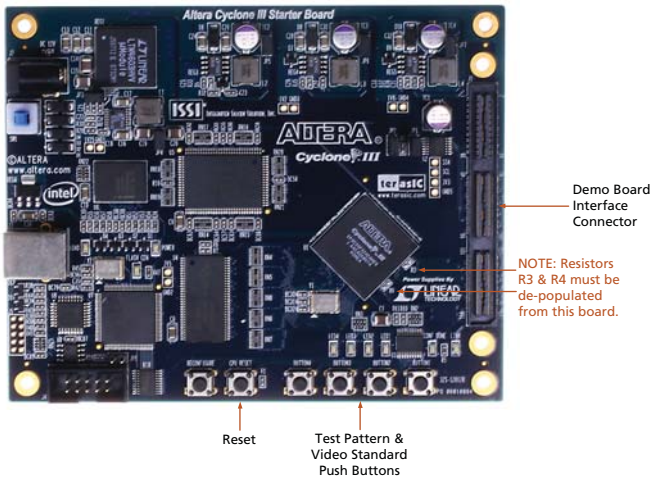

Figure 2-6: Altera DK-START-3C25N Cyclone III Development Board

3. Detailed Description

This section describes the frequently used devices and their functions. For unused jumpers, switches, and LEDs on the FPGA board, please refer to the Altera Board User Guides.

3.1 Operating Modes (FPGA Board)

The current release of the FPGA code supports five distinct modes of operation: Pass-through, 3G Level B to Dual-Link, Dual-Link to 3G Level B, Test Pattern with Genlock, and Test Pattern with Free-run. Operating modes can be set through dip switch SW6 (DK-DEV-3C120N only), or by programming the FPGA's internal registers (Reg2) through the SPI. Programming through the SPI is the only option to set operating modes for the DK-START-3C25N, which does not have a user dip switch. In the case of DK-START-3C25N, Reg3 replaces the dip switch, although Reg2 is still available. Table 3-1 shows how the operating mode can be selected by the dip switches on the Altera Boards.

Table 3-1: Altera Board Operating Modes

Dip Switch	State	Reg4 (2:0)*	Operating Mode	Notes
SW3: Bit 1,2,3	OFF/OFF/OFF	000	Video Pass-through Mode	All standards
	OFF/ON/ON	011	3G Level B to DL	–
	ON/OFF/OFF	100	DL to 3G Level B	YCbCr 422 10b. The monitor set to 1080i59.94
	ON/ON/OFF	110	Genlock Test Pattern	Selected standards
	ON/OFF/ON	101	Test Pattern	All standards and patterns
SW3: Bit 4-8	Not Defined			

*DK-START-3C25N only.

Video Pass-Through: Received video from input A is passed to output A, and input B passed to output B without any processing. All SD, HD and 3G formats are supported. For 3G, the default setting is Level A. If Level B is anticipated, the configuration for the GS2972 must be changed through the SPI.

3G Level B to Dual-Link (HD): 3G Level B video from input A is passed to outputs A and B as a two-HD-stream output.

Dual-Link (HD) to 3G Level B: Two HD signals, with the same standard, from inputs A and B are multiplexed on to a 10-bit stream and passed to output A. By default, the GS2972 is configured to output a 3G Level B video signal.

Stand-alone Video Test Pattern Generator - Free-Run Mode: The system generates a video test pattern signal using clock and timing from the GS4911B, with the GS4911B in free-run mode.

Stand-alone Video Test Pattern generator - Genlock Mode: Video test patterns are generated using clock and timing signals from the GS4911B, derived from an external Genlock source.

Other modes which may be implemented through a GS2970/72 configuration change are: 3G Level A to Dual-Link and Dual-Link to 3G Level A.

The video test patterns are shown in Table 3-2:

Table 3-2: Video Test Patterns

ID	Pattern
0	Check Field/Pathological
1	100% Colour Bars
2	75% Colour Bars
3	SMPTE RP219 Bars
4	EG1 Bars
5	5 Step Stair Case
6	Luma Step
7	75% Blue
8	Green
9	Red
10	100% Black
11	40% Gray
12	100% White
13	75% Colour Bars
14	75% Colour Bars
15	75% Colour Bars

The Test Pattern Video Standards are shown in Table 3-3.

Table 3-3: Test Pattern Video Standards

LED3-0	GS4911B VID_STD	Standard	
0000	21	1080p60	1920x1080/60/1:1 148.5 MHz
0001	22	1080p59.94	1920x1080/59.94/1:1 148.35 MHz
0010	23	1080p50	1920x1080/50/1:1 148.5 MHz
0011	29	1080p30	1920x1080/30/1:1 74.25 MHz
0100	31	1080p29.97	1920x1080/29.97/1:1 74.175 MHz
0101	33	1080p25	1920x1080/25/1:1 74.25 MHz

Table 3-3: Test Pattern Video Standards

LED3-0	GS4911B VID_STD		Standard
0110	35	1080p24	1920x1080/24/1:1 74.25 MHz
0111	37	1080p23.98	1920x1080/23.98 74.175 MHz
1000	25	1080i60	1920x1080/60i 74.25 MHz
1001	26	1080i59.94	1920x1080/59.94i 74.175 MHz
1010	27	1080i50	1920x1080/50i 74.25 MHz
1011	11	720p60	1280x720/60/1:1 74.25 MHz
1100	12	720p59.94	1280x720/59.94/1:1 74.175 MHz
1101	13	720p50	1280/720/50/1:1 74.25 MHz
1110	14	720p30	1280x720/30/1:1 74.25 MHz
1111	15	720p29.97	1280x720/29.97/1:1 74.25 MHz

3.2 Hardware Description

3.2.1 Jumpers

Selection of the video input can be done from either the FPGA or from the jumper headers (J13 and J14) on the 3Gb/s SDI Demo Board.

When the jumpers are open (removed from the header), the FPGA takes control of the video input multiplexers. When the FPGA outputs 'ones', the jumper can override the settings.

Table 3-4 shows the selections available through jumpers J13 and J14:

Table 3-4: Video Source Selection by Jumpers on 3Gb/s SDI Demo Board

Jumper	Video Path	Jumper State	Input Selected
J13	A	Open	AIN1
		Closed	AIN2
J14	B	Open	BIN1
		Closed	Optical

3.2.2 LED Indicators

3.2.2.1 Lock Status LEDs (3G SDI Demo Board)

U4, U5, U13, U14, U22 and U23 on the 3Gb/s SDI Demo Board are bi-colour LEDs that indicate the lock status of the Gennum Transmitter, Receiver and Clock/Timing devices.

Table 3-5: Lock Status

LED	Function	Green	Red
U4	GS2970 A, U8 Lock Status	Locked	Unlocked
U5	GS2970 B, U11 Lock Status	Locked	Unlocked
U13	GS2972 A, U15 Lock Status	Locked	Unlocked
U14	GS2972 B, U16 Lock Status	Locked	Unlocked
U22	GS4911B, U19 Lock Status	Locked	Lock Lost
U23	GS4911B, U19 Ref Status	Detected	Lost

3.2.2.2 Test Pattern Generator Status LEDs (FPGA board, DK-DEV-3C120N only)

LEDs 0 through 7 on the DK-DEV-3C120N board indicate the type of the test pattern, the video standard and configuration status.

Table 3-6: Test Pattern Generator Status

LED	Descriptions
LED3 -LED0	Video Standard of the Test Pattern
LED7 - LED4	Pattern selected

3.2.3 Connectors

3.2.3.1 Video Inputs AIN (J3, J4) and BIN (J6)

The 3Gb/s SDI Demo Board includes three SDI inputs. The applied SDI stream passes through Gennum's GS2974B Cable Equalizer before entering the Micrel SY58017U Mux. The output of the Mux is fed into the SDI input pins of the GS2970 Receiver.

3.2.3.2 AES Audio Inputs (J10, J11)

Up to four channels of audio are supported by the Demo Board. Group One can be connected directly to the GS2972 as AES (J10, J11).

This configuration is meant to allow users to have the capability of evaluating audio embedding. For SD audio, when embedding audio with both groups, the audio needs to be synchronized externally.

3.2.3.3 External Sync (J12)

Gennum's GS4911B is connected to a sync separator to provide synchronization to an external video timing reference. When in free-run mode, the GS4911B can also be used to provide clock and timing signals for the stand-alone Pattern Generator.

3.2.3.4 Optical Connector (U30)

Optionally, a Gennum GO2921 Optical Module (U30) may be plugged into the cage provided. The GO2921 is an optical transceiver which allows input of a signal via optical fibre, and outputs a video signal from one of the GS2972 Transmitters (U15, U16). 3Gb/s, HD and SD video signals are supported.

3.2.3.5 SDI Outputs (J8, J9)

Two BNC connectors for SDI outputs, J8 and J9, are connected to the two GS2972 Transmitters U15 and U16 respectively.

3.2.3.6 SDI Loop-Through (J5)

A re-clocked or non-re-clocked buffered version of the input stream from GS2970(A) is available on the serial loop-through output (J5). It is designed to be SMPTE compliant for voltage level, rise/fall time and return loss at three rates (SD, HD and 3G) using the compensation network. The GS2978 Cable Driver is necessary to guarantee return loss specification.

The signal rate on the GS2978 Cable Driver is automatically set to SD or HD mode by the RATE_DET signal from the GS2970 (U8).

3.2.3.7 Audio Outputs (J1, J2)

In AES mode, AES-encoded CMOS-level signals are distributed through line drivers and supplied to two BNC connectors (J1, J2).

3.2.3.8 SPI Header (J7)

The standard Gennum SPI header on the 3Gb/s SDI Demo Board, along with the USB dongle, allow the user to explore all settings and tuning possibilities of Gennum's 3Gb/s SDI and timing products, through a USB connection to a PC.

Gennum's GS2970, GS2972 and GS4911B devices contain sets of internal status and configuration registers. These registers are available to the host via the SPI.

3.2.3.9 HSMC Connector (J15)

The HSMC Connector (J15) on the 3Gb/s SDI Demo Board is compatible with Altera's standard connector for interfacing to Altera demo boards.

Input Signals:

- 2 x 10-bit video data from two GS2970s
- 2 x PCLK from two GS2970s
- 2 x STAT[0:4] outputs from two GS2970s, HVF and rate detection
- Serial audio input ACLK, WCLK, DATA1_2 and DATA3_4 from one GS2970
- HVF, PCLK and ACLK1 from GS4911B
- Inputs from GSPI header SCLK, SDIN, $\overline{CS}$

Output Signals:

- 2 x 10-bit video data from two GS2972s
- 2 x PCLK to GS2972s
- HVF input to first GS2972
- Serial audio input to first GS2972, ACLK, WCLK, DATA1_2 and DATA3_4
- SDOUT to the SPI header
- SCLK, SDIN, 6 x $\overline{CS}$ for the SPI on the board
- Output from the SPI on the board (SDOUT)

Table 3-7: HSMC Connector Signals

3Gb/s SDI Board		CYCLONEIII 3c120 Board		CYCLONEIII 3c25 Board	
J15 pin	3Gb/s SDI Board Net Name	Board Net Name	FPGA Pin	Board Net Name	FPGA Pin
pin 33	SDIN_0	HSMB_SDA	H26	HSMC_SDA	E1
pin 34	SCLK_0	HSMB_SCL	H25	HSMC_SCL	F3
pin 39	SDOUT_0	HSMB_CLK_OUT0	J22	HSMC_CLKOUT0	A1
pin 40	ACLK4911	HSMB_CLK_IN0	A15	HSMC_CLKIN0	A9
pin 41	GS4911_HVF1	HSMB_D0	G24	HSMC_D0	H6
pin 42	Rx_A_STAT4	HSMB_D1	H23	HSMC_D1	D3
pin 43	GS4911_HVF0	HSMB_D2	G25	HSMC_D2	M5
pin 44	Rx_B_AUDIO2	HSMB_D3	H24	HSMC_D3	L6
pin 47	PCLK_Tx_A	HSMB_TX_P0	J25	HSMC_D4	T1
pin 48	Rx_B_AUDIO3	HSMB_RX_P0	F27	HSMC_D5	M3
pin 49	GS4911_HVF2	HSMB_TX_N0	J26	HSMC_D6	N7
pin 50	Rx_B_AUDIO0	HSMB_RX_N0	F28	HSMC_D7	T2
pin 53	Tx_A_DATA9	HSMB_TX_P1	L23	HSMC_D8	N8
pin 54	Rx_B_AUDIO1	HSMB_RX_P1	G27	HSMC_D9	H15
pin 55	Tx_A_DATA8	HSMB_TX_N1	L24	HSMC_D10	J13
pin 56	F_Rx_A	HSMB_RX_N1	G28	HSMC_D11	H16
pin 59	Tx_A_DATA7	HSMB_TX_P2	M25	HSMC_D12	N10
pin 60	V_Rx_A	HSMB_RX_P2	K25	HSMC_D13	N16
pin 61	Tx_A_DATA6	HSMB_TX_N2	M26	HSMC_D14	N11
pin 62	H_Rx_A	HSMB_RX_N2	K26	HSMC_D15	N15
pin 65	Tx_A_DATA5	HSMB_TX_P3	N25	HSMC_D16	K17
pin 66	Rx_A_DATA0	HSMB_RX_P3	K27	HSMC_D17	R16
pin 67	Tx_A_DATA4	HSMB_TX_N3	N26	HSMC_D18	P11

Table 3-7: HSMC Connector Signals

3Gb/s SDI Board		CYCLONEIII 3c120 Board		CYCLONEIII 3c25 Board	
pin 68	Rx_A_DATA1	HSMB_RX_N3	K28	HSMC_D19	T16
pin 71	Tx_A_DATA3	HSMB_TX_P4	R27	HSMC_TX_p4	B2
pin 72	Rx_A_DATA2	HSMB_RX_P4	L27	HSMC_RX_p4	C2
pin 73	Tx_A_DATA2	HSMB_TX_N4	R28	HSMC_TX_n4	B1
pin 74	Rx_A_DATA3	HSMB_RX_N4	L28	HSMC_RX_n4	C1
pin 77	Tx_A_DATA1	HSMB_TX_P5	R25	HSMC_TX_p5	G2
pin 78	Rx_A_DATA4	HSMB_RX_P5	M27	HSMC_RX_p5	H2
pin 79	Tx_A_DATA0	HSMB_TX_N5	R26	HSMC_TX_n5	G1
pin 80	Rx_A_DATA5	HSMB_RX_N5	M28	HSMC_RX_n5	H1
pin 83	GSPI_SCLK_R	HSMB_TX_P6	U25	HSMC_TX_p6	K2
pin 84	Rx_A_DATA6	HSMB_RX_P6	P25	HSMC_RX_p6	K5
pin 85	GSPI_SDIN_Conn	HSMB_TX_N6	U26	HSMC_TX_n6	K1
pin 86	Rx_A_DATA7	HSMB_RX_N6	P26	HSMC_RX_n6	L5
pin 89	GSPI_SDOUT	HSMB_TX_P7	V27	HSMC_TX_p7	L2
pin 90	Rx_A_DATA8	HSMB_RX_P7	P27	HSMC_RX_p7	L4
pin 91	GSPI_CS0	HSMB_TX_N7	V28	HSMC_TX_n7	L1
pin 92	Rx_A_DATA9	HSMB_RX_N7	P28	HSMC_RX_n7	L3
pin 95	GSPI_CS1	HSMB_CLK_OUT_P 1	AC26	HSMC_CLKOUT_p1	D14
pin 96	PCLK_Rx_A	HSMB_CLK_IN_P1	J27	HSMC_CLKIN_p1	F17
pin 97	GSPI_CS2	HSMB_CLK_OUT_N 1	AD26	HSMC_CLKOUT_n1	C14
pin 98	PCLK4911	HSMB_CLK_IN_N1	J28	HSMC_CLKIN_n1	F18
pin 101	GSPI_CS3	HSMB_TX_P8	V25	HSMC_TX_p8	M2
pin 102	Tx_A_AUDIO0	HSMB_RX_P8	P21	HSMC_RX_p8	P2
pin 103	GSPI_CS4	HSMB_TX_N8	V26	HSMC_TX_n8	M1
pin 104	Tx_A_AUDIO1	HSMB_RX_N8	R21	HSMC_RX_n8	P1
pin 107	Tx_A_H	HSMB_TX_N9	W26	HSMC_TX_p9	R2
pin 108	Tx_A_AUDIO2	HSMB_TX_P9	W25	HSMC_RX_p9	T3
pin 109	Tx_A_V	HSMB_RX_P9	R22	HSMC_TX_n9	R1
pin 110	Tx_A_AUDIO3	HSMB_RX_N9	R23	HSMC_RX_n9	R3
pin 113	Tx_A_F	HSMB_TX_P10	Y25	HSMC_TX_p10	E17
pin 114	SPI_SDOUT_Exp	HSMB_RX_P10	T25	HSMC_RX_p10	G17
pin 115	Rx_B_STAT4	HSMB_TX_N10	Y26	HSMC_TX_n10	E18

Table 3-7: HSMC Connector Signals

3Gb/s SDI Board		CYCLONEIII 3c120 Board		CYCLONEIII 3c25 Board	
pin 116	F_Rx_B	HSMB_RX_N10	T26	HSMC_RX_n10	G18
pin 119	PCLK_Tx_B	HSMB_TX_P11	AA25	HSMC_TX_p11	H17
pin 120	V_Rx_B	HSMB_RX_P11	U27	HSMC_RX_p11	K18
pin 121	Lock_Rx_B	HSMB_TX_N11	AA26	HSMC_TX_n11	H18
pin 122	H_Rx_B	HSMB_RX_N11	U28	HSMC_RX_n11	L18
pin 125	Tx_B_DATA9	HSMB_TX_P12	AB25	HSMC_TX_p12	L17
pin 126	Rx_B_DATA0	HSMB_RX_P12	U22	HSMC_RX_p12	L16
pin 127	Tx_B_DATA8	HSMB_TX_N12	AB26	HSMC_TX_n12	M18
pin 128	Rx_B_DATA1	HSMB_RX_N12	V22	HSMC_RX_n12	M17
pin 131	Tx_B_DATA7	HSMB_TX_P13	Y23	HSMC_TX_p13	L14
pin 132	Rx_B_DATA2	HSMB_RX_P13	W28	HSMC_RX_p13	L13
pin 133	Tx_B_DATA6	HSMB_TX_N13	Y24	HSMC_TX_n13	L15
pin 134	Rx_B_DATA3	HSMB_RX_N13	W27	HSMC_RX_n13	M14
pin 137	Tx_B_DATA5	HSMB_RX_P14	V23	HSMC_TX_p14	P17
pin 138	Rx_B_DATA4	HSMB_TX_N14	AE28	HSMC_RX_p14	R17
pin 139	Tx_B_DATA4	HSMB_TX_P14	AE27	HSMC_TX_n14	P18
pin 140	Rx_B_DATA5	HSMB_RX_N14	V24	HSMC_RX_n14	R18
pin 143	Tx_B_DATA3	HSMB_TX_P15	W22	HSMC_TX_p15	R5
pin 144	Rx_B_DATA6	HSMB_RX_P15	AB27	HSMC_RX_p15	M6
pin 145	Tx_B_DATA2	HSMB_TX_N15	Y22	HSMC_TX_n15	R4
pin 146	Rx_B_DATA7	HSMB_RX_N15	AB28	HSMC_RX_n15	N6
pin 149	Tx_B_DATA1	HSMB_TX_P16	V21	HSMC_TX_p16	T17
pin 150	Rx_B_DATA8	HSMB_RX_P16	AC27	HSMC_RX_p16	M13
pin 151	Tx_B_DATA0	HSMB_TX_N16	W21	HSMC_TX_n16	T18
pin 152	Rx_B_DATA9	HSMB_RX_N16	AC28	HSMC_RX_n16	N13
pin 155	Rx_B_DATA9	HSMB_CLK_OUT_P 2	AD27	HSMC_CLKOUT_p2	U18
pin 156	PCLK_Rx_B	HSMB_CLK_IN_P2	Y27	HSMC_CLKIN_p2	N17
pin 157	CS0_0	HSMB_CLK_OUT_N 2	AD28	HSMC_CLKOUT_n2	V18
pin 158	Lock_Rx_A	HSMB_CLK_IN_N2	Y28	HSMC_CLKIN_n2	N18

3.2.4 Push Buttons

3.2.4.1 Reset

Because of the limited number of the connections on the J15 connector, there are two separate resets. On the SDI Demo board, the RESET push button (S1) will reset all Gennum parts on the board. In order to reset the FPGA board, the CPU_RESET push button must be pressed. It is recommended that the Gennum board be reset before the Altera board.

3.2.4.2 Test Pattern

The Pattern Generator is active in Test Pattern operation mode.

In Genlock mode, the Pattern Generator is synchronized to the external sync input. While in Free-run mode, it does not need an external sync input.

The output test pattern may be changed by using the following two push buttons:

UP push button

- USER_PB1 (DK-DEV-3C120N)
- BUTTON2 (DK-START-3C25N)

DOWN push button

- USER_PB0 (DK-DEV-3C120N)
- BUTTON1 (DK-START-3C25N)

3.2.4.3 Test Pattern Video Standard

The video standard of the test pattern may be changed by using the two push buttons:

UP push button

USER_PB3 (DK-DEV-3C120N)

BUTTON4 (DK-START-3C25N)

DOWN push button

USER_PB2 (DK-DEV-3C120N)

BUTTON3 (DK-START-3C25N)

NOTE: After power-up or reset, the board does not output a test pattern signal until one of the push buttons is pressed.

3.3 FPGA

3.3.1 Programming from Flash Memory

At power-up or by pressing the RESET_CONFIG or FACTORY_CONFIG push button, the MAX II CPLD device's PFL megafunction will configure the Cyclone III FPGA from flash memory. The provided POF file can be used to program flash memory.

For more details, please refer to **cycloneIII_3c120_dev_reference_manual.pdf**, **cycloneIII_3c25_start_board_reference_manual.pdf** and **Altera Application Note 386: Using the Parallel Flash Loader with the Quartus II software.**

3.3.2 JTAG Programming

The FPGA can be programmed at any time while the board is powered by the USB 2.0 interface with the Quartus II Programmer in JTAG mode. To program the device, connect a USB cable to the USB jack (J3) on the FPGA board. Open the Quartus II Programmer and load the provided SOF file. Check that all switches and jumpers on the board are set for the JTAG mode. Click the start button.

This method is appropriate for code-debugging stage, since configuration on the FPGA can be updated quickly. However, it is volatile; each time after powering-up, the cable has to be used to download the code. For more details, please refer to **cycloneIII_3c120_dev_reference_manual.pdf** or **cycloneIII_3c25_start_board_reference_manual.pdf**.

4. Getting Started

4.1 Quick Start Guide

Please follow the steps below to achieve a quick start up:

1. Turn off the power switch on the FPGA board and apply power to power jack.
2. Confirm that all jumpers and switches are set to default state.
3. Connect the USB cable to the USB jack (J3).
4. Plug the J15 connector (on the bottom side of the Gennum 3Gb/s SDI Demo Board) into the Port B connector located on the right hand side of the Altera Board (J1 for the EP3C25 board). Secure with the hardware provided (screws, stand-offs, washers and nuts).
5. Connect a SDI video source to the AIN1(J3) and/or AIN2(J4) BNC connectors, or the BIN1(J6) BNC connector (located on the right-hand side of the SDI Demo Board). These connectors accept SD, HD and 3G SDI input signals. A loop-through output is available on J5 of the SDI Demo Board.
6. Connect the output video cables to the AOUTn(J8) and the BOUT(J9) BNC connectors located at the right-hand side of the SDI Demo Board.
7. For audio embedding, connect the AES Audio Input signals to the AES_IN1 (J10) and AES_IN2 (J11); AES_IN1 is for embedding Audio channels 1 and 2, while AES_IN2 is for channels 3 and 4.
8. For Genlock to an external black burst signal, connect a source to EXT_SYNC (J12).
9. For de-embedded audio, connect the cables on to AUDIO_OUT1 (J1) and AUDIO_OUT2 (J2).
10. Set the Operating Mode on the Altera Board. Refer to Table 3-1: Altera Board Operating Modes.
11. Turn on the power switch. Use the Quartus II Programmer to configure the device in JTAG mode. Select the provided SOF file for programming. If programming from flash memory is preferred, an explanation of the required steps can be found in: **cycloneIII_3c120_dev_reference_manual.pdf**, **cycloneIII_3c25_start_board_reference_manual.pdf** and **Altera Application Note 386: Using the Parallel Flash Loader with the Quartus II software**.
12. Flash load with the Quartus II software. The board performs initialization after reset. First, the FPGA configures the I/O Expander's pins as outputs, and then the control pins on the Gennum devices are set by the I/O Expander. If required by the operating mode, the internal registers of the Gennum devices are written by the FPGA through the daisy-chained SPI to complete the initialization.

When a new operation mode is selected through the DIP switches, the on-board devices are programmed for the new mode by the FPGA via the SPI and the MAX 7301 I/O Expander.

The GS2970s and GS2972s are configured in SMPTE mode by default. They perform full SMPTE processing, and feature a number of signal integrity checks and measurement capabilities.

Refer to the GS2970 and GS2972 Data Sheets for a more detailed explanation of their modes of operation.

For the SDI receiver Rate Selection, the GS2970 Receivers automatically detect the input signal as SD-SDI, HD-SDI or 3G-SDI.

For the SDI Transmitter Rate Selection, the GS2972 Transmitters are configured by the FPGA to output the detected rate. The FPGA reads the rate values from the SDI Receivers and programs the RATE_SEL pins on the GS2972 accordingly via the I/O Expander.

When no video input signal is detected by either Equalizer (U6 or U7), the corresponding Receivers (U8, U11), can be placed in Standby mode. In this mode, no signal is generated at the output, and the power consumption is reduced. By default, this mode is disabled by DNP R130 and populating R131 on the SDI Demo Board.

In Pass-through mode, Input A needs a valid single for the board configuration to stabilize so that Input B can work without any interruption. This is due to the FPGA attempting to detect the input on A and configure the board repeatedly.

In Test Pattern Generator mode, the GS4911B is configured to provide the clock and timing signals of the selected standard. The test pattern output is available on SDI Output A (J8).

NOTE: After power-up or reset, the board does not output a test pattern signal until the sel_standard push button is pressed.

5. Advanced User Guide

The next step after evaluating the 3Gb/s products would be designing the user application board and the associated FPGA code. This section presents the implementation details of this demo/evaluation platform for the low cost Spartan 3A FPGA.

5.1 Top Level Architecture

Figure 5-1 is a simplified diagram of the FPGA top level architecture. It consists of a Test Pattern Generator, Channel A/B Input Paths, a Board Control Unit, Output Mux A/B and a SPI Interface.

The Board Control Unit sets the operating mode and provides access to the internal registers via the SPI. It also sets the control pins of the Gennum devices, via Maxim's MAX 7301 I/O Expander.

The right and left side of the diagram lists the signals to and from various blocks on the board. Also illustrated are the data/clock paths and major building blocks inside of the FPGA to achieve the five major operating modes. The signals in grayed-out text are reserved, and not currently used in the design.

For more details, please refer to the Advanced User Guide section, and the FPGA code provided with the kit.

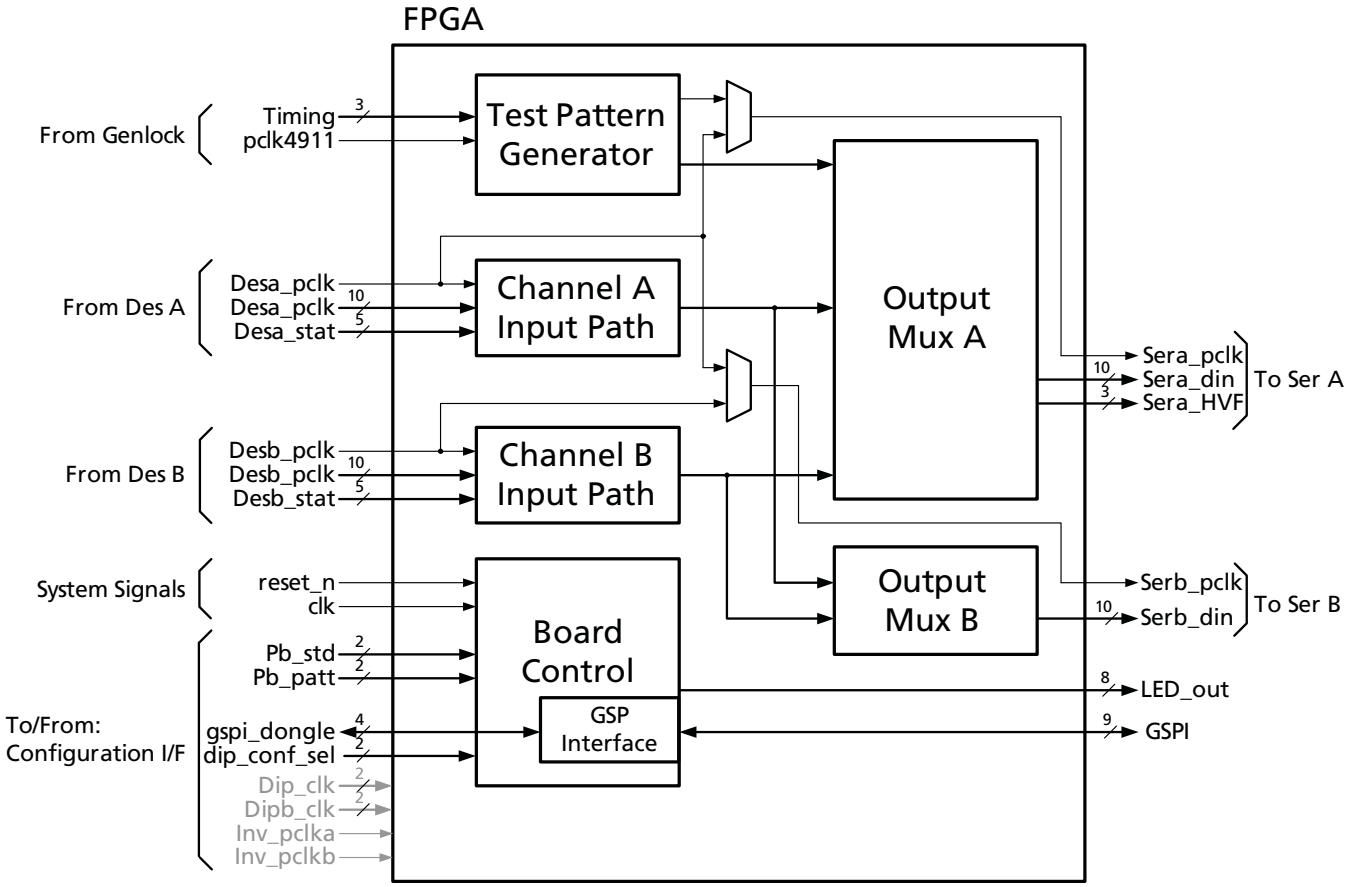

Figure 5-1: Simplified Top Level Architecture

5.2 Clock Tree and Data Path

Figure 5-2 illustrates the Test Pattern Generator data path, Receiver A Input Path, Receiver B Input Path, Output Muxing and Clock trees in detail.

The following design rules have been applied:

- Input data is captured by the DDRs in the I/O cells to ensure predictable timing margin
- Source synchronous output: DDR data and clock output both use DDR registers in the I/O cells to achieve constant phase-relation regardless of the FPGA package and mode settings
- All output data is clocked with an output from the FIFOs to achieve timing paths between input and output clocks

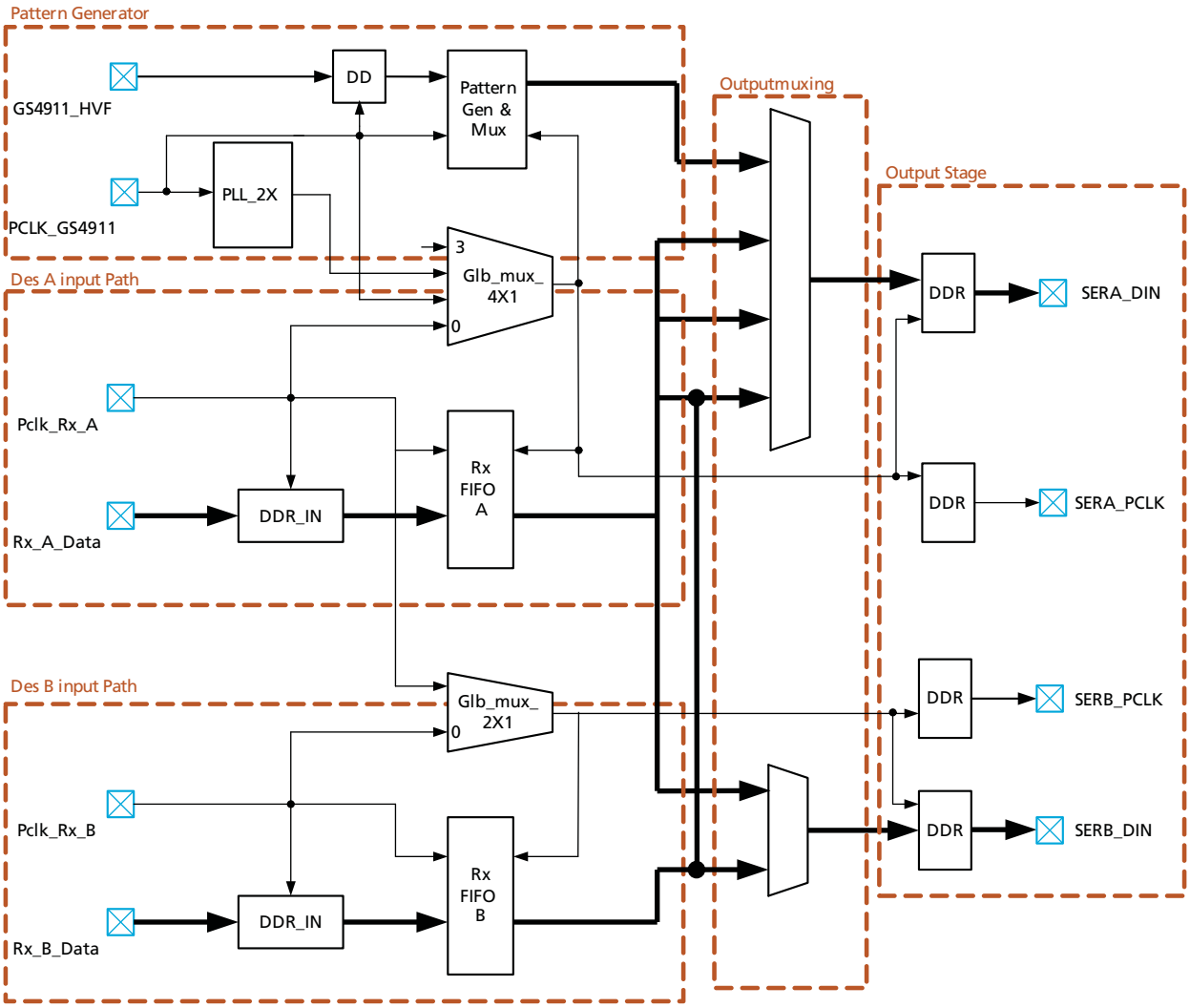

Figure 5-2: Clock and Data Path

On the FPGA, the Pattern Generator produces a video signal based on the clock (PCLK4911) and timing signals (FPGA internal name FVH_in or FPGA pad name Timing[2:0]) from the GS4911B. The output multiplexer selects an output among the A and B video streams and the Pattern Generator signal.

5.3 Pattern Generator

The pattern generator supports the sixteen HD/3G formats shown in Table 3-2, and the sixteen patterns shown in Table 3-3. The GS4911B on the 3Gb/s SDI Demo Board provides the pixel clock and timing signals (HVF). It can be set for either Free-run mode or Genlock-mode to an external sync signal. The output values of the video pattern generator are not bandwidth limited. When these patterns are displayed on an analog display, the transitions between bars can cause ringing of the video image at these transitions. If required, transitions can be limited by filtering the signal in the FPGA.

5.3.1 Top Level Architecture

Figure 5-3 illustrates the major blocks in the Pattern Generator, and the following items:

- The configuration signals from the control block of the FPGA on the left side
- The clock and timing signals from GS4911B
- The system level clock and reset signals
- The generated test pattern data/clock/timing and lock signals on the left side
- The data flow between the blocks

The PLL_X2 in the output muxing block generates 2x clock for all HD standards, since the GS4911B provides 1x clock while the Transmitter is wired for 10-bit mode, which results in a requirement of a 2x clock. Depending on the 3G or HD standard selected, the Pclk_Tx_A_sig will feed GS4911 clock or frequency-doubled GS4911 clock. The Pattern_Gen block generates a 20-bit YCbCr data stream for the selected standard and pattern.

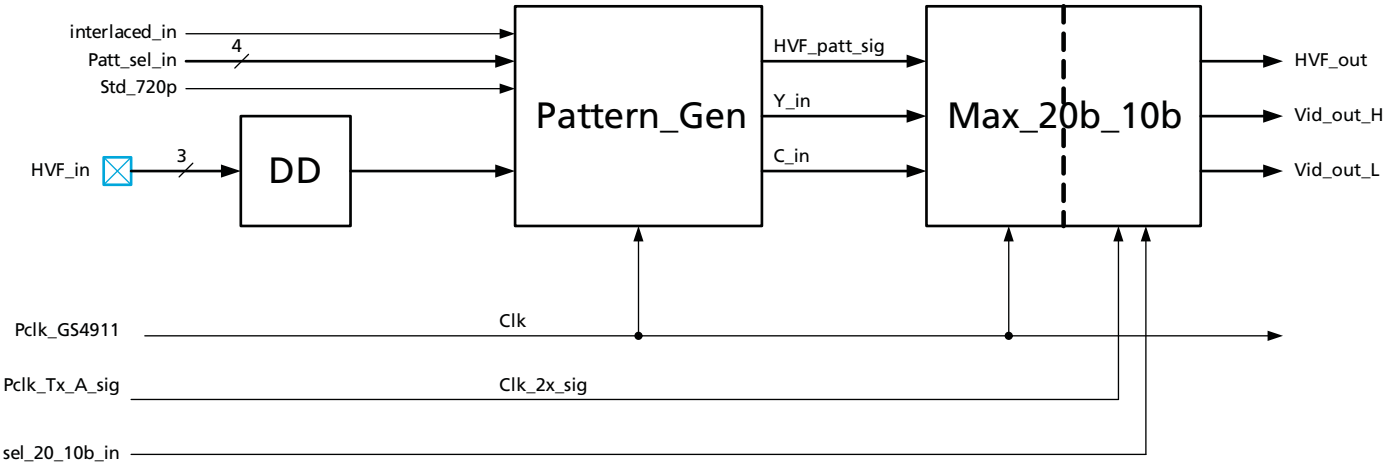

Figure 5-3: Pattern Generator Top Level Architecture

5.3.2 Colour Bar Generator

The Colour Bar Generator generates all patterns shown in Table 3-2 except Check Field/Pathological, which is generated by another sub-block (Gen_Path) in Pattern_Gen.

Figure 5-4 shows the signal flow of this sub-block.

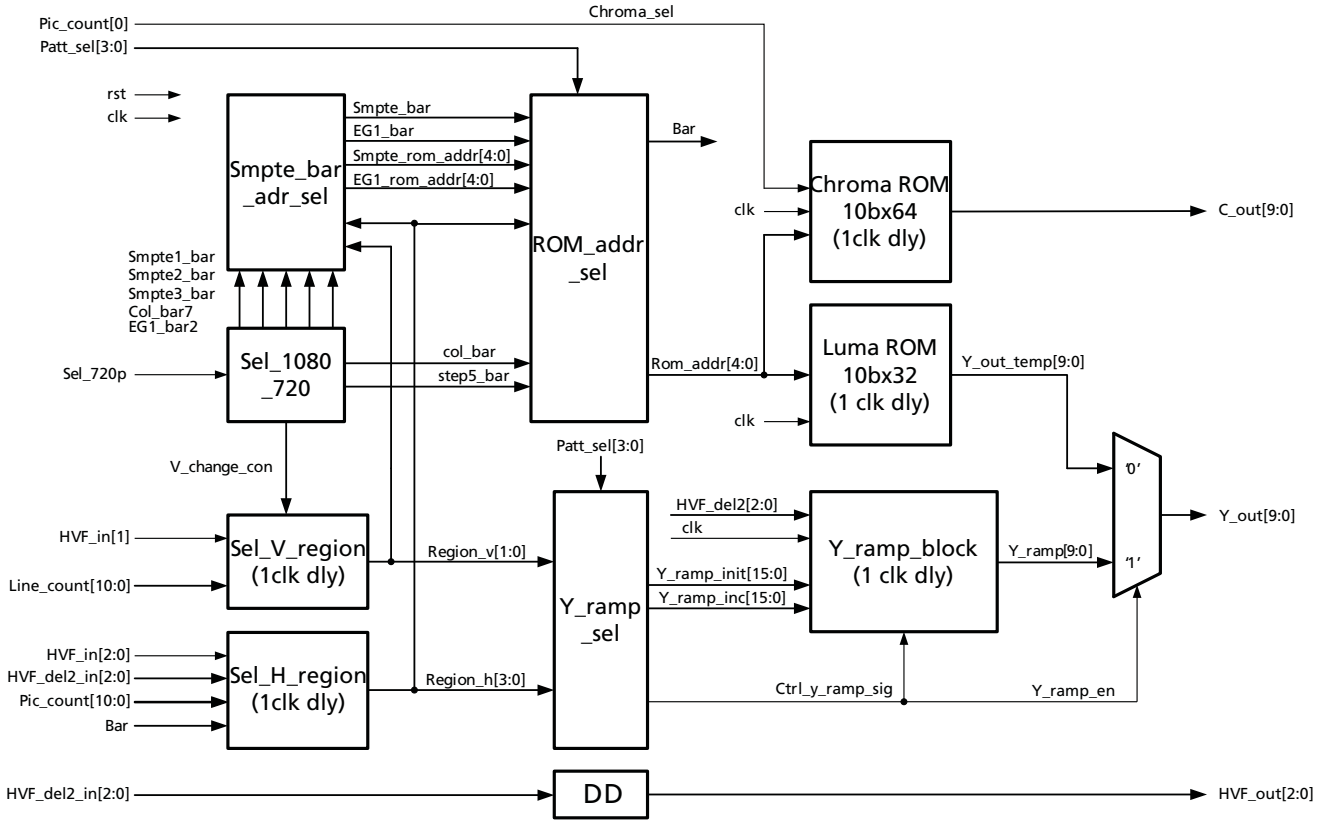

Figure 5-4: Colour Bar Generator in Pattern_Gen

5.3.3 20b to 10b Mux

The Max_20b_10b block multiplexes the 20-bit data onto a 10-bit bus for all HD standards. For all 3G standards, the 20-bit data flows through. The data output stage of the FPGA will multiplex 20-bit SDR (Single Data Rate) into a 10-bit DDR (Dual Data Rate) for all 3G standards.

YC_rd_sync sub-block is used to synchronize the H leading edge with the 10-bit chroma output.

After reset, this block will wait for the FIFO to be filled, and then it starts to read the data from both Y and C FIFO until the falling edge of the H is detected. It will set the sel_y_c properly for initial value and sel_y_c/sel_y_c_n will toggle on every clk_x2 thereafter.

The FIFOs were designed for the data to cross different clock domains.

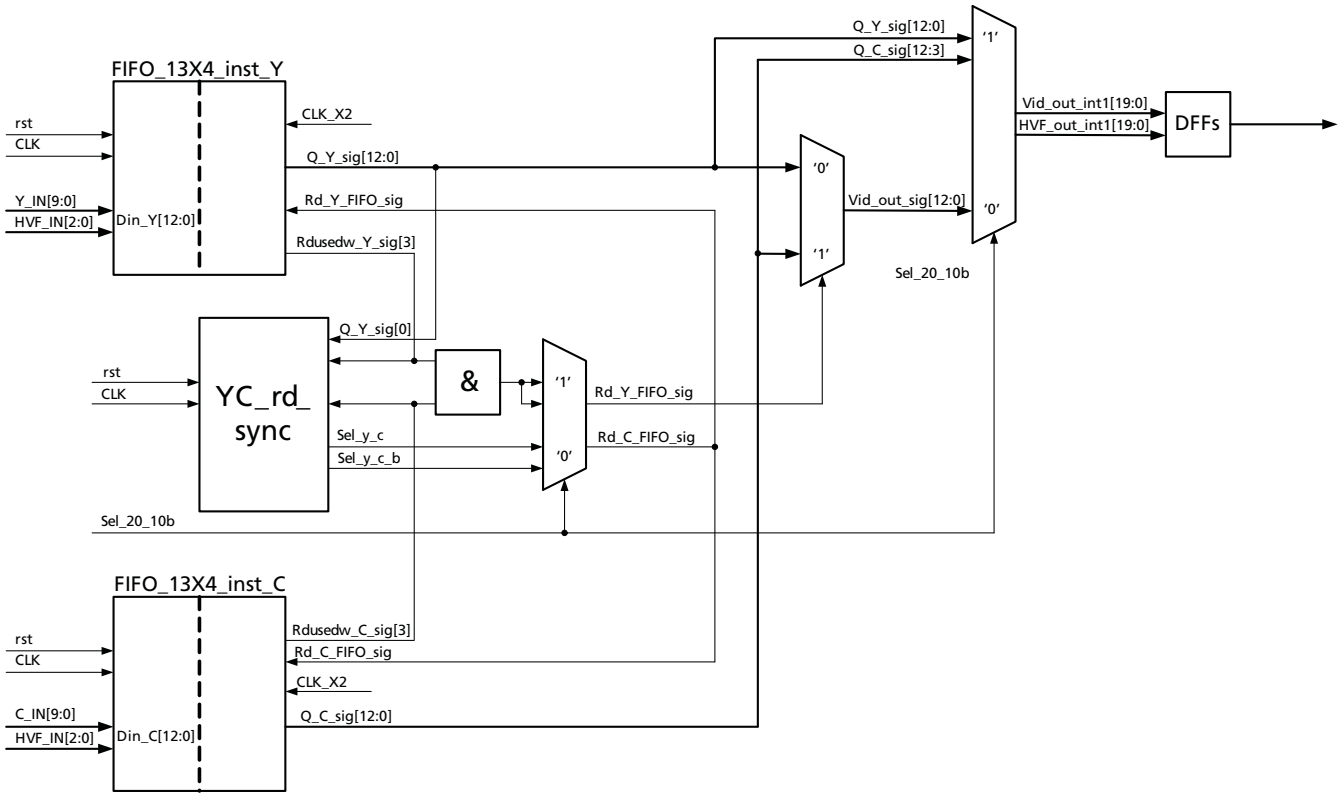

Figure 5-5: Mux_20_10b

5.4 Optical Module

An Optical Module connector and cage are provided on the Demo Board. The user may purchase an Optical Module for evaluation, but it is not supplied as part of this kit. The test wiring diagram of this module is shown in Figure 5-6. To test the Optical Module, follow the setup and procedure below.

Setup:

- Use a fibre cable for loop-back connection
- Operation Mode: Test Pattern Generator (SW3 bit1-3="ON-OFF-ON")
- Data Path: Pattern Generator on FPGA->Ser A->Optical Tx->Fibre->Optical Rx->Des B->FPGA->Ser B->SDI Monitor

Procedures:

To enable 3G mode, connect a 3Gb/s source to J6 (BIN1), remove the shunt on J14, power-up the boards, and then reset the boards. The FPGA will detect the rate on Des B and configure Ser B for 3G mode. Then change the test pattern standard/pattern for 3G and add the shunt on J14.

To enable HD mode, connect a HD source to J6 (BIN1), remove the shunt on J14, power-up the boards, and then reset the boards. The FPGA will detect the rate on Des B and configure Ser B for HD mode. Then change the test pattern standard/pattern for HD and add the shunt on J14.

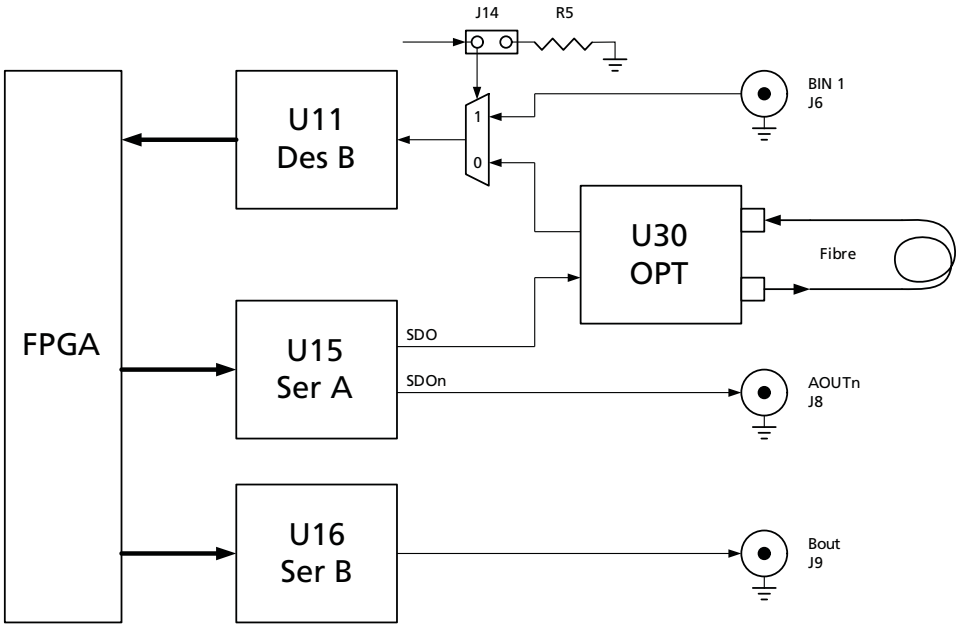

Figure 5-6: Optical Module Test Data Flow

5.5 Clock Termination

The FPGA drives the GS2972s in source-synchronous mode. All output data bits and clock signals use DDRs in the I/O cells to minimize the skew. There are some options for the clock implementation to achieve the data to clock setup/hold time required by the GS2972:

- Use a PLL to shift the clock by 90° to centre the clock edge in the data window. It provides the best timing margin, but uses FPGA PLL/BUFG clock resources and adds clock jitter
- Use the general routing resources in the FPGA to adjust the clock delay to centre the clock edge in the data window. This method does not use FPGA resources, but the clock routing has to be manually done on the FPGA each time with S&P&R (Synthesize, Place and Route pass)
- Use the drive-strength/slew-rate adjustment of the output buffers to shift data/clock; the delay adjustment through OBUF is very limited

5.6 Host Interface and Register Map

Host_if is a configuration and status register block accessible by PC through a GSPI dongle.

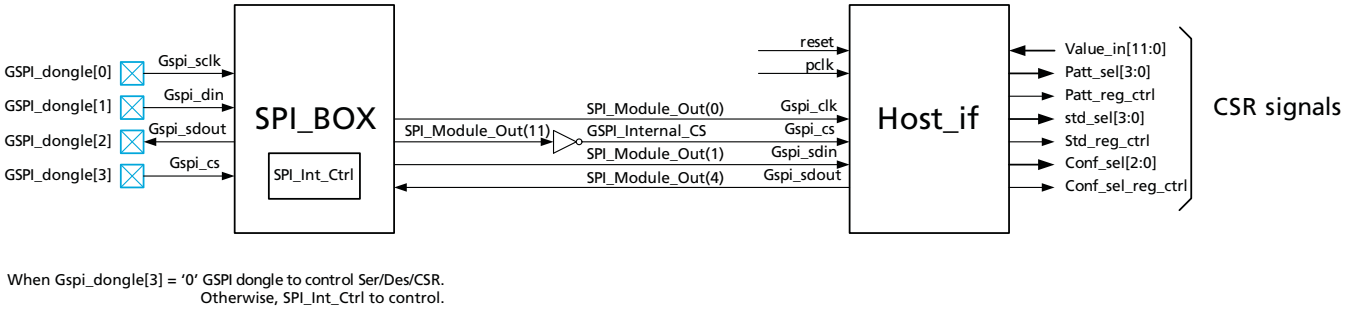

Figure 5-7: Host Interface Block Diagram

Table 5-1: Host Interface Register Map

Address	Register Name	Bits	Access	Reset Value	Valid Range	Descriptions
0	r0r.Patt_sel	3:0	R/W	0000	0 - 15	Pattern selection register
	r0r.Patt_reg_ctrl	4	R/W	0	0 - 1	0: Pattern is controlled by push buttons 1: Pattern is controlled by register
1	r1r.Std_sel	3:0	R/W	0000	0 - 15	Video standard register of the test pattern
	r1r.Std_reg_ctrl	4	R/W	0	0 - 1	0: Standard is controlled by push buttons 1: Standard is controlled by register
2	r2r.Conf_sel	2:0	R/W	000	0, 1, 4, 6, 7	Operation mode selection register
	r2r.Confi_sel_reg_ctrl	3	R/W	0	0 - 1	0: Operation mode is controlled by push buttons 1: Operation mode is controlled by register

Table 5-2 shows the ID values required to select specific devices on the 3G SDI Demo Board.

Table 5-2: Device Select Values

ID	Device
01	GS2970(A)
02	GS2970(B)
04	GS2972(A)
08	GS2972(B)
10	GS4911B
20	Internal Board Registers
80	I/O Expander

5.6.1 Graphical User Interface (GUI)

Figure 5-8 shows a screen shot of the GUI software.

NOTE: The operating mode for the DK-START-3C25N board can only be set with the GUI.

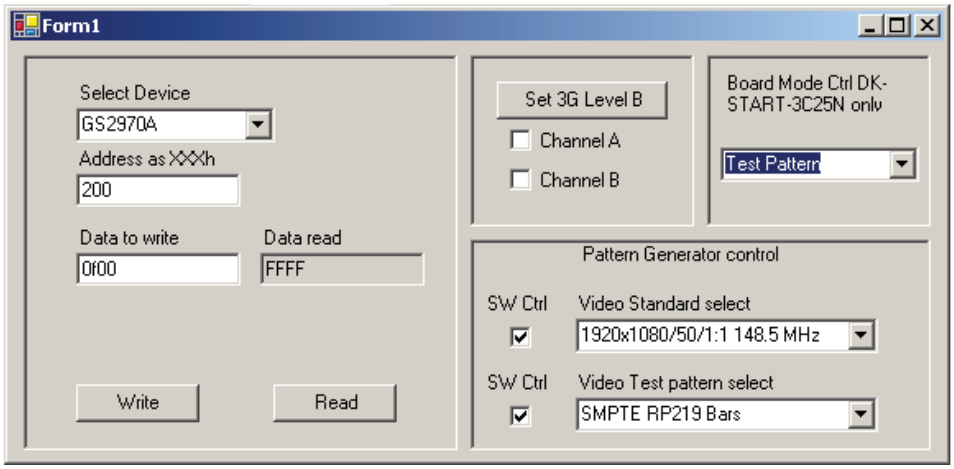

Figure 5-8: GUI Software Screen Shot

6. Related Documents

6.1 Gennum's Documentation

- GS2970 Datasheet (Doc ID 47478)
- GS2972 Datasheet (Doc ID 47479)
- GS4911B Datasheet (Doc ID 36655)
- GS2974B Datasheet (Doc ID 45062)
- GO2921 Datasheet (Doc ID 47116)
- GS2978 Datasheet (Doc ID 37186)
- FPGA code

6.2 Altera's Documentation

- cycloneIII_3c120_dev_reference_manual.pdf
- cycloneIII_3c25_dev_reference_manual.pdf
- Application Note 386: Using the Parallel Flash Loader with the Quartus II software.

7. Appendix

7.1 Schematics

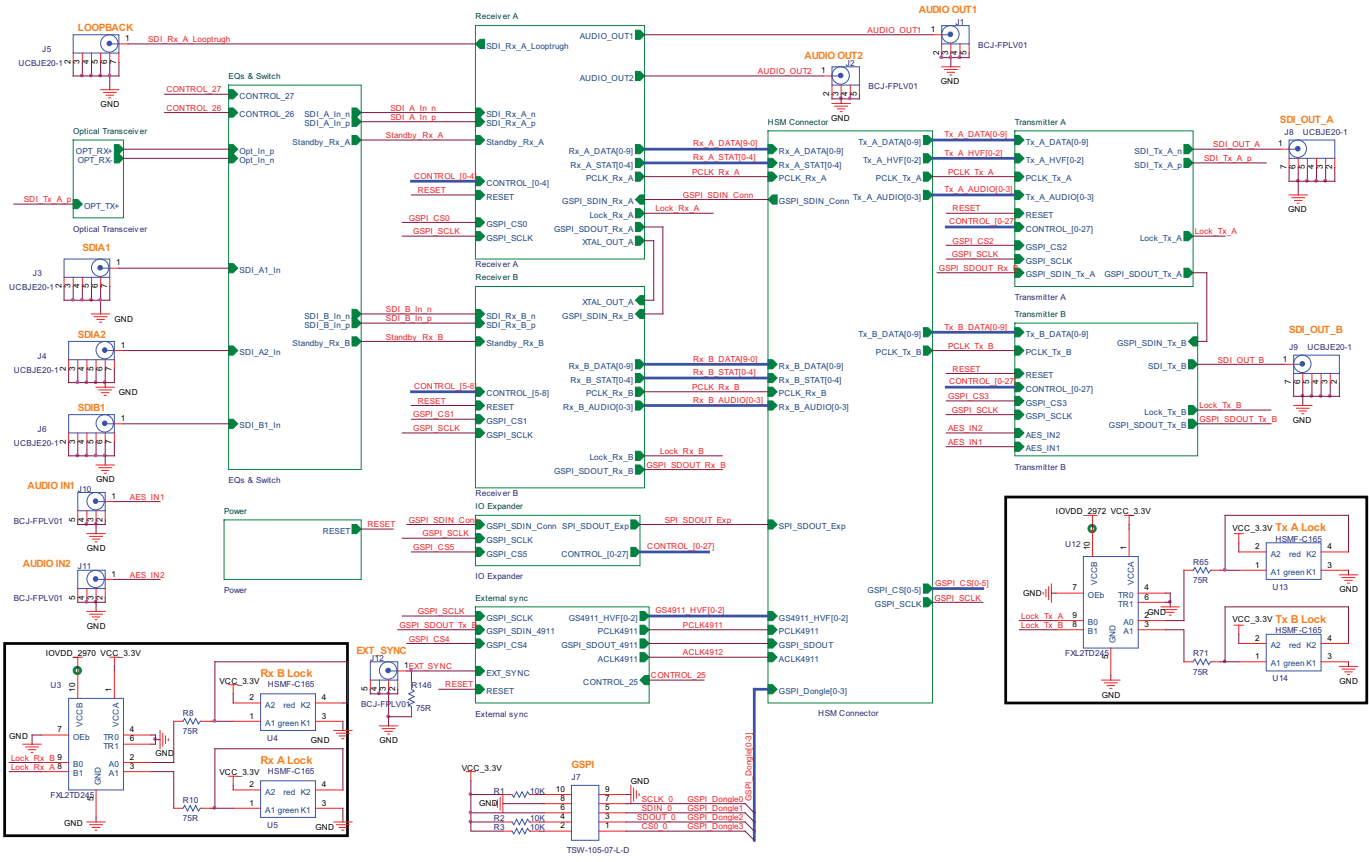

Figure 7-1: Top Schematic

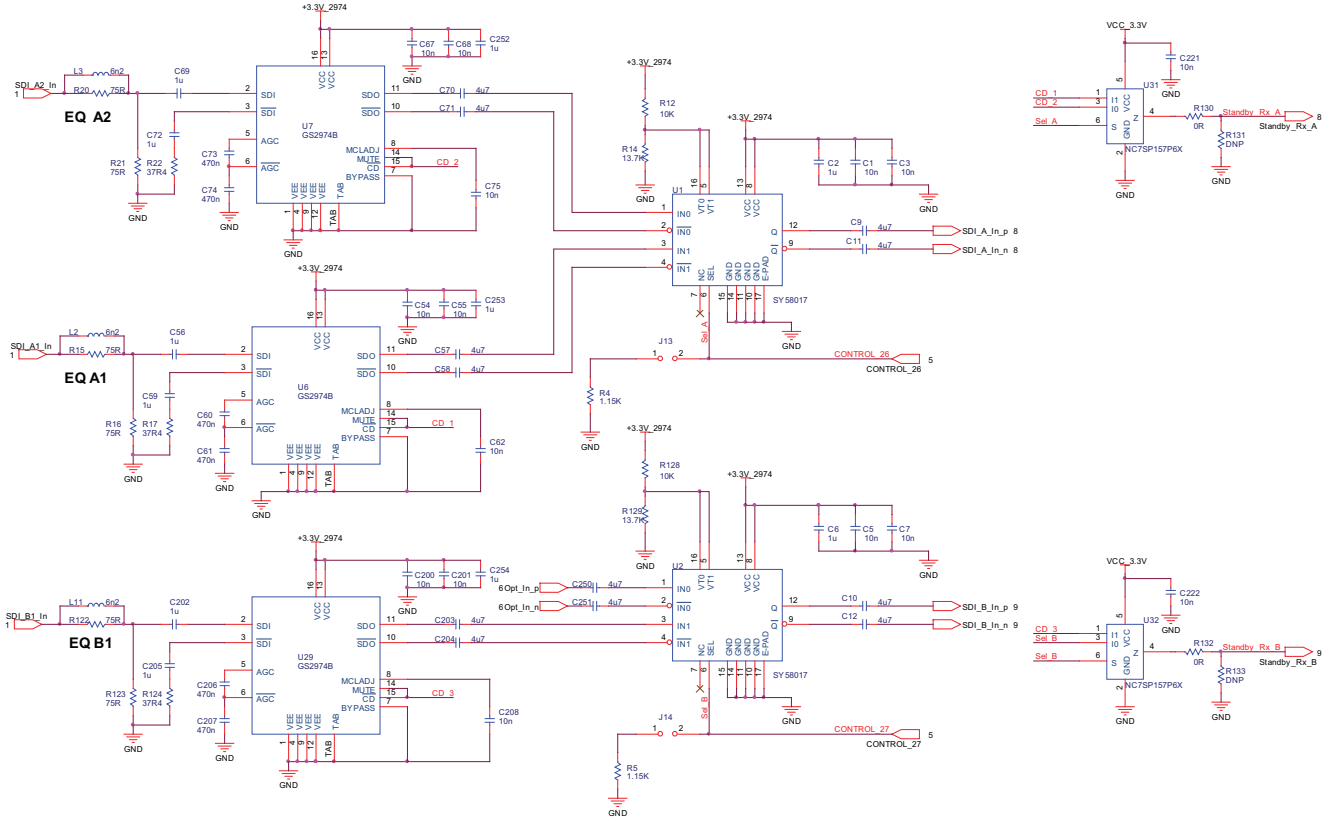

Figure 7-2: Equalizers

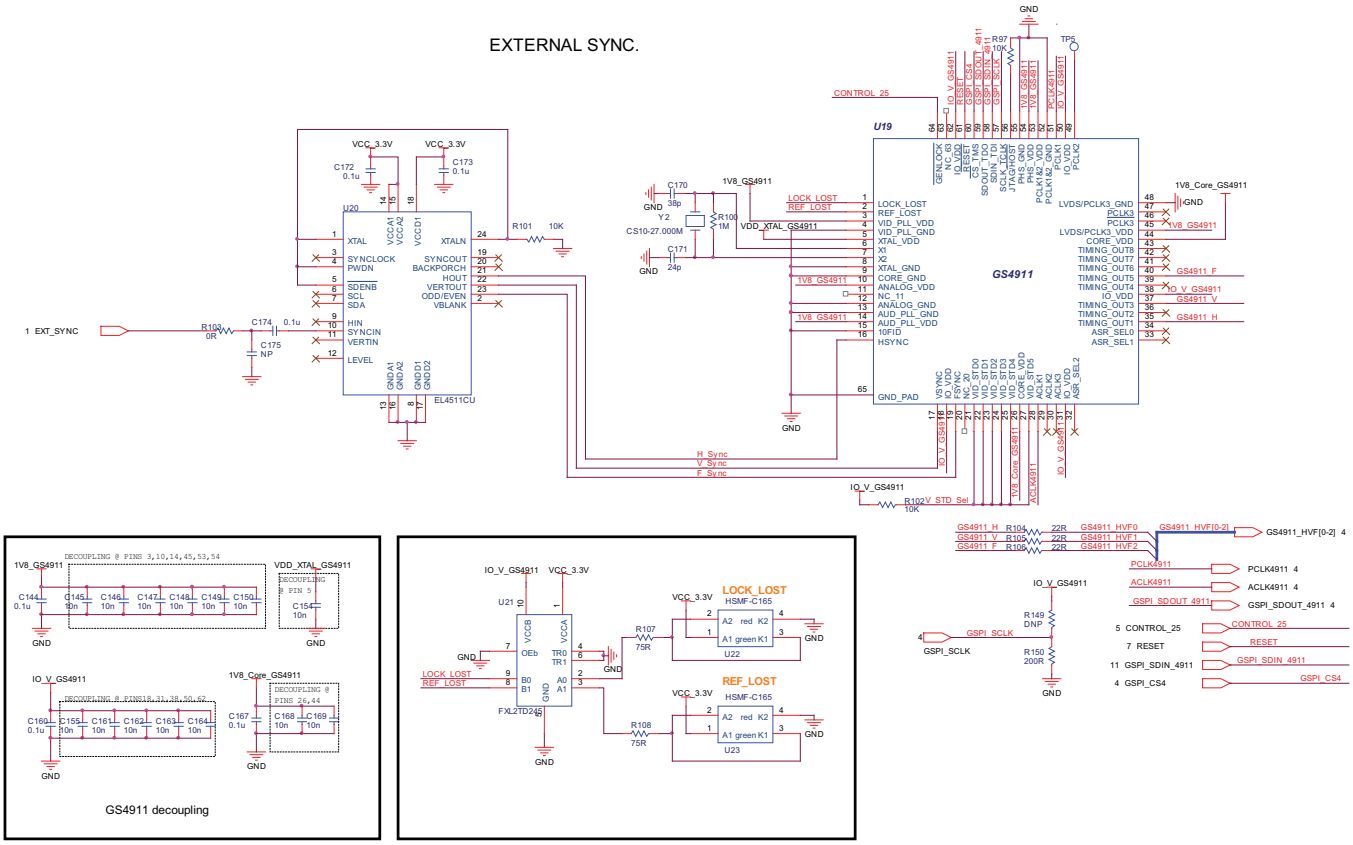

Figure 7-3: External Sync

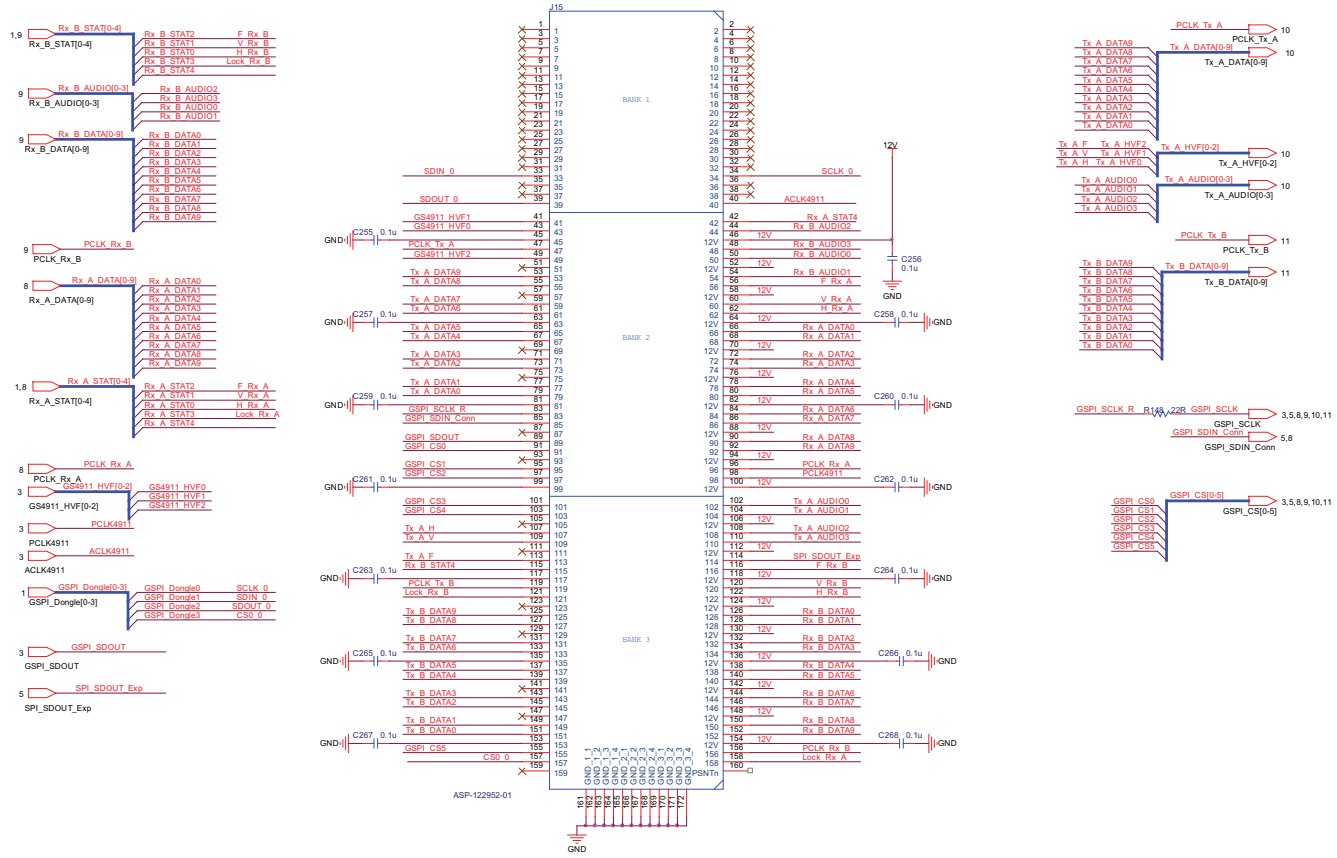

Figure 7-4: HSM Connector

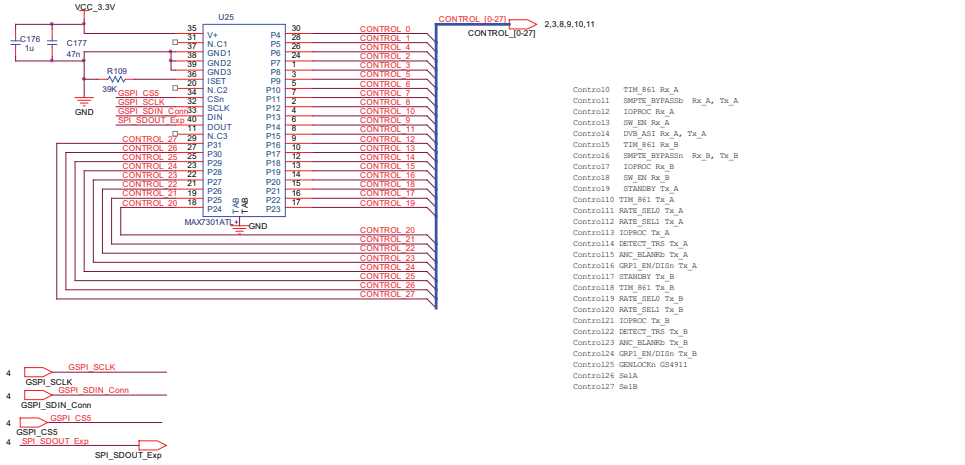

Figure 7-5: I/O Expander

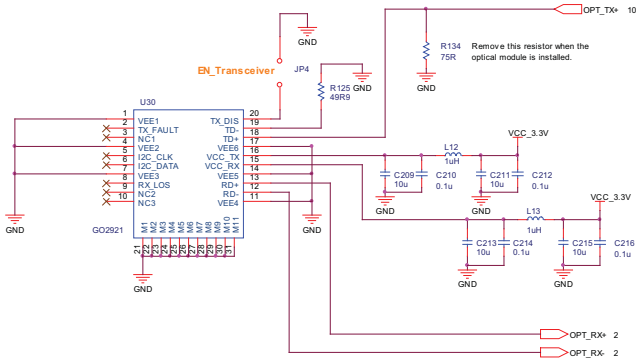

Figure 7-6: Optical Transceiver

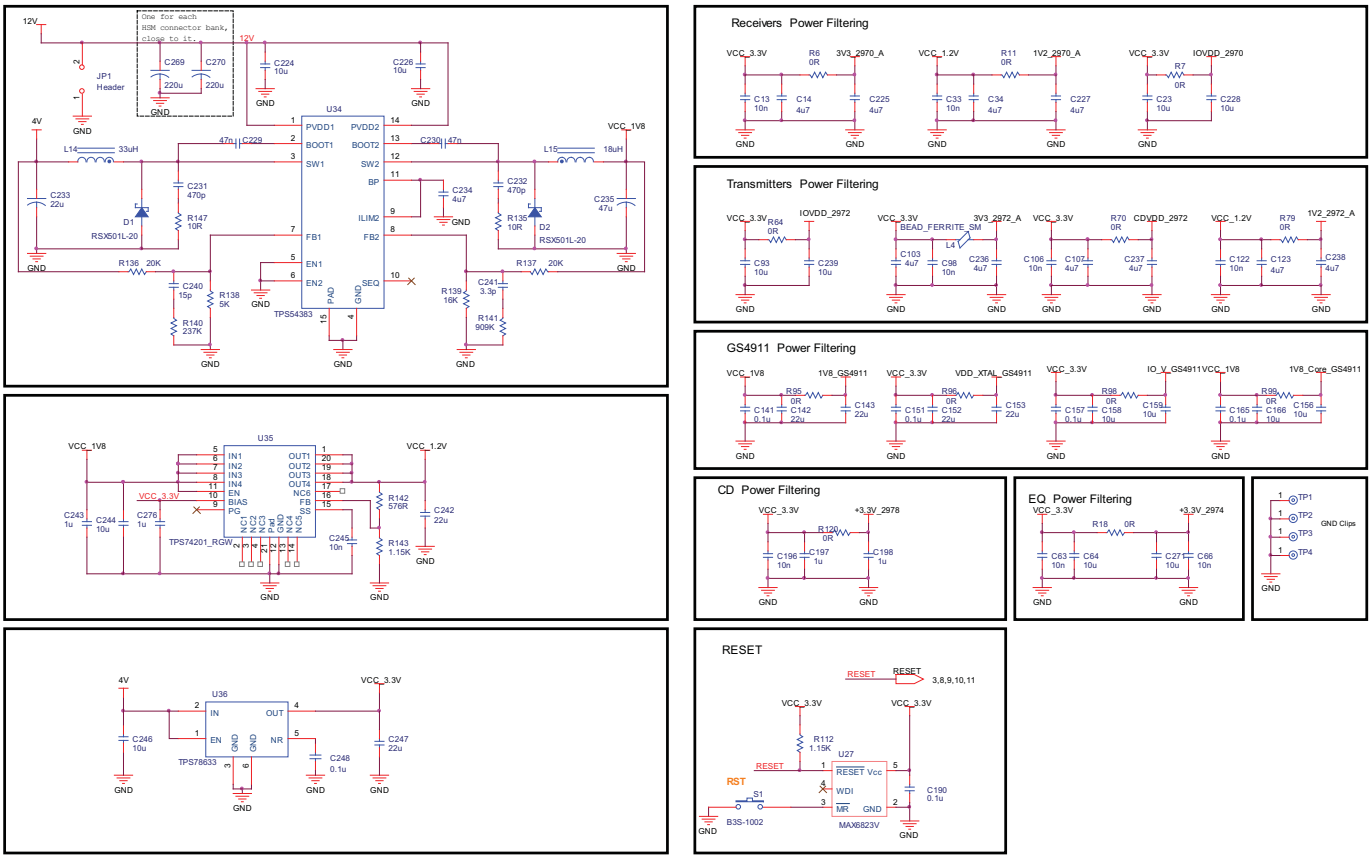

Figure 7-7: Power

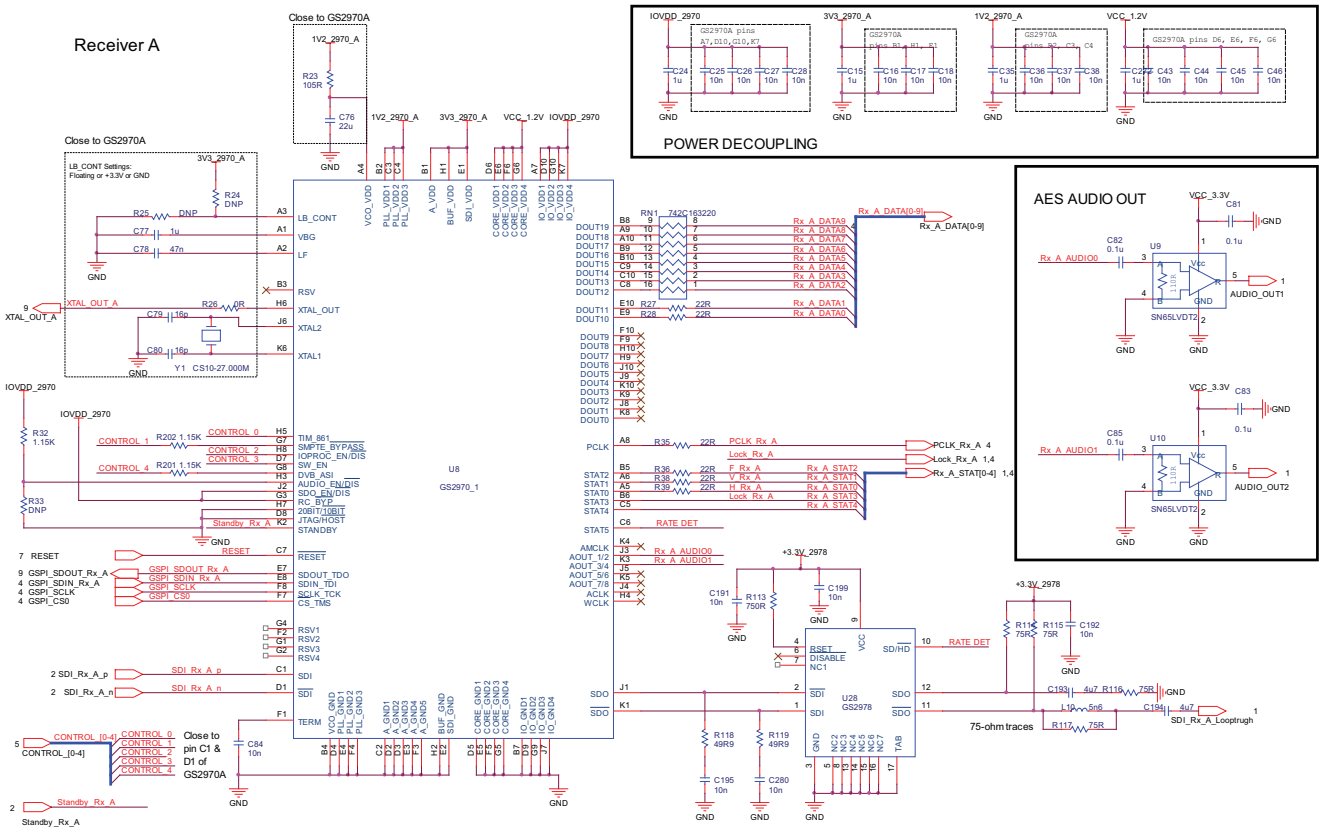

Figure 7-8: Receiver A

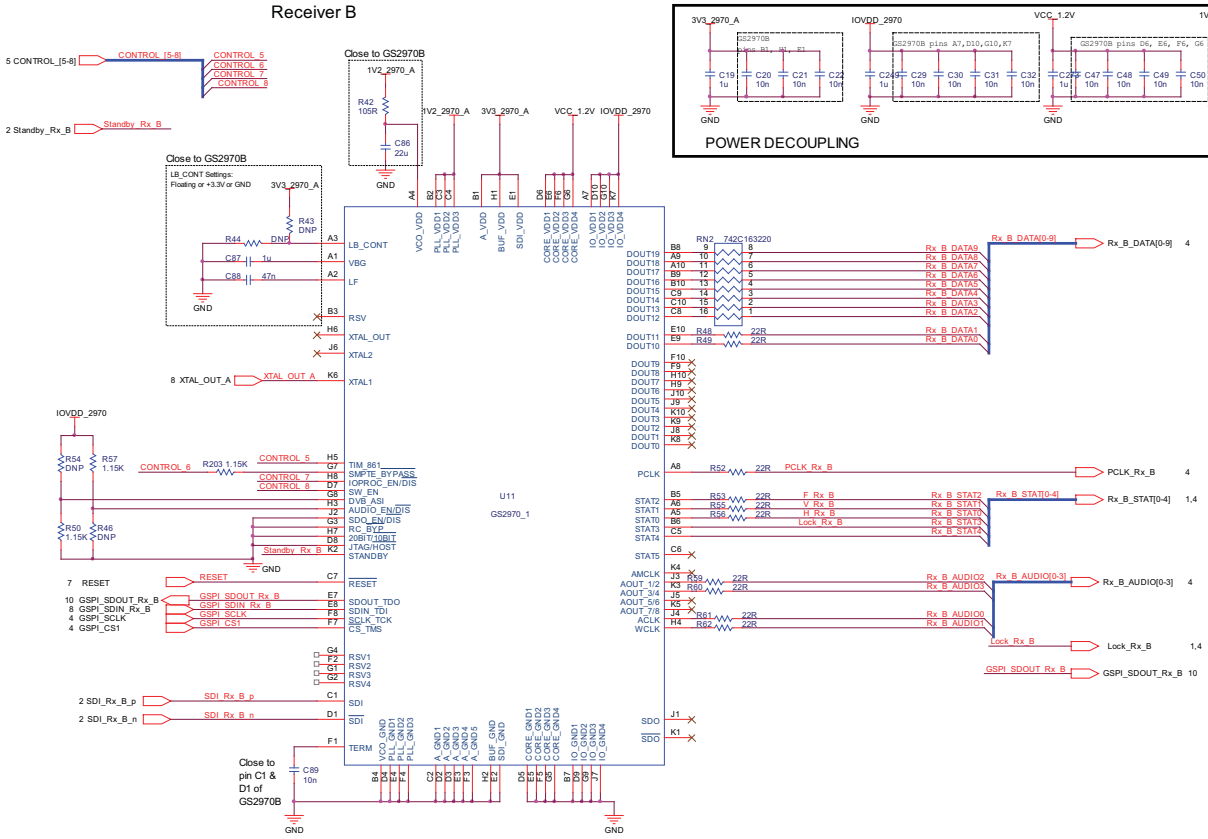

Figure 7-9: Receiver B

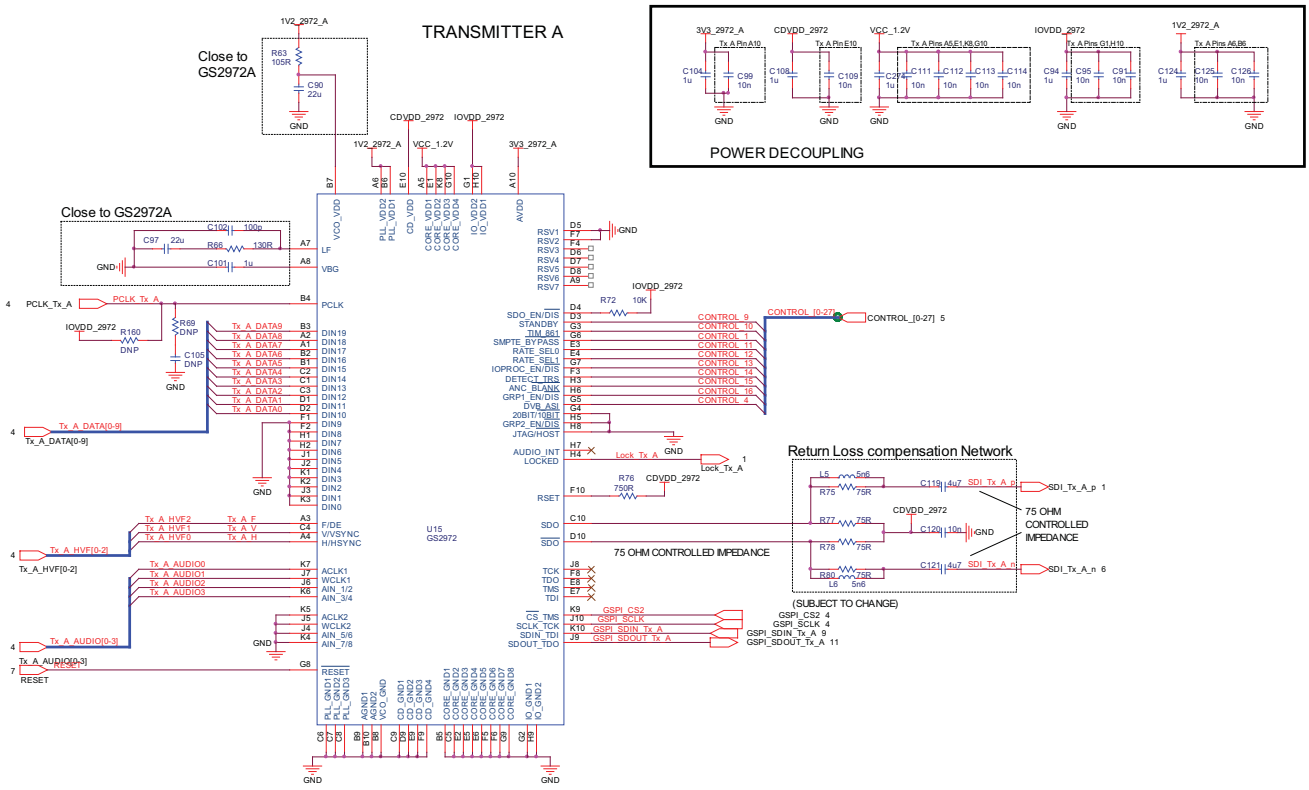

Figure 7-10: Transmitter A

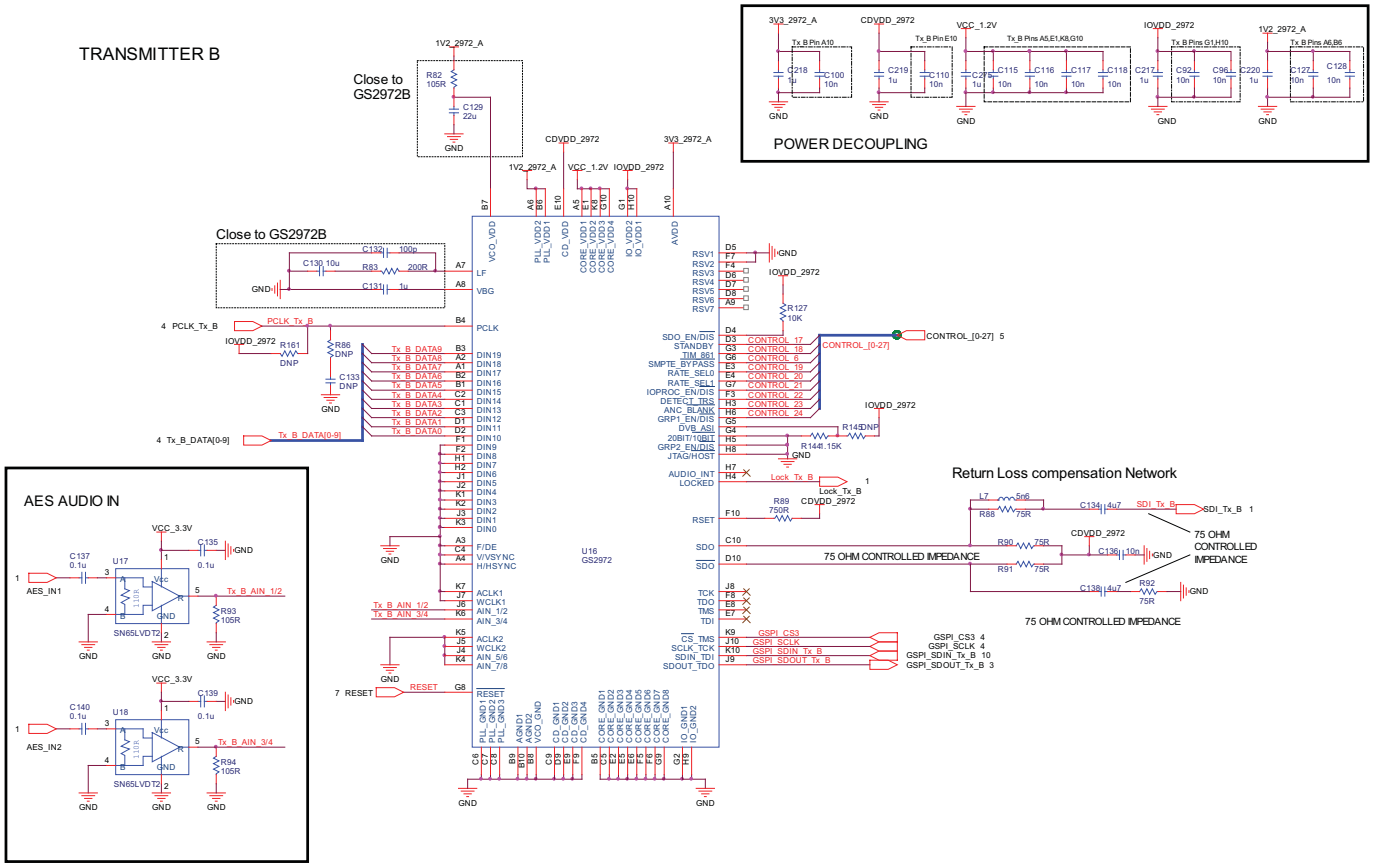

Figure 7-11: Transmitter B

7.2 Board Layout

The 3Gb/s SDI Demo Board is an 8-layer board with controlled impedance requirement. The layers are Top, Gnd1, Pwr1, Pwr2, Gnd2, Sig1, Gnd3 and Bottom. Figure 7-12 and Figure 7-13 show the Top and Bottom layers of the board. The Allegro brd file and Gerber files are provided as part of the kit where the details of all layers may be viewed.

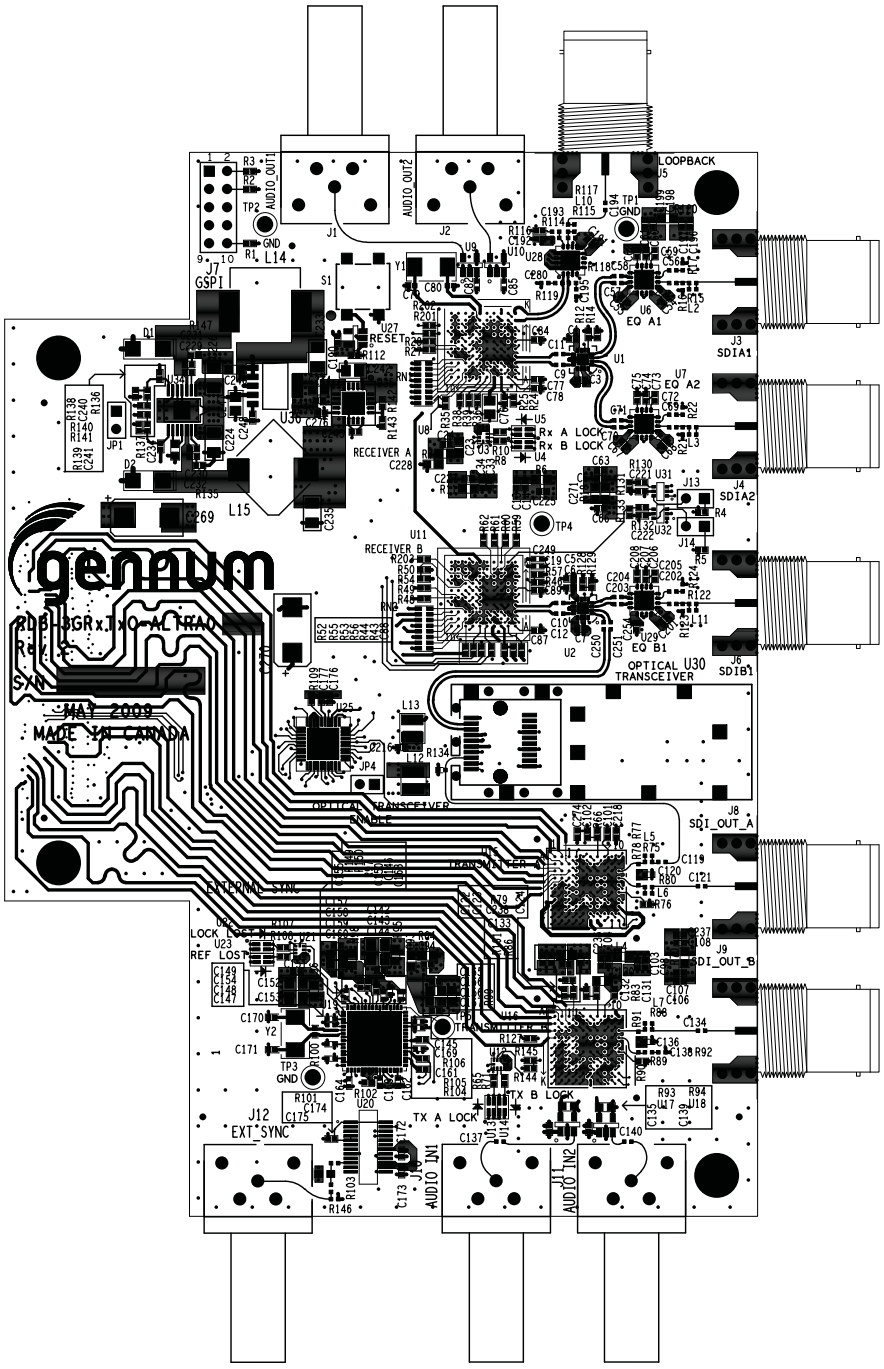

Figure 7-12: Top Layer

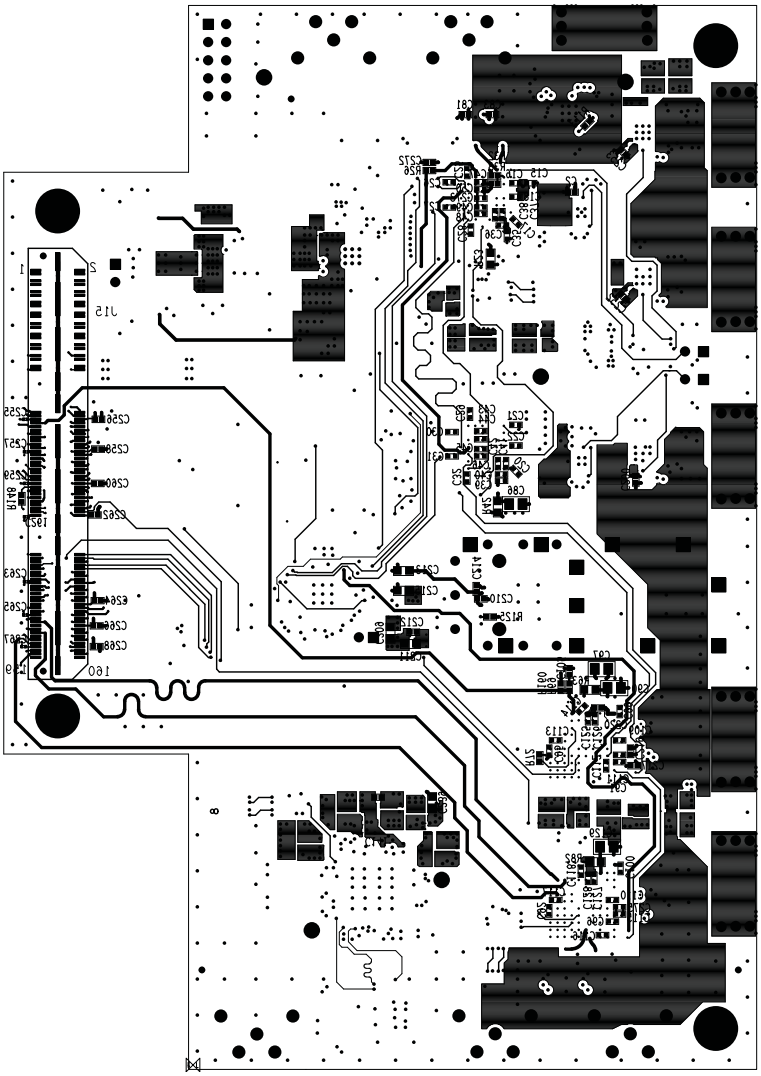

Figure 7-13: Bottom Layer

7.3 Bill of Materials

Table 7-1 lists all of the parts used on the 3Gb/s SDI Demo Board. For additional information of the parts, such as manufacturer and part numbers, please refer to the Excel spread sheet provided with the kit.

Table 7-1: Bill of Materials

Quantity	Reference Designator	Description
94	C1, C3, C5, C7, C13, C16, C17, C18, C20, C21, C22, C25, C26, C27, C28, C29, C30, C31, C32, C33, C36, C37, C38, C40, C41, C41, C42, C42, C43, C44, C45, C46, C47, C48, C49, C50, C54, C55, C62, C63, C66, C67, C68, C75, C84, C89, C91, C92, C95, C96, C98, C99, C100, C106, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C120, C122, C125, C126, C127, C128, C136, C145, C146, C147, C148, C149, C150, C154, C155, C161, C162, C163, C164, C168, C169, C191, C192, C195, C196, C199, C200, C201, C208, C221, C222, C245	Capacitor; ceramic 10000pF 16V 10% X7R 0402
38	C2, C6, C15, C19, C24, C35, C39, C56, C59, C69, C72, C77, C87, C94, C101, C104, C108, C124, C131, C176, C197, C198, C202, C205, C217, C218, C219, C220, C243, C249, C252, C253, C254, C272, C273, C274, C275, C276	Capacitor; ceramic 1µF 10V X5R 0402
28	C9, C10, C11, C12, C14, C34, C57, C58, C70, C71, C103, C107, C119, C121, C123, C134, C138, C193, C194, C203, C204, C225, C227, C236, C237, C238, C250, C251	Capacitor; ceramic 4.7µF 6.3V X5R 0402
17	C23, C64, C93, C130, C156, C158, C159, C166, C209, C211, C213, C215, C228, C239, C244, C246, C271	Capacitor; ceramic 10µF 6.3V X5R 0603
6	C60, C61, C73, C74, C206, C207	Capacitor; ceramic 0.47µF 6.3V X5R 0402
11	C76, C86, C90, C97, C129, C242, C247, C142, C143, C152, C153	Capacitor; ceramic 22µF 10V X5R 0805
5	C78, C88, C177, C229, C230	Capacitor; ceramic 47000pF 16V X7R 0402
2	C79, C80	Capacitor; ceramic 16pF 50V 0402 UHI Q
24	C81, C82, C83, C85, C135, C137, C139, C140, C141, C144, C151, C157, C160, C165, C167, C172, C173, C174, C190, C210, C212, C214, C216, C248	Capacitor; ceramic 0.10µF 10V X7R 0402
2	C102, C132	Capacitor; ceramic 100pF 25V NP0 0402
1	C170	Capacitor; ceramic 39pF 50V 5% COG 0402
1	C171	Capacitor; ceramic 24pF 50V C0G 0402
2	C224, C226	Capacitor; ceramic 10µF 25V X5R 1206
2	C231, C232	Capacitor; ceramic 470pF 25V 0402 SMD
1	C233	Capacitor; tantalum 22µF 10V 20% SMD
1	C234	Capacitor; ceramic 4.7µF 10V X5R 0603
1	C235	Capacitor; tantalum 47µF 6.3V 20% SMD
1	C240	Capacitor; ceramic 15pF 25V C0G 0402
1	C241	Capacitor; ceramic 3.3pF 25V C0G 0402
7	C255, C257, C259, C261, C263, C265, C267	Capacitor; ceramic 0.1µF 6.3V X5R 0201

Table 7-1: Bill of Materials

Quantity	Reference Designator	Description
7	C256, C258, C260, C262, C264, C266, C268	Capacitor; ceramic 0.1µF 16V 10% X5R 0402
2	C269, C270	Capacitor; tantalum 220µF 16V 10% LOESR SMD
1	C280	Capacitor; ceramic 10000pF 16V 10% X7R 0402
2	D1, D2	Diode; shottky 25V 5A SOD-106 TR
2	JP1, JP4	Header 2mm 1x2
5	J1, J2, J10, J11, J12	Connector, 75Ω BNC; front chassis-mount right-angle
6	J3, J4, J5, J6, J8, J9	Connector; RF/Coaxial
1	J7	Connector, header; 10-position 0.100" DL gold
2	J13, J14	Connector, header; 0.100 single STR 36-position
1	J15	Connector, Samtec ASP-122952-01
3	L2, L3, L11	Inductor; 6.2nH 300mA 0402
1	L4	Filter Chip; 120Ω 3A 0603
4	L5, L6, L7, L10	Inductor; 5.6nH 300mA 0402
2	L12, L13	Inductor; 1.0µH 20% 445mA 1210
1	L14	Inductor; power shield 33µH SMD
1	L15	Coil; power choke 18µH 2.5A SMD
2	RN1, RN2	Resistor, array; 22Ω 16-term 8RES SMD
10	R1, R2, R3, R12, R72, R97, R101, R102, R127, R128	Resistor; 10kΩ 1/16W 5% 0402 SMD
11	R4, R5, R32, R50, R57, R112, R143, R144, R201, R202, R203	Resistor; 1.15kΩ 1/16W 1% 0402 SM
12	R6, R7, R11, R18, R64, R70, R79, R95, R96, R98, R99, R120	Resistor; 0Ω 1/10W 5% 0402 SMD
26	R8, R10, R15, R16, R20, R21, R65, R71, R75, R77, R78, R80, R88, R90, R91, R92, R107, R108, R114, R115, R116, R117, R122, R123, R134, R146	Resistor; 75.0Ω 1/16W 1% 0402 SMD
2	R14, R129	Resistor; 13.7kΩ 1/16W 1% 0402 SMD
3	R17, R22, R124	Resistor; 37.4Ω 1/16W 1% 0402 SMD
1	R23	Resistor; 105Ω 1/10W 1% 0603 SMD
4	R26, R103, R130, R132	Resistor; 0Ω 1/10W 5% 0402 SMD
20	R27, R28, R35, R36, R38, R39, R48, R49, R52, R53, R55, R56, R59, R60, R61, R62, R104, R105, R106, R148	Resistor; 22.0Ω 1/16W 1% 0402 SMD
5	R42, R63, R82, R93, R94	Resistor; 105Ω 1/10W 1% 0603 SMD
1	R66	Resistor; 130Ω 1/10W 0.5% 0402 SMD
3	R76, R89, R113	Resistor; 750Ω 1/16W 1% 0402 SMD
2	R83, R150	Resistor; 200Ω 1/16W 1% 0402 SMD
1	R100	Resistor; 1.00MΩ 1/16W 1% 0402 SMD
1	R109	Resistor; 10kΩ 1/16W 5% 0402 SMD

Table 7-1: Bill of Materials

Quantity	Reference Designator	Description
3	R118, R119, R125	Resistor; 49.9Ω 1/16W 1% 0402 SMD
2	R135, R147	Resistor; 10Ω 1/16W 1% 0402 SMD
2	R136, R137	Resistor; 20kΩ 1/16W 1% 0402 SMD
1	R138	Resistor; 4.99kΩ 1/16W 0.1% 0402 SMD
1	R139	Resistor; 16.0kΩ 1/16W 1% 0402 SMD
1	R140	Resistor; 237kΩ 1/16W 1% 0402 SMD
1	R141	Resistor; 909kΩ 1/16W 1% 0402 SMD
1	R142	Resistor; 576Ω 1/16W 1% 0402 SMD
1	S1	Switch; tact 6mm 160GF H=4.3mm
4	TP1, TP2, TP3, TP4	Clips
1	TP5	Test point
2	U1, U2	IC; MUX 2:1 DIFF PREC HS 16-MLF
3	U3, U12, U21	Translator; 2-bit LV DL 10MICROPAK
6	U4, U5, U13, U14, U22, U23	Agilent HSMF-C165 Miniature Bi-colour Surface Mount Chip LED
3	U6, U7, U29	Gennum GS2974B Adaptive Cable Equalizer
2	U8, U11	Gennum GS2970 3G/HD/SD-SDI Deserializer
4	U9, U10, U17, U18	IC; diff line DVR/RCVR HS SOT23-5
2	U13, U14	Agilent HSMF-C165 Miniature Bi-colour Surface Mount Chip LED
2	U15, U16	Gennum GS2972 3G/HD/SD-SDI Serializer
1	U19	Gennum GS4911B Clock and Timing Generator
1	U20	IC; VID Sync Separator HDTV 24QSOP
1	U24	IC; I/O Port Expander 40-TQFN
1	U25	IC; LDO REG 1.5A w/prog SS 20QFN
1	U26	IC; REG LDO 500mA 1.8V TSOT23-5
1	U28	Gennum GS2978 Cable Driver
1	U30	Connector and Cage for Gennum SFP Optical Module
2	U31, U32	IC; MUX ULP 2-inp noninv SC70-5
1	U34	TPS54383
1	U35	IC; LDO regulator 1.5A w/prog SS 20QFN
1	U36	IC; LDO regulator 3.3V 1.5A SOT223
2	Y1, Y2	Crystal; 27.0000 MHz 18pF SMD

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