LOW-JITTER SAW OSCILLATOR (SPSO)

OUTPUT : LV-PECL, LVDS, HCSL

EG - 2121 / 2102CA

- Frequency range : 53.125 MHz to 700 MHz
- Supply voltage : 2.5 V ··· EG-2121CA
  3.3 V ··· EG-2102CA
- Output : LV-PECL or LVDS or HCSL
- Function : Output enable (OE)
- External dimensions : 7.0 × 5.0 × 1.2 mm

- Very low jitter and low phase noise by SAW unit.

Pb Free RoHS Compliant

Product Number (please contact us)
EG-2121CA: Q3805CAx0xxxx00
: X1M000101xxxx00
EG-2102CA: Q3806CA00xxxx00
: X1M000091xxxx00

Actual size

EG-2121CA

EG-2102CA

Specifications (characteristics)

▶Differential LV-PECL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		LV-PECL		
Output frequency range	f_0	53.125 MHz to 500 MHz	100 MHz to 700 MHz	Please contact us about available frequencies.
Supply voltage	V_{CC}	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +100 °C		Storage as single product.
Operating temperature	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	I_{CC}	80 mA Max.	100 mA Max.	OE=V_{CC}, L_ECL=50 Ω
Disable current	I_dis	20 mA Max.	32 mA Max	OE=GND
Symmetry	SYM	P:40 % to 60 % (f_0 > 350 MHz)	P:45 % to 55 %	at outputs crossing point
		P:45 % to 55 % (f_0 ≤ 350 MHz)		
		D:48 % to 52 % (f_0 ≤ 175 MHz)	D:48 % to 52 % (f_0 ≤ 350 MHz)	
Output voltage	V_{OH}	1.55 V Typ.	2.35 V Typ.	DC characteristics
		V_{CC}-1.025 V to V_{CC}-0.88 V		
	V_{OL}	0.8 V Typ.	1.6 V Typ.	
		V_{CC}-1.81 V to V_{CC}-1.62 V		
Output load condition (ECL)	L_ECL	50 Ω		Terminated to V_{CC} -2.0 V
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal
	V_{IL}	30 % V_{CC} Max.		
Rise time / Fall time	t_r / t_f	400 ps Max.		Between 20% and 80% of (V_{OH}-V_{OL})
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t_{PJ}	0.8 ps Max.		f_0 < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ f_0 < 200 MHz; Offset frequency: 12 kHz to 20 MHz
		0.3 ps Max.		200 MHz ≤ f_0; Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, V_{CC}=2.5 V,3.3 V

▶LVDS Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		LVDS		
Output frequency range	f_0	53.125 MHz to 700 MHz		Please contact us about available frequencies.
Supply voltage	V_{CC}	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +100 °C		Storage as single product.
Operating temperature	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	I_{CC}	30 mA Max	45 mA Max.	OE=V_{CC}, L_LVDS= 100 Ω
Disable current	I_dis	20 mA Max	30 mA Max.	OE=GND
Symmetry	SYM	L:40 % to 60 % (f_0 > 350 MHz)	L:40 % to 60 % (f_0 > 350 MHz)	at outputs crossing point
		L:45 % to 55 % (f_0 ≤ 350 MHz)	L:45 % to 55 % (f_0 ≤ 350 MHz)	
		V:48 % to 52 % (f_0 ≤ 175 MHz)	V:48 % to 52 % (f_0 ≤ 175 MHz)	
Output voltage	V_{OD}	350 mV Typ. 247 mV to 454 mV		V_{OD1}, V_{OD2}; DC characteristics
	dVOD	50 mV Max.		dVOD = | V_{OD1}-V_{OD2} |
	V_{OS}	1.25 V Typ. 1.125 V to 1.375 V		V_{OS1}, V_{OS2}
	dVOS	150 mV Max.		dVOS = | V_{OS1}-V_{OS2} |
Output load condition (LVDS)	L_LVDS	100 Ω		Connected between OUT to $\overline{OUT}$
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal
	V_{IL}	30 % V_{CC} Max.		
Rise time / Fall time	t_r / t_f	400 ps Max.		Between 20 % and 80 %of Differential Output Peak to Peak voltage
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t_{PJ}	0.8 ps Max.		f_0 < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ f_0 < 200 MHz; Offset frequency: 12 kHz to 20 MHz
		0.3 ps Max.		200 MHz ≤ f_0; Offset frequency: 12 kHz to 20 MHz
Frequency aging	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, V_{CC}=2.5 V,3.3 V

►HCSL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		HCSL		
Output frequency range	f_0	100 MHz to 350 MHz		Please contact us about available frequencies.
Supply voltage	V_{CC}	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +125 °C		Storage as single product.
Operating temperature	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	I_{CC}	80 mA Max.	85 mA Max.	OE=V_{CC},L_HCSL=50 Ω
Disable current	I_dis	20 mA Max.	35 mA Max	OE=GND
Symmetry	SYM	45 % to 55 %		at outputs crossing point
Output Voltage	V_{OH}	0.75 V Typ.		DC characteristics
	V_{OL}	-0.3 V Typ.		
Output load condition (HCSL)	L_HCSL	50 Ω		Terminated to GND
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal
	V_{IL}	30 % V_{CC} Max.		
Rise time / Fall time	t_r / t_f	500 ps Max.		Between 0.175 V and 0.525 V of output
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t_{PJ}	0.8 ps Max.		f_0 < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ f_0 < 200 MHz
		0.3 ps Max.		200 MHz ≤ f_0
Frequency aging *2	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, V_{CC}=2.5 V,3.3 V

Product Name EG-2121 CA 250.000000MHz P G P A

(Standard form) ① ② ③ ④⑤⑥⑦

①Model ②Package type ③Frequency

④Output/Symmetry ⑤Frequency tolerance ⑥Operating temperature

⑦Frequency aging (A*1: Frequency tolerance include aging, N*2: Frequency tolerance exclude aging)

*1 This includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, and aging(+25 °C,10 years).
*2 This includes initial frequency tolerance, temperature variation, supply voltage variation, and reflow drift(except aging).
(⑤⑥⑦: GRA, GSA are not available)
(⑤⑥: As for LV-PECL and LVDS output, for 53.125 MHz ≤ f_0 < 100 MHz only HP is available)

④ Symbol	Output	Symmetry EG-2121CA	Symmetry EG-2102CA
P	LV-PECL	40 % to 60 %(f_0 > 350 MHz) 45 % to 55 %(f_0 ≤ 350 MHz)	45 % to 55 %
D	LV-PECL	48 % to 52 %(f_0≤ 175 MHz)	48 % to 52 %(f_0 ≤ 350 MHz)
L	LVDS	40 % to 60 %(f_0 > 350 MHz) 45 % to 55 %(f_0 ≤ 350 MHz)	
V	LVDS	48 % to 52 %(f_0 ≤ 175 MHz)	
H	HCSL	45 % to 55 %	

⑤Frequency tolerance	
G	±50 × 10^{-6}
H	±100 × 10^{-6}

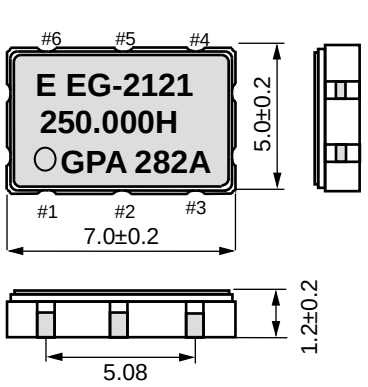
⑥Operating temperature	
P	0 to +70°C
R	-5 to +85°C
S	-20 to +70°C

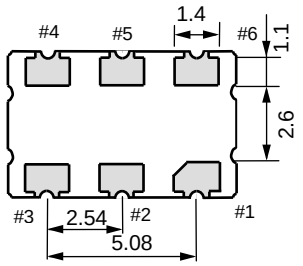
Table 2 Jitter

Item	Symbol	Specifications	Remarks
Jitter *	t_{DJ}	0.2 ps Typ.	Deterministic Jitter
	t_{RJ}	3 ps Typ.	Random Jitter
	t_{RMS}	3 ps Typ.	σ (RMS of total distribution)
	t_{p-p}	25 ps Typ.	Peak to Peak
	t_{acc}	4 ps Typ.	Accumulated Jitter(σ) n=2 to 50000 cycles

* Tested using a DTS-2075 Digital timing system made by WAVECREST with jitter analysis software VISI6. : Differential LV-PECL, LVDS output
* Based on SIA-3100C signal integrity analyzer made from WAVECREST. : HCSL output

External dimensions (Unit:mm)





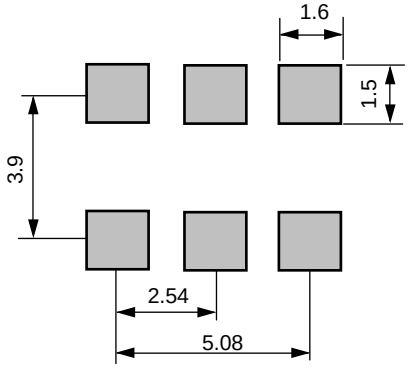
OE pin = HIGH : Specified frequency output.
OE pin = LOW : Output is high impedance

Pin map

Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

#3 is connected to the cover.

Footprint (Recommended) (Unit:mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

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