

DATA SHEET

74F253

Dual 4-bit input multiplexer (3-State)

Product specification

1988 Nov 29

IC15 Data Handbook

Dual 4-input multiplexer (3-State)

74F253

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Common select inputs
- Separate Output Enable Inputs

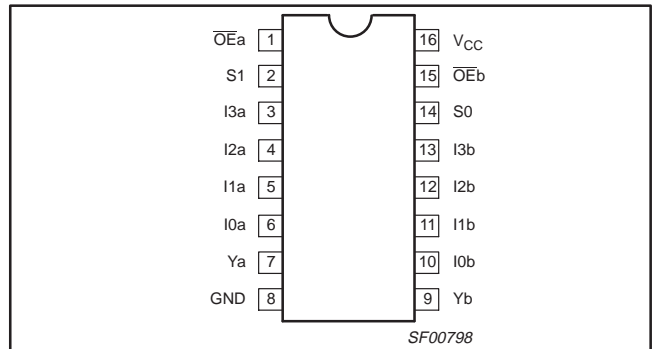
DESCRIPTION

The 74F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S0, S1). When the individual Output Enable (\overline{OE}_a , \overline{OE}_b) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 74F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-State devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE	PKG DWG #
	$V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C \text{ to } +70^\circ C$	
16-pin plastic DIP	N74F253N	SOT38-4
16-pin plastic SO	N74F253D	SOT109-1

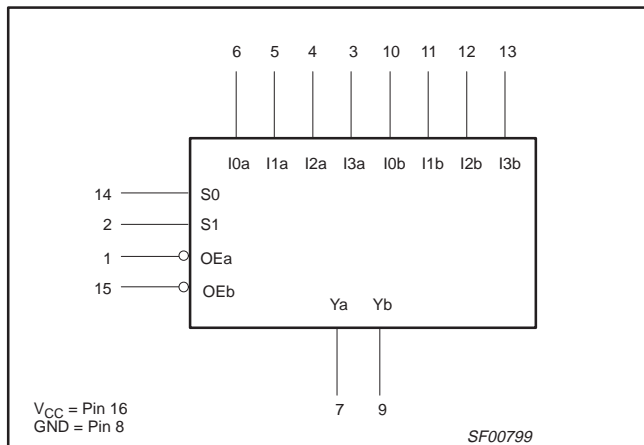
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a–I3a	Port A data inputs	1.0/1.0	20 μ A/0.6mA
I0b–I3b	Port B data inputs	1.0/1.0	20 μ A/0.6mA
S0, S1	Common Select inputs	1.0/1.0	20 μ A/0.6mA
\overline{OE}_a	Port A Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{OE}_b	Port B Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
Ya, Yb	3-State outputs	150/40	3mA/24mA

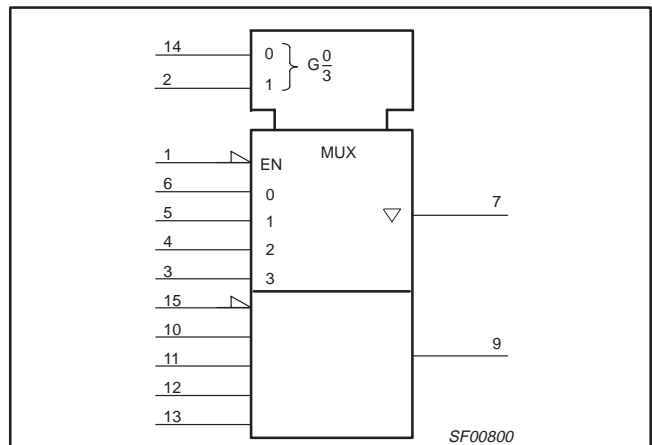
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



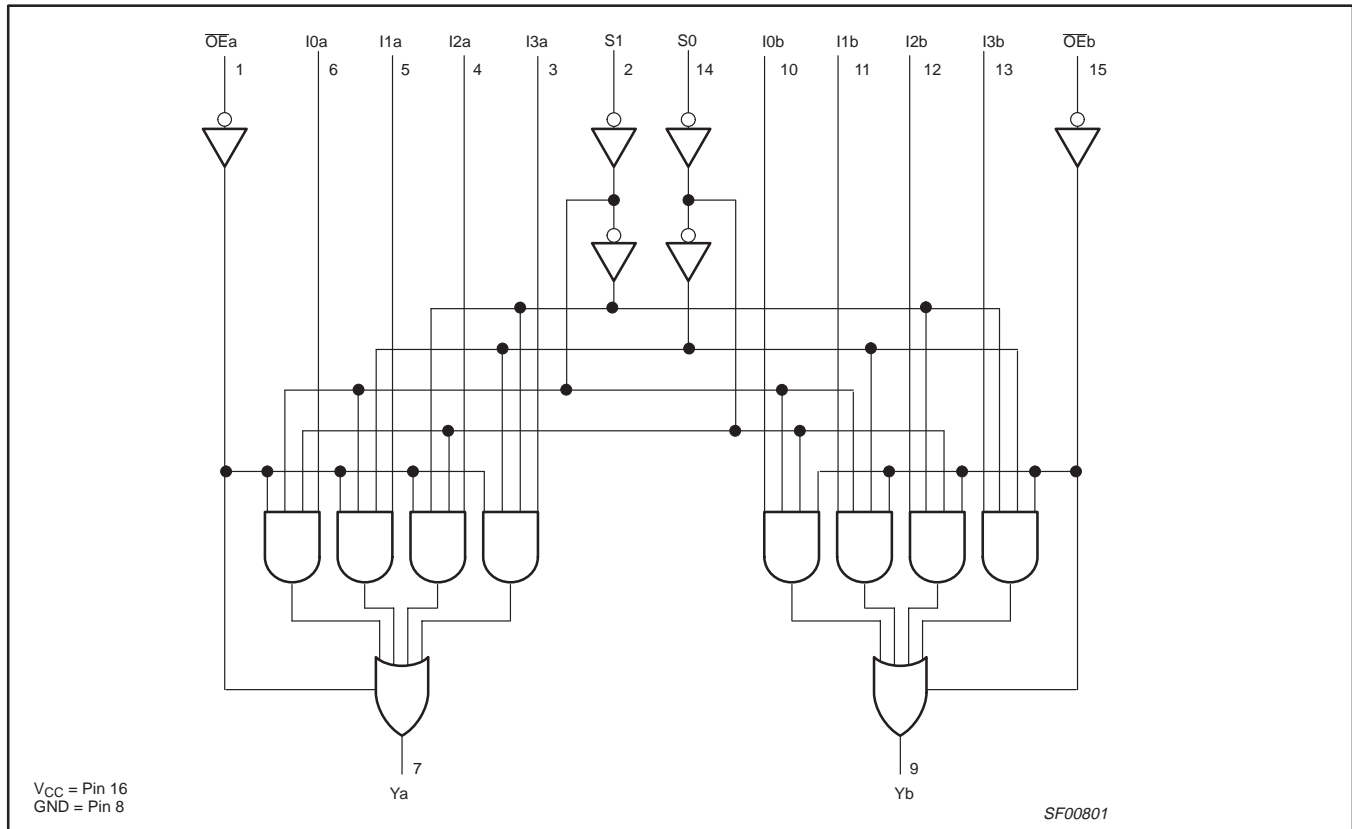
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S0	S1	I0	I1	I2	I3	OE	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ^{NO TAG}		LIMITS			UNIT	
				MIN	TYP NO TAG	MAX		
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.4			V	
			±5%V _{CC}	2.7	3.3		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V	
			±5%V _{CC}		0.35	0.50	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				-0.6	mA	
I _{OZH}	Off-state output current High-level voltage applied	V _{CC} = MAX, V _O = 2.7V				50	μA	
I _{OZL}	Off-state output current Low-level voltage applied	V _{CC} = MAX, V _O = 0.5V				-50	μA	
I _{OS}	Short-circuit output current ^{NO TAG}	V _{CC} = MAX		-60		-150	mA	
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	OE _n =GND, S _n =I _n =4.5V		10	16	mA
		I _{CCL}		OE _n =S _n =I _n =GND		12	23	mA
		I _{CCZ}		OE _n =4.5V, S _n =I _n =GND		14	23	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Dual 4-input multiplexer (3-State)

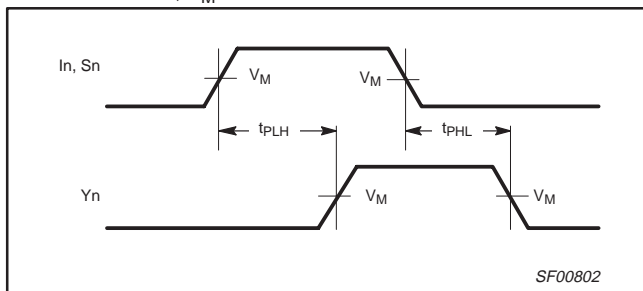
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AC ELECTRICAL CHARACTERISTICS

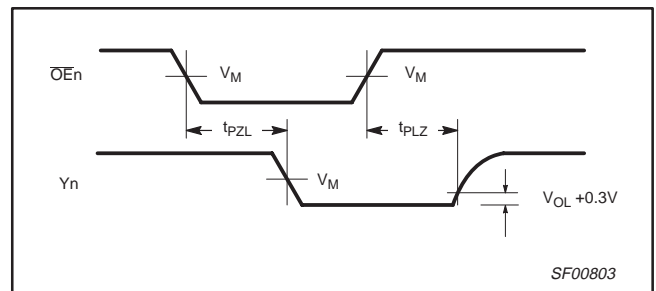
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5V T _{amb} = +25°C C _L = 50pF R _L = 500Ω			V _{CC} = +5V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay In to Y _n	Waveform NO TAG	3.0 3.0	4.5 5.0	7.0 7.0	3.0 3.0	7.5 8.0	ns
t _{PLH} t _{PHL}	Propagation delay S _n to Y _n	Waveform NO TAG	4.5 5.0	7.5 8.5	10.5 11.0	4.5 4.5	11.0 12.0	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.5 6.5	8.0 8.0	3.0 3.0	9.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	3.5 3.0	5.0 5.0	2.0 1.5	6.0 6.0	ns

AC WAVEFORMS

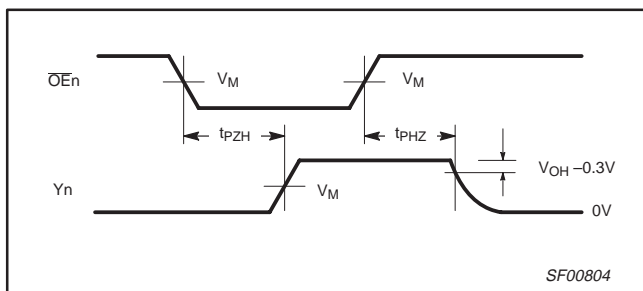
For all waveforms, V_M = 1.5V



Waveform 1. Propagation Delay, Data and Select to Output



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

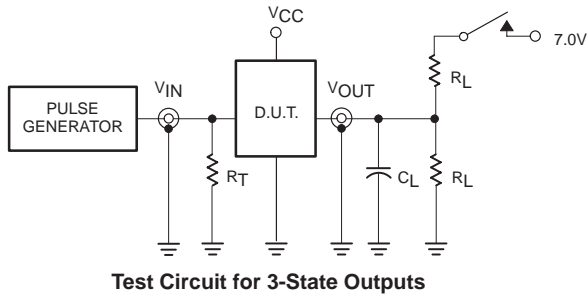


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

Dual 4-input multiplexer (3-State)

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TEST CIRCUIT AND WAVEFORMS



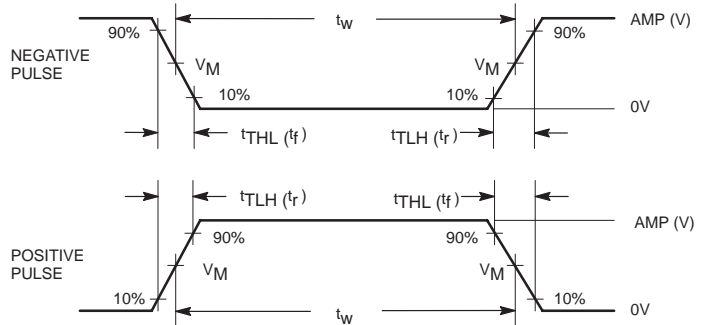
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

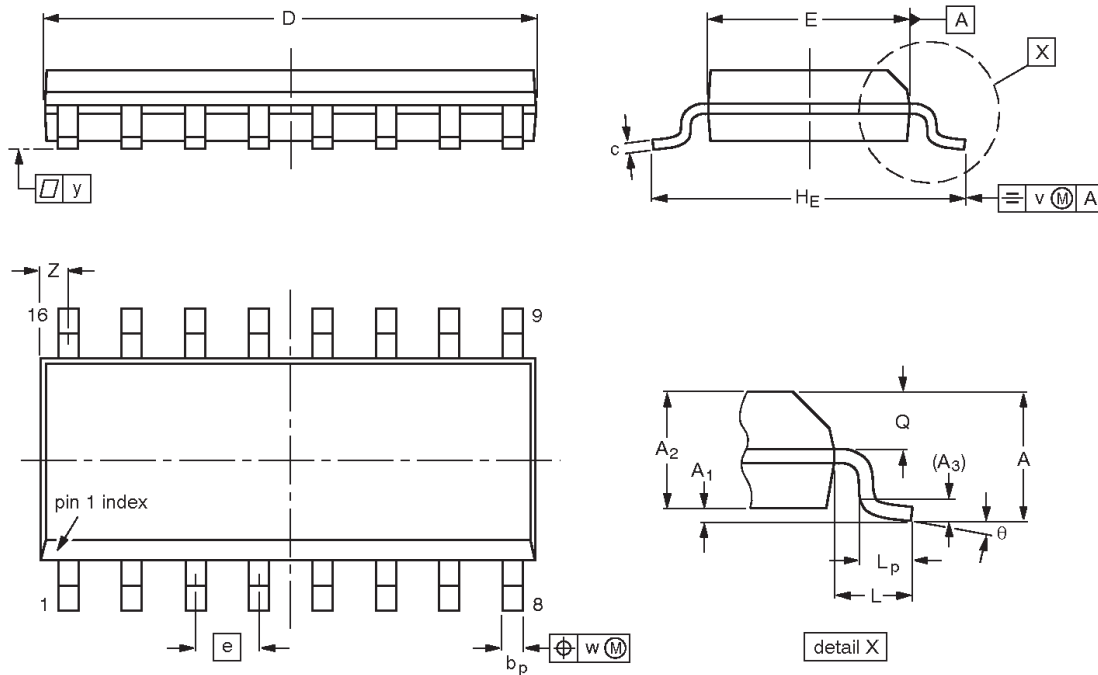
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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