



# BT1308 series D

Triacs logic level

Rev. 01 — 26 February 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Passivated sensitive gate triacs in a SOT54 plastic package

### 1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Gate triggering in four quadrants
- Direct interfacing to low-power gate drive circuits

### 1.3 Applications

- General purpose switching and phase control
- Low-power AC fan speed control

### 1.4 Quick reference data

- $V_{DRM} \leq 400$  V (BT1308-400D)
- $V_{DRM} \leq 600$  V (BT1308-600D)
- $I_{TSM} \leq 9$  A ( $t = 20$  ms)
- $I_{GT} \leq 5$  mA
- $I_{GT} \leq 7$  mA (T2– G+)
- $I_{T(RMS)} \leq 0.8$  A

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 2 (T2)	 SOT54 (TO-92)	 sym051
2	gate (G)		
3	main terminal 1 (T1)		

### 3. Ordering information

**Table 2. Ordering information**

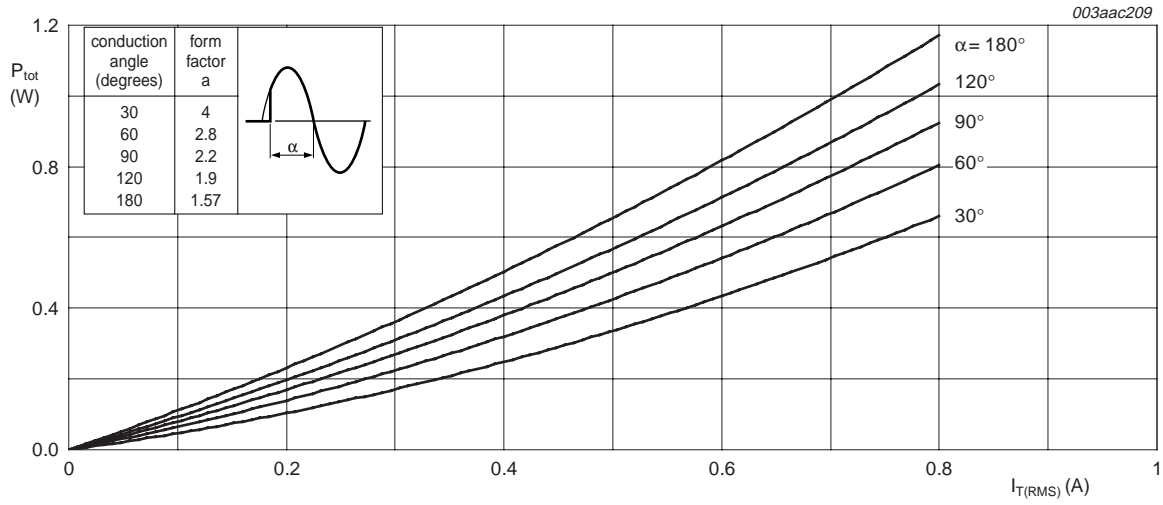
Type number	Package		Version
	Name	Description	
BT1308-400D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT1308-600D			

### 4. Limiting values

**Table 3. Limiting values**

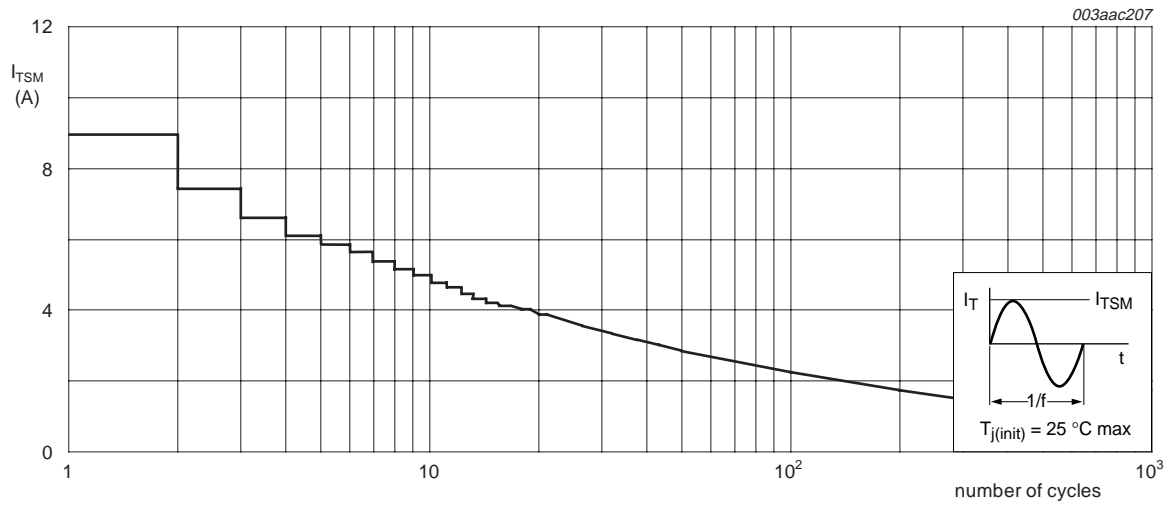
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DRM</sub>	repetitive peak off-state voltage	BT1308-400D	-	400	V
		BT1308-600D	-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 55 °C; see <a href="#">Figure 4</a> and <a href="#">5</a>	-	0.8	A
I <sub>TSM</sub>	non-repetitive peak on-state current	full sine wave; T <sub>j</sub> = 25 °C prior to surge; see <a href="#">Figure 2</a> and <a href="#">3</a>			
		t = 20 ms	-	9	A
		t = 16.7 ms	-	10	A
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms	-	0.32	A <sup>2</sup> s
dI <sub>T</sub> /dt	rate of rise of on-state current	I <sub>TM</sub> = 1 A; I <sub>G</sub> = 20 mA; dI <sub>G</sub> /dt = 0.2 A/μs			
		T2+ G+	-	50	A/μs
		T2+ G-	-	50	A/μs
		T2- G-	-	50	A/μs
		T2- G+	-	10	A/μs
I <sub>GM</sub>	peak gate current		-	1	A
P <sub>GM</sub>	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.1	W
T <sub>stg</sub>	storage temperature		-40	+150	°C
T <sub>j</sub>	junction temperature		-	125	°C



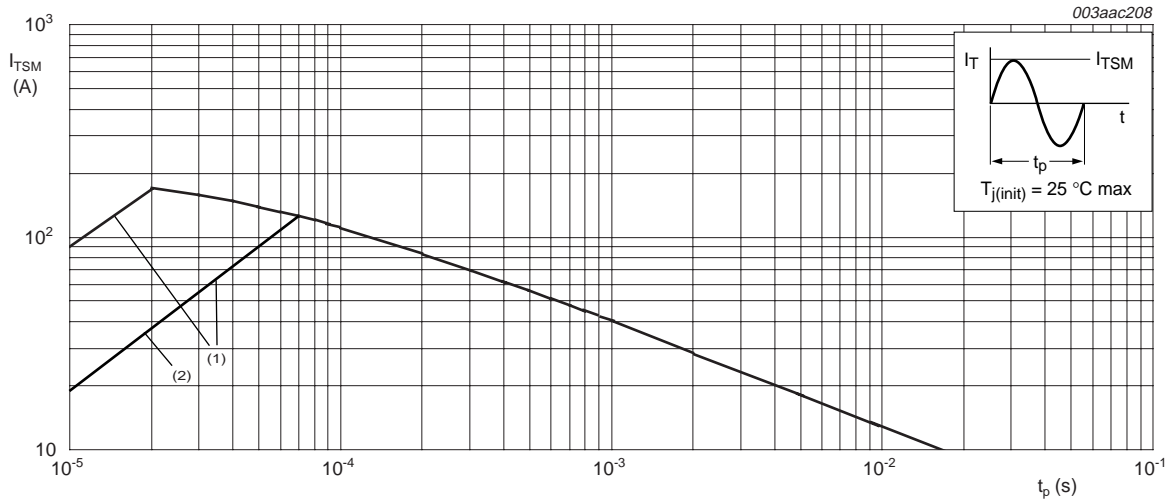
$\alpha$  = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



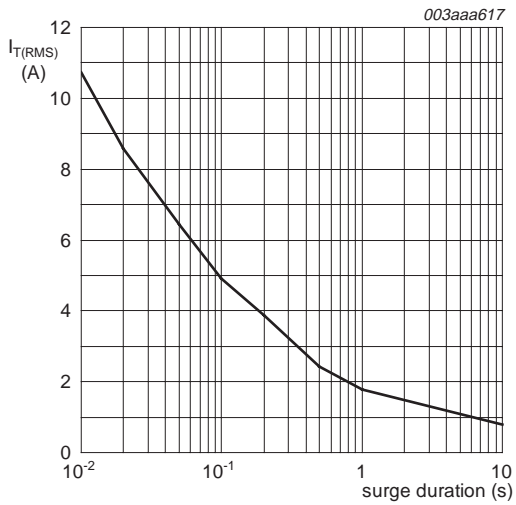
f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



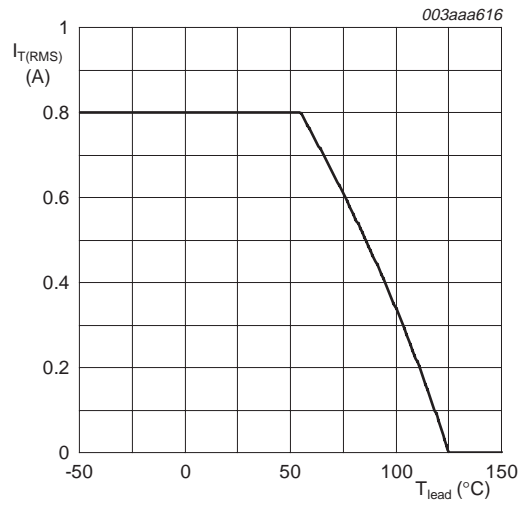
- $t_p \leq 20 \text{ ms}$
- (1)  $di_T/dt$  limit
  - (2) T2- G+ quadrant limit

**Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values**



$f = 50 \text{ Hz}$   
 $T_{\text{lead}} = 55 \text{ }^\circ\text{C}$

**Fig 4. RMS on-state current as a function of surge duration; maximum values**

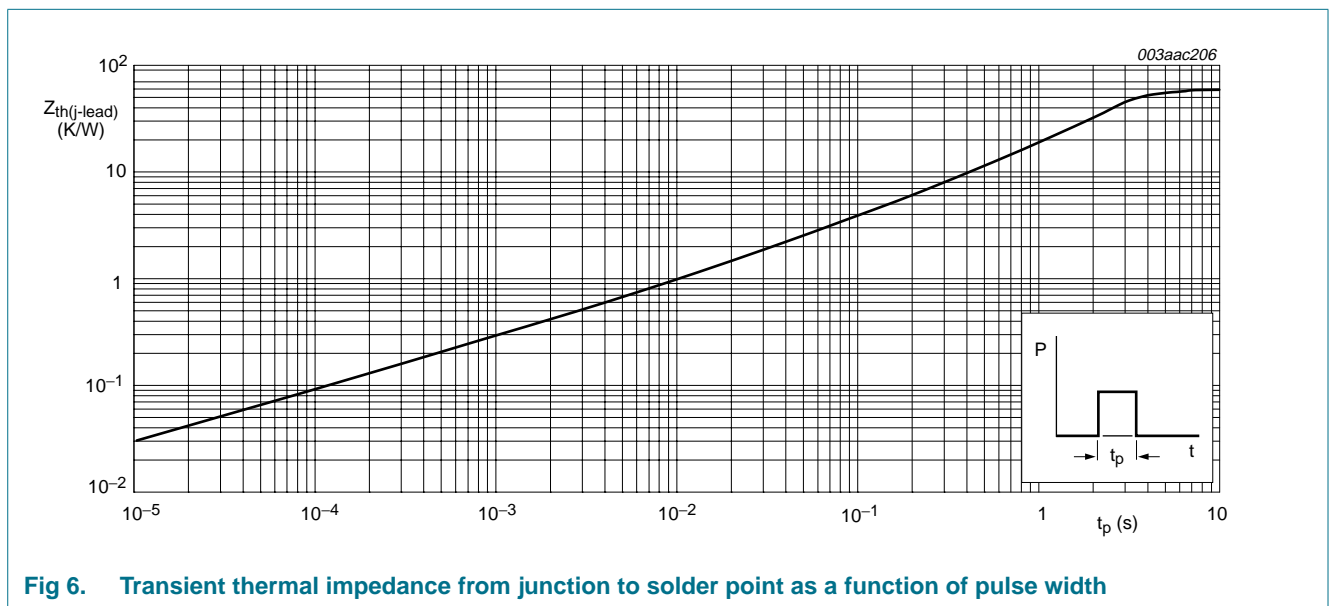


**Fig 5. RMS on-state current as a function of lead temperature; maximum values**

### 5. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length 4 mm; see <a href="#">Figure 6</a>	-	150	-	K/W



## 6. Characteristics

**Table 5. Characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; see <a href="#">Figure 8</a>				
		T2+ G+	-	1	5	mA
		T2+ G-	-	2	5	mA
		T2- G-	-	2	5	mA
		T2- G+	-	4	7	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; see <a href="#">Figure 10</a>				
		T2+ G+	-	1	10	mA
		T2+ G-	-	5	10	mA
		T2- G-	-	1	10	mA
		T2- G+	-	2	10	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; see <a href="#">Figure 11</a>	-	1	10	mA
$V_T$	on-state voltage	$I_T = 0.85\text{ A}$ ; see <a href="#">Figure 9</a>	-	1.35	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; see <a href="#">Figure 7</a>	-	0.9	2	V
		$V_D = V_{DRM}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 110\text{ °C}$	0.1	0.7	-	V
$I_D$	off-state current	$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$ ; $T_j = 110\text{ °C}$ ; exponential waveform; gate open circuit	30	45	-	V/ $\mu$ s
$dV_{com}/dt$	rate of change of commutating voltage	$V_{DM} = V_{DRM(max)}$ ; $T_j = 50\text{ °C}$ ; $I_{TM} = 0.84\text{ A}$ ; $dI_{com}/dt = 0.3\text{ A/ms}$	-	5	-	V/ $\mu$ s
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 1\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 25\text{ mA}$ ; $dI_G/dt = 5\text{ A}/\mu$ s	-	2	-	$\mu$ s

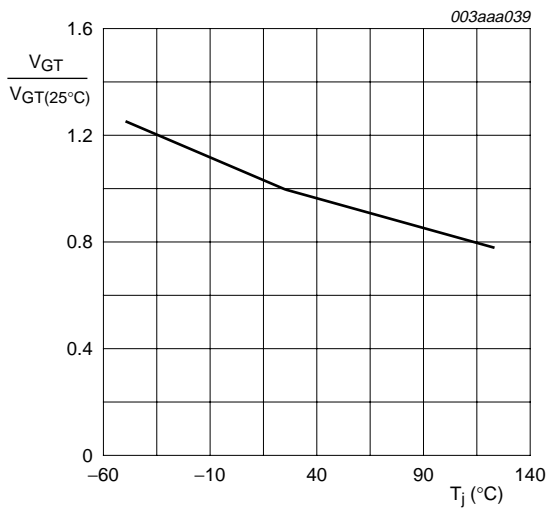
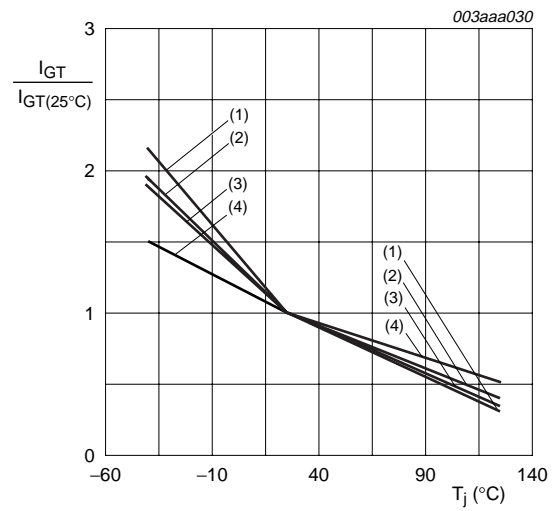
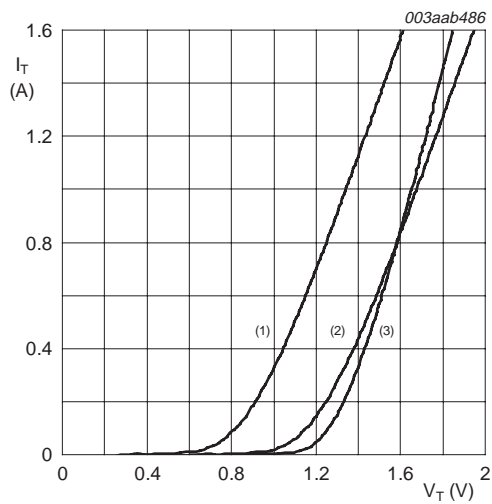


Fig 7. Normalized gate trigger voltage as a function of junction temperature



- (1) T2+ G+
- (2) T2- G+
- (3) T2- G-
- (4) T2+ G-

Fig 8. Normalized gate trigger current as a function of junction temperature



- $V_o = 1.171 \text{ V}$   
 $R_s = 0.5125 \text{ } \Omega$
- (1)  $T_j = 125 \text{ } ^\circ\text{C}$ ; typical values
  - (2)  $T_j = 125 \text{ } ^\circ\text{C}$ ; maximum values
  - (3)  $T_j = 25 \text{ } ^\circ\text{C}$ ; maximum values

Fig 9. On-state current as a function of on-state voltage

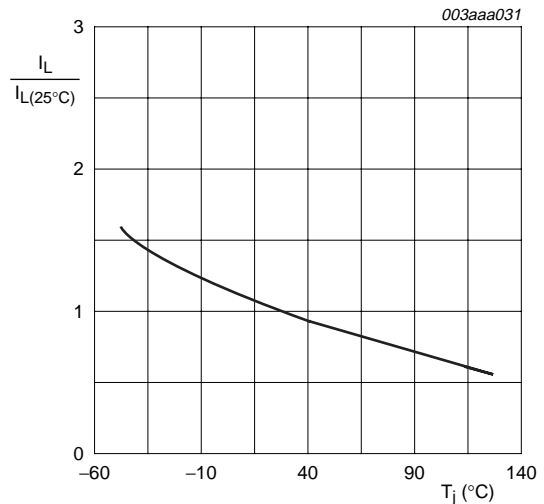


Fig 10. Normalized latching current as a function of junction temperature

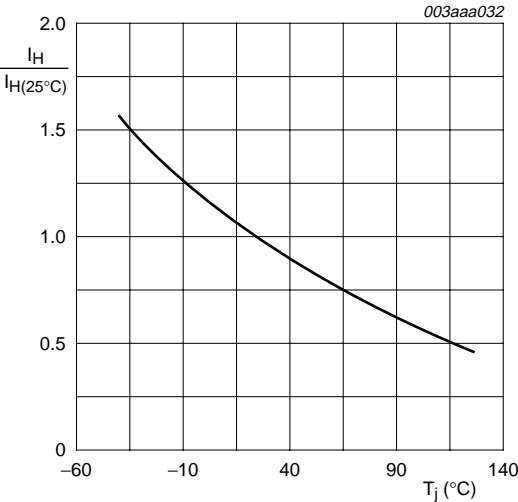


Fig 11. Normalized holding current as a function of junction temperature



7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

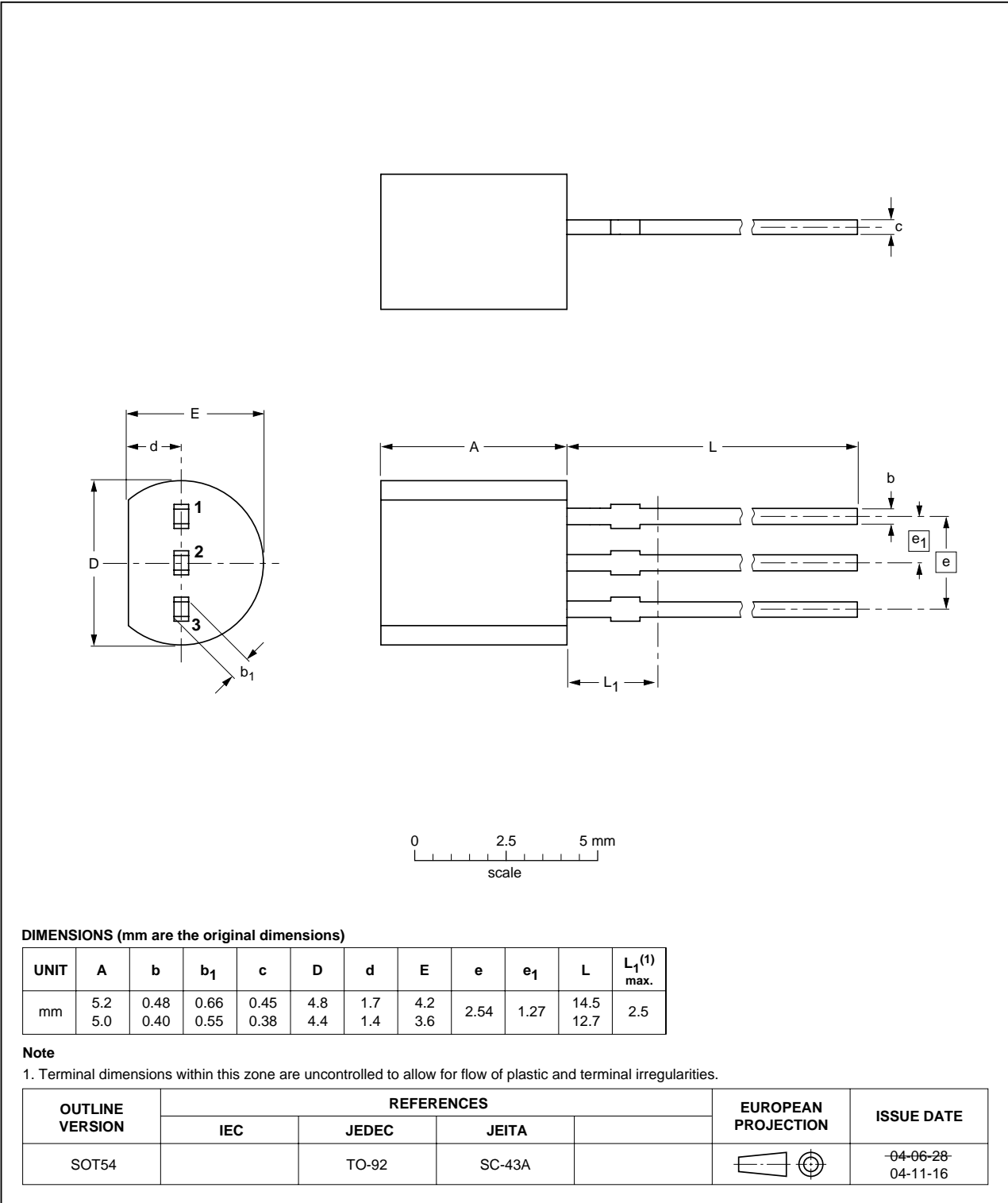


Fig 12. Package outline SOT54 (TO-92)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT1308_SER_D_1	20080226	Product data sheet	-	-

## 9. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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