

BUK6610-75C

N-channel TrenchMOS FET

Rev. 02 — 14 October 2010

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating
- Suitable for intermediate level gate drive sources

1.3 Applications

- 12 V Automotive systems
- Start-Stop micro-hybrid applications
- Electric and electro-hydraulic power steering
- Transmission control
- EngineMotors, lamps and solenoid control management
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 75 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see Figure 1 | - | - | 78 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | - | 158 | W |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 11 | - | 8.6 | 10 | mΩ |

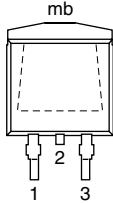
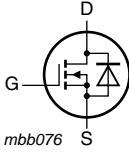


Table 1. Quick reference data ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|-----|-----|-----|------|
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 78\text{ A}$; $V_{sup} \leq 75\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped | - | - | 121 | mJ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 25\text{ A}$; $V_{DS} = 60\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 13 ; see Figure 14 | - | 30 | - | nC |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|--|
| 1 | G | gate |  |  |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|-------------|---------|--|---------|
| | Name | Description | |
| BUK6610-75C | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------------------------|--|--|-----------|-----|------|---|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 75 | V | |
| V_{GS} | gate-source voltage | DC | [1] | -16 | 16 | V |
| | | Pulsed | [2] | -20 | 20 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 | - | 78 | A | |
| | | $T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 [3] | - | 55 | A | |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see Figure 3 | - | 311 | A | |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | 158 | W | |
| T_{stg} | storage temperature | | -55 | 175 | °C | |
| T_j | junction temperature | | -55 | 175 | °C | |
| Source-drain diode | | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 78 | A | |
| I_{SM} | peak source current | $t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$ | - | 311 | A | |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 78\text{ A}; V_{sup} \leq 75\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped | - | 121 | mJ | |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | | [4][5][6] | - | J | |

[1] -16V accumulated duration not to exceed 168 hrs.

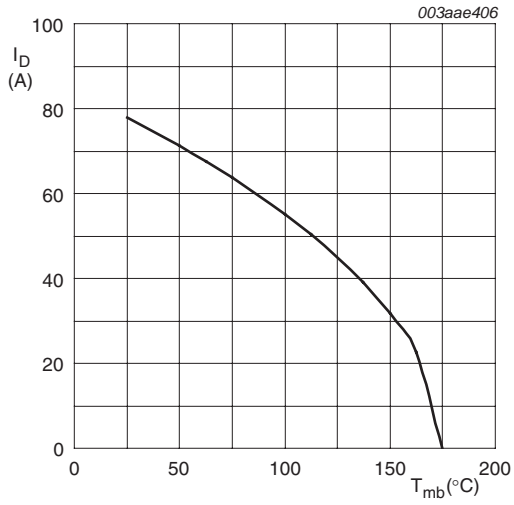
[2] Accumulated pulse duration not to exceed 5mins.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

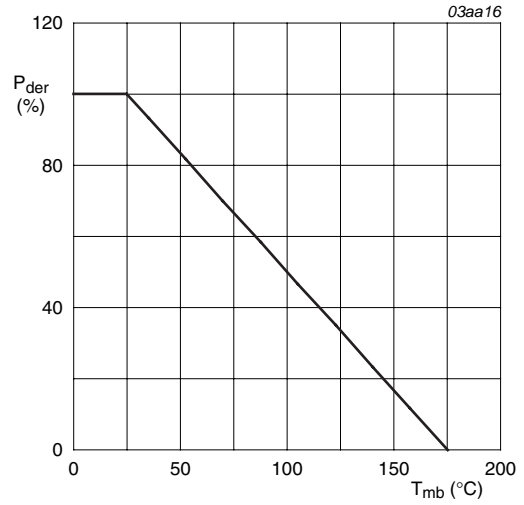
[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.



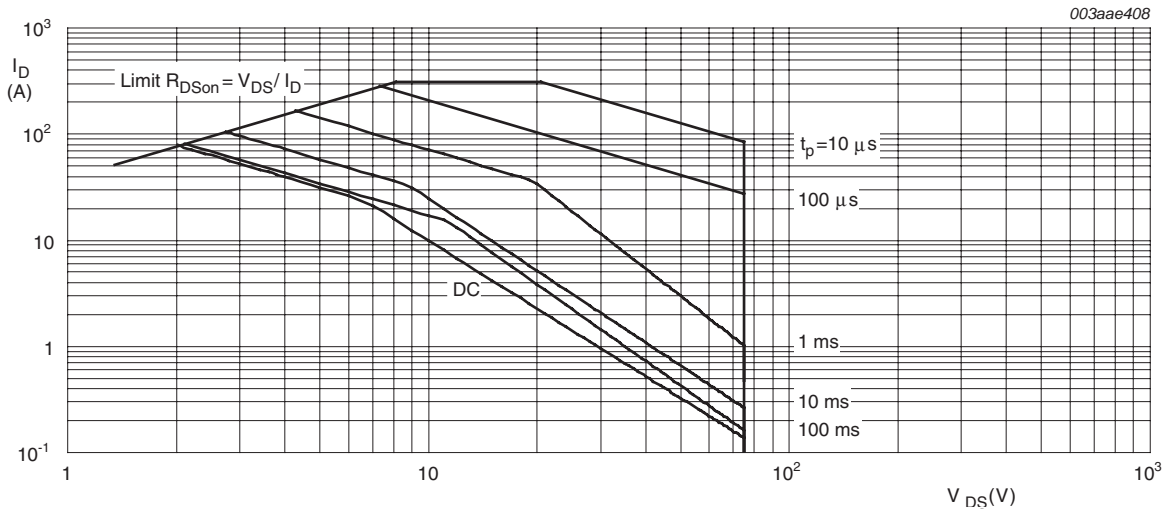
$$V_{GS} \geq 10V$$

Fig. 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is a single pulse}$$

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 0.95 | K/W |

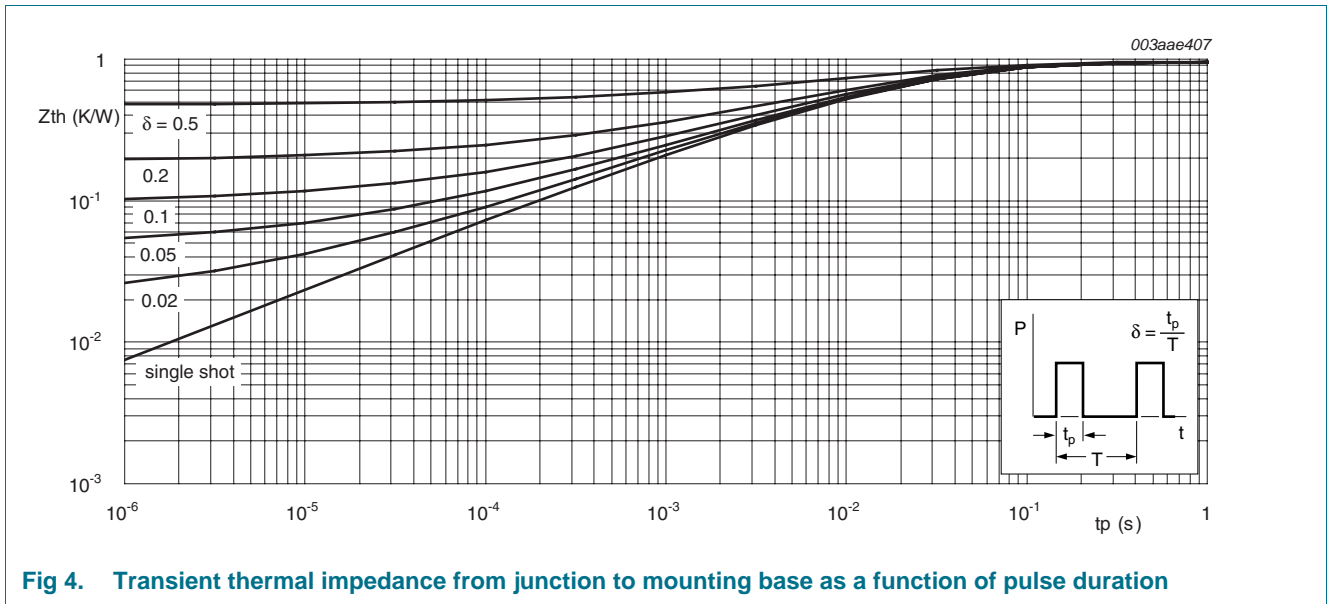


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

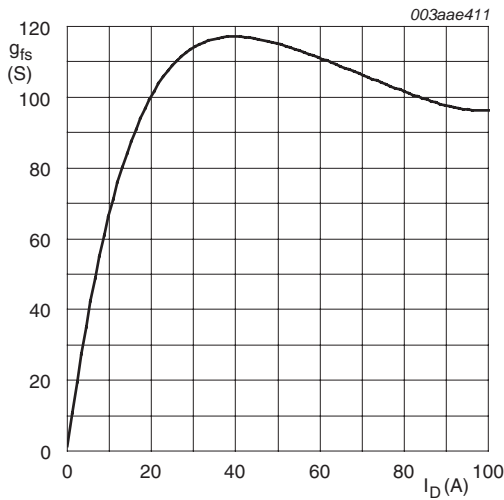
6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 75 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 68 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10 | 1.8 | 2.3 | 2.8 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 9 | - | - | 3.3 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 9 | 0.8 | - | - | V |
| I_{DSS} | drain leakage current | $V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| | | $V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 1 | μA |
| I_{GSS} | gate leakage current | $V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 5 | 100 | nA |
| | | $V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 5 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 11 | - | 8.6 | 10 | m Ω |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 11 | - | 10.4 | 14.2 | m Ω |
| | | $V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 11 | - | 9.8 | 12.5 | m Ω |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$; see Figure 12 ; see Figure 11 | - | - | 26 | m Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 5 \text{ V}$; see Figure 13 ; see Figure 14 | - | 52 | - | nC |
| | | $I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 14 ; see Figure 13 | - | 81 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 13 ; see Figure 14 | - | 11 | - | nC |
| Q_{GD} | gate-drain charge | | - | 30 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 16 | - | 3938 | 5251 | pF |
| C_{oss} | output capacitance | | - | 310 | 372 | pF |
| C_{rSS} | reverse transfer capacitance | | - | 206 | 282 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 55 \text{ V}; R_L = 2.2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$ | - | 18 | - | ns |
| t_r | rise time | | - | 40 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 165 | - | ns |
| t_f | fall time | | - | 80 | - | ns |
| L_D | internal drain inductance | from upper edge of drain mounting base to centre of die ; $T_j = 25 \text{ }^\circ C$ | - | 3.5 | - | nH |
| L_S | internal source inductance | from source lead to source bond pad ; $T_j = 25 \text{ }^\circ C$ | - | 7.5 | - | nH |

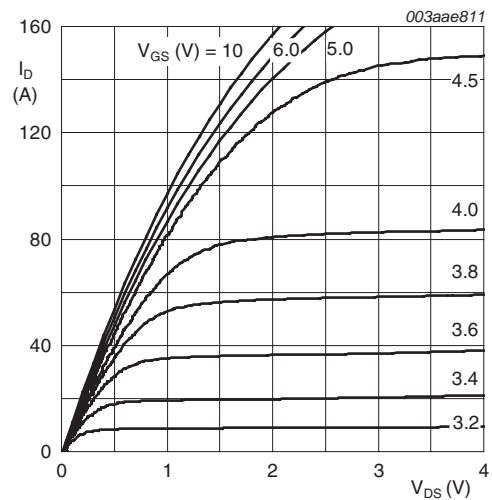
Table 6. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|---|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 15 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; | - | 50.5 | - | ns |
| Q_r | recovered charge | $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$ | - | 105 | - | nC |



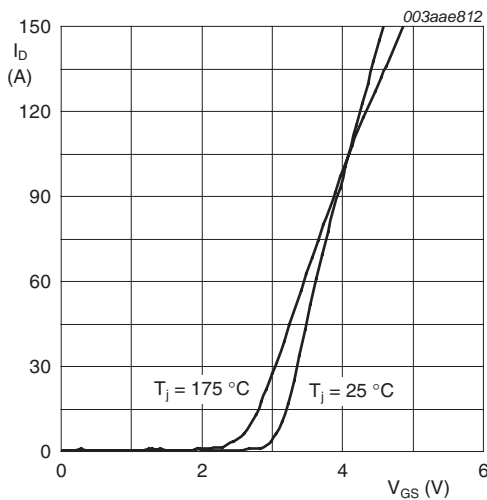
$T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = 25\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



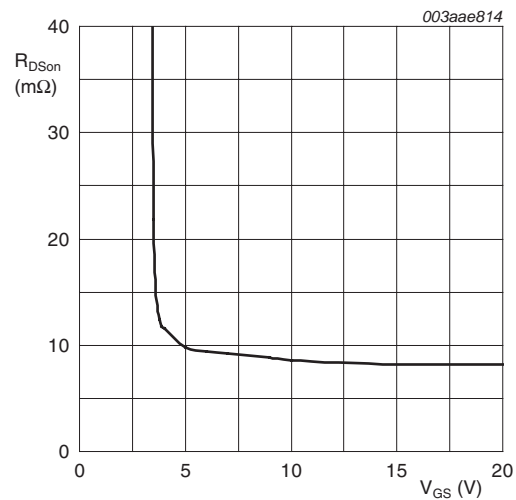
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



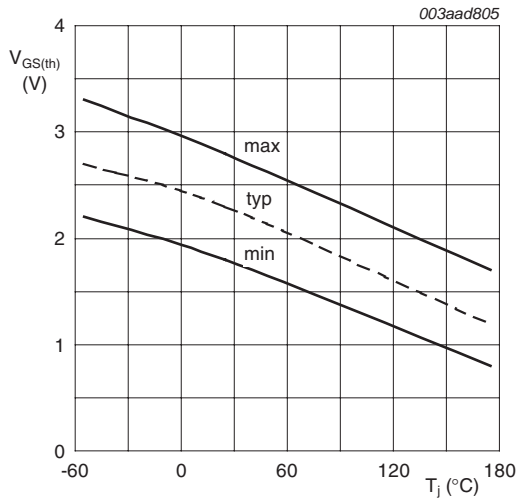
$V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



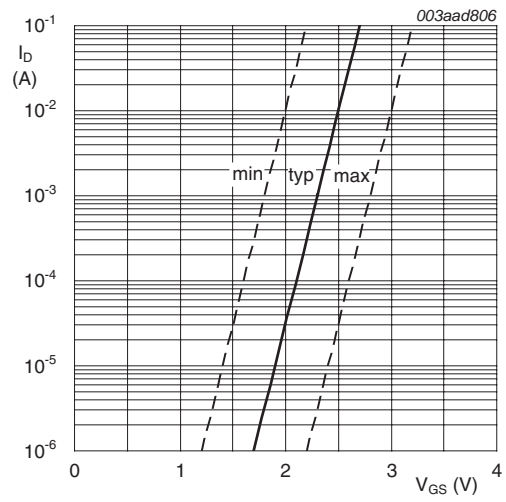
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



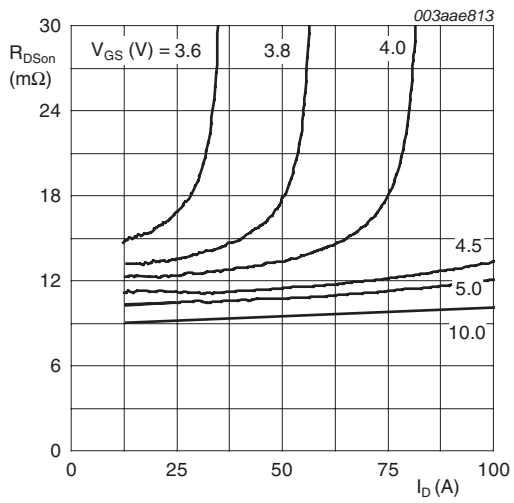
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



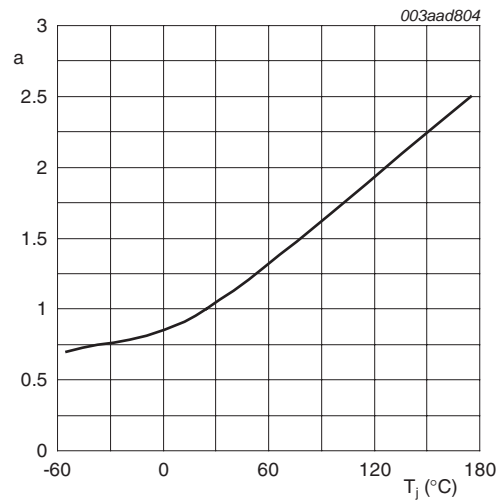
$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



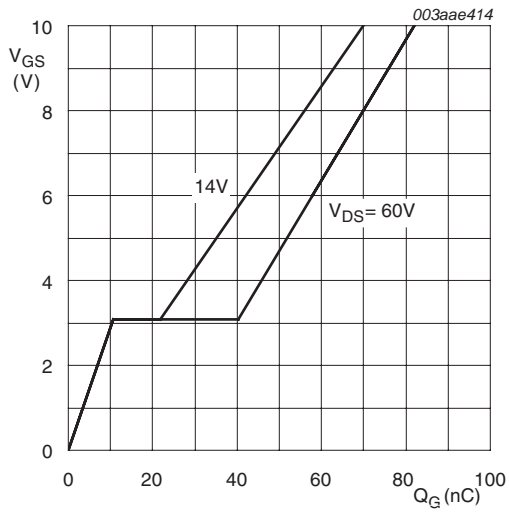
$$T_j = 25^\circ\text{C}$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C; I_D = 25A$

Fig 13. Gate-source voltage as a function of gate charge; typical values

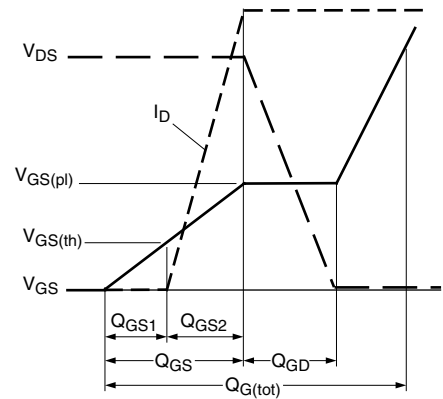
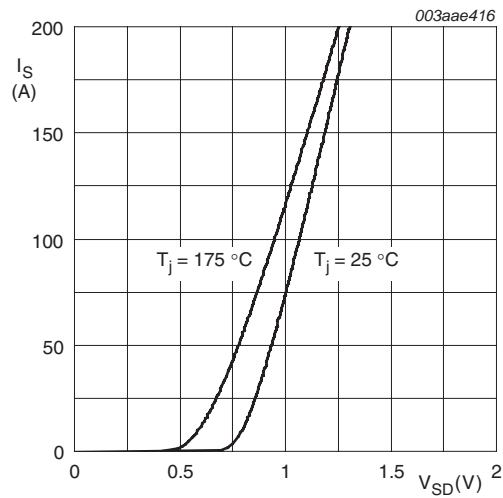


Fig 14. Gate charge waveform definitions



$V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

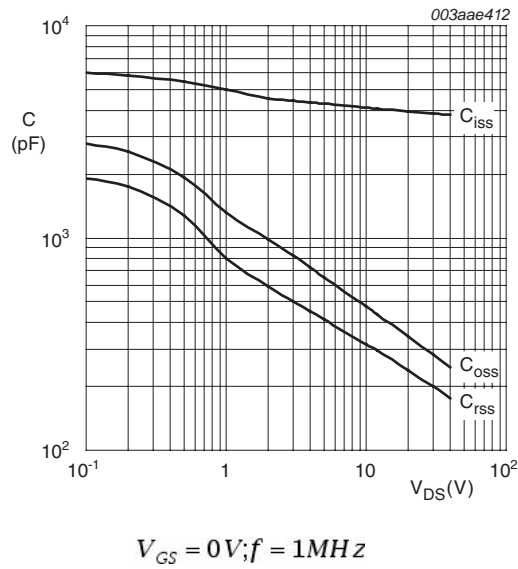


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

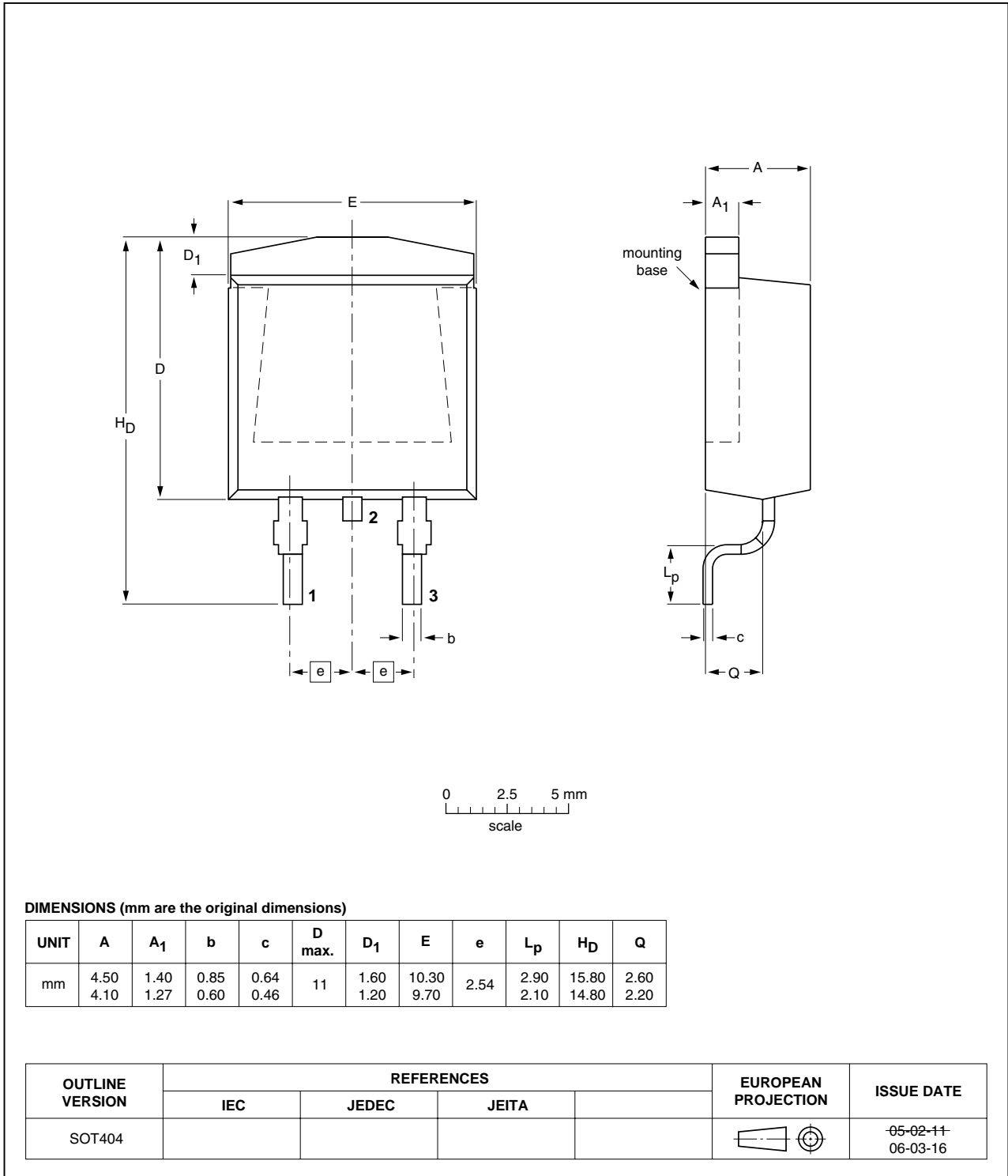


Fig 17. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|---|----------------------|---------------|-----------------|
| BUK6610-75C v.2 | 20101014 | Product data sheet | - | BUK6610-75C v.1 |
| Modifications: | <ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content. | | | |
| BUK6610-75C v.1 | 20090323 | Objective data sheet | - | - |

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9.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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