

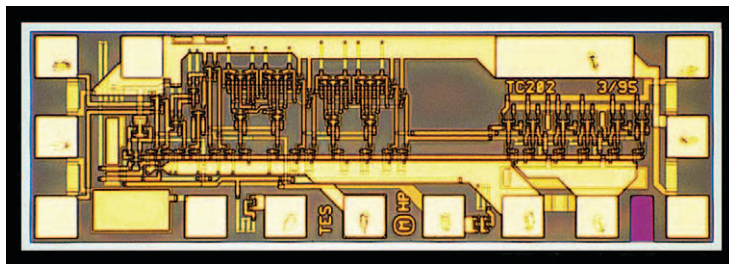
# Keysight Technologies

HMMC-3004 DC-16 GHz

GaAs HBT MMIC Divide-by-4 Prescaler

1GC1-8002

## Data Sheet



## Features

- Wide Frequency Range:  
0.2 to 16 GHz
- High Input Power Sensitivity:  
On-chip pre- and post-amps  
-20 to +10 dBm (1-10 GHz)  
-15 to +10 dBm (10-12 GHz)  
-10 to +5 dBm (12-15 GHz)
- Dual-mode  $P_{out}$ : (chip form)  
+6.0 dBm (0.99  $V_{p-p}$ ) @ 80 mA  
0 dBm (0.5  $V_{p-p}$ ) @ 60 mA
- Low Phase Noise:  
-153 dBc/Hz @ 100 kHz Offset
- (+) or (-) Single Supply Bias operation
- Wide bias supply range: 4.5 to 6.5 volt operating range
- Differential I/O with on-chip 50  $\Omega$  matching

## Description

The Keysight Technologies, Inc. HMMC-3004 GaAs HBT MMIC Prescaler offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers an input disable contact pad to eliminate any self-oscillation condition.

## Absolute Maximum Ratings<sup>1</sup>

(@  $T_A = 25^\circ\text{C}$ , unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
$V_{CC}$	Bias supply voltage		+7	volts
$V_{EE}$	Bias supply voltage	-7		volts
$V_{CC}-V_{EE}$	Bias supply delta	0	+7	volts
$V_{Disable}$	Pre-amp disable voltage	$V_{EE}$	$V_{CC}$	volts
$V_{Logic}$	Logic threshold voltage	$V_{CC} - 1.5$	$V_{CC} - 1.2$	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
$V_{RFIn}$	DC input voltage (@ $RF_{in}$ or $RF_{in}$ ports)		$V_{CC} \pm 0.5$	volts
$T_{BS}^2$	Backside Ambient Temperature	-40	+85	$^\circ\text{C}$
$T_{st}$	Storage Temperature	-65	+165	$^\circ\text{C}$
$T_{max}$	Max. Assembly Temperature (60 s max.)		310	$^\circ\text{C}$

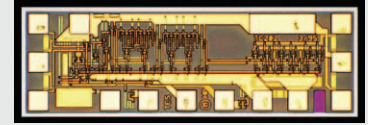
1. Operation in excess of any parameter limit (except  $T_{BS}$ ) may cause permanent damage to the device.
2.  $MTTF > 1 \times 10^6$  hours @  $T_{BS} \leq 85^\circ\text{C}$ . Operation in excess of maximum operating temperature ( $T_{BS}$ ) will degrade MTTF.

## DC Specifications/Physical Properties<sup>1</sup>

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 5.0$  volts, unless otherwise listed)

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
$V_{CC} - V_{EE}$	Operating bias supply difference <sup>1</sup>	4.5	5.0	6.5	Volts
$ I_{CC} $ or $ I_{EE} $	Bias supply current ( <b>High</b> output power configuration <sup>2</sup> : $V_{PwrSel}=V_{EE}$ )	68	80	92	mA
	Bias supply current ( <b>Low</b> output power configuration: $V_{PwrSel}=\text{open}$ )	51	60	69	mA
$V_{RFIn(q)}$ , $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		$V_{CC}$		Volts
$V_{Logic}$	Nominal ECL Logic Level ( $V_{Logic}$ contact self-bias voltage, generated on-chip)	$V_{CC} - 1.45$	$V_{CC} - 1.35$	$V_{CC} - 1.25$	Volts

1. Prescaler will operate over full specified supply voltage range,  $V_{CC}$  or  $V_{EE}$  not to exceed limits specified in Absolute Maximum Ratings section.
2. High output power configuration:  $P_{out} = +6.0$  dBm ( $V_{out} = 0.99 V_{p-p}$ ). Low output power configuration:  $P_{out} = 0$  dBm ( $V_{out} = 0.5 V_{p-p}$ ).



Chip size:

1330 x 440  $\mu\text{m}$  (52.4 x 17.3 mils)

Chip size tolerance:

$\pm 10 \mu\text{m}$  ( $\pm 0.4$  mils)

Chip thickness:

$127 \pm 15 \mu\text{m}$  ( $5 \pm 0.6$  mils)

Pad dimensions:

70 x 70  $\mu\text{m}$  (2.8 x 2.8 mils)

## RF Specifications

( $T_A = 25\text{ }^\circ\text{C}$ ,  $Z_0 = 50\text{ }\Omega$ ,  $V_{CC} - V_{EE} = 5.0\text{ volts}$ )

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation <sup>1</sup> ( $P_{in} = -10\text{ dBm}$ )		0.2	0.5	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency <sup>2</sup>		3.4		GHz
	@ dc (Square-wave input)	-15	$\geq 25$	+10	dBm
	@ $f_{in} = 500\text{ MHz}$ (Sine-wave input)	-15	$\geq 20$	+10	dBm
$P_{in}$	$f_{in} = 1\text{ to }10\text{ GHz}$	-15	$\geq 25$	+10	dBm
	$f_{in} = 10\text{ to }12\text{ GHz}$	-10	$\geq 15$	+10	dBm
	$f_{in} = 12\text{ to }15\text{ GHz}$	-4	$\geq 10$	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ $f_{in} < 12\text{ GHz}$ )		15		dB
$S_{12}$	Small-Signal Reverse Isolation (@ $f_{in} < 12\text{ GHz}$ )		30		dB
$\phi_N$	SSB Phase Noise (@ $P_{in} = 0\text{ dBm}$ , 100 kHz offset from a $f_{out} = 1.2\text{ GHz}$ carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing ( $f_{in} = 10\text{ GHz}$ , $P_{in} = -10\text{ dBm}$ )		1		ps
$T_r$ or $T_f$	Output transition time (10% to 90% rise/fall time)		70		ps
<b>High Output Power Operating Mode<sup>3</sup></b>					
$P_{out}$	@ $f_{out} < 1\text{ GHz}$	4	6		dBm
	@ $f_{out} = 2.5\text{ GHz}$	4	6		dBm
	@ $f_{out} = 3.5\text{ GHz}$	3	5		dBm
$ V_{out(p-p)} $	@ $f_{out} < 1\text{ GHz}$	0.79	0.99		Volts
	@ $f_{out} = 2.5\text{ GHz}$	0.79	0.99		Volts
	@ $f_{out} = 3.5\text{ GHz}$	0.7	0.88		Volts
$P_{Spitback}$	$f_{out}$ power level appearing at $RF_{in}$ or $\overline{RF}_{in}$ (@ $f_{in} = 12\text{ GHz}$ , unused $RF_{out}$ or $\overline{RF}_{out}$ unterminated)		-48		dBm
	$f_{out}$ power level appearing at $RF_{in}$ or $\overline{RF}_{in}$ (@ $f_{in} = 12\text{ GHz}$ , both $RF_{out}$ and $\overline{RF}_{out}$ terminated)		-68		dBm
$P_{feedthru}$	Power level of $f_{in}$ appearing at $RF_{out}$ or $\overline{RF}_{out}$ (@ $f_{in} = 12\text{ GHz}$ , $P_{in} = 0\text{ dBm}$ , referred to $P_{in}(f_{in})$ )		-30		dBc
$H_2$	Second harmonic distortion output level (@ $f_{out} = 3.0\text{ GHz}$ , referred to $P_{out}(f_{out})$ )		-25		dBc
<b>Low Output Power Operating Mode<sup>4</sup></b>					
$P_{out}$	@ $f_{out} < 1\text{ GHz}$	-2	0		dBm
	@ $f_{out} = 2.5\text{ GHz}$	-2	0		dBm
	@ $f_{out} = 3.5\text{ GHz}$	-3.0	-1.0		dBm
$ V_{out(p-p)} $	@ $f_{out} < 1\text{ GHz}$	0.39	0.5		Volts
	@ $f_{out} = 2.5\text{ GHz}$	0.39	0.5		Volts
	@ $f_{out} = 3.5\text{ GHz}$	0.35	0.44		Volts
$P_{Spitback}$	$f_{out}$ power level appearing at $RF_{in}$ or $\overline{RF}_{in}$ (@ $f_{in} = 12\text{ GHz}$ , unused $RF_{out}$ or $\overline{RF}_{out}$ unterminated)		-57		dBm
	$f_{out}$ power level appearing at $RF_{in}$ or $\overline{RF}_{in}$ (@ $f_{in} = 12\text{ GHz}$ , both $RF_{out}$ and $\overline{RF}_{out}$ terminated)		-77		dBm
$P_{feedthru}$	Power level of $f_{in}$ appearing at $RF_{out}$ or $\overline{RF}_{out}$ (@ $f_{in} = 12\text{ GHz}$ , $P_{in} = 0\text{ dBm}$ , referred to $P_{in}(f_{in})$ )		-30		dBc
$H_2$	Second harmonic distortion output level (@ $f_{out} = 3.0\text{ GHz}$ , referred to $P_{out}(f_{out})$ )		-30		dBc

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.

2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ( $V_{Disable}$ ) feature, or the Differential Input de-biasing technique.

3.  $V_{PwrSel} = V_{EE}$

4.  $V_{PwrSel} = \text{Open circuit}$

## Applications

The HMMC-3004 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broadband frequency translation is required.

## Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is “slew-rate” limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not dc connected to any dc bias point on the device.

For positive supply operation  $V_{CC}$  is nominally biased at any voltage in the +4.5 to +6.5 volt range with  $V_{EE}$  (or  $V_{EE}$  &  $V_{PwrSel}$ ) grounded. For negative bias operation  $V_{CC}$  is typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to  $V_{EE}$  (or  $V_{EE}$  &  $V_{PwrSel}$ ).

Several features are designed into this prescaler:

### 1. Dual-output power feature

Bonding both  $V_{EE}$  and  $V_{PwrSel}$  pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm [ $0.5 V_{p-p}$ ] at the RF output port while drawing ~40 mA supply current. Eliminating the  $V_{PwrSel}$  connection results in reduced output -6.0 dBm [ $0.25 V_{p-p}$ ] but at a reduced current draw of ~30 mA resulting in less overall power dissipation.

(NOTE:  $V_{EE}$  must ALWAYS be bonded and  $V_{PwrSel}$  must NEVER be biased to any potential other than  $V_{EE}$  or opencircuited.)

### 2. VLogic ECL contact pad

Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage ( $V_{CC} - 1.35$  V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than  $V_{CC}$ ) to force the pre-scaler to operate at a system generated logic threshold voltage.

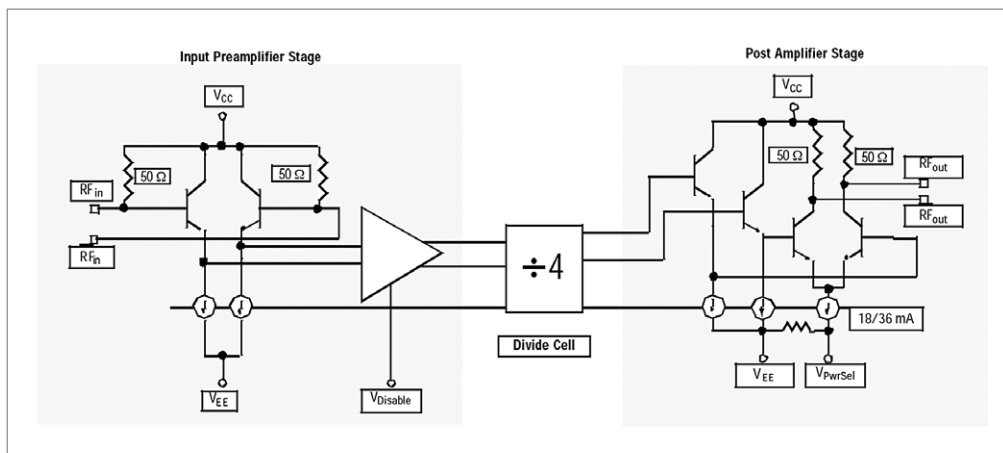


Figure 1. Simplified schematic diagram

### 3. Input disable feature

If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain “ideal” conditions where the input is well matched at the right input frequency, the device may “self-oscillate,” especially under small signal input powers or with only noise present at the input. This “self-oscillation” will produce an undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than  $V_{CC} - 1.35\text{ V}$ ), the input preamplifier stage is locked into either logic “high” or logic “low” preventing frequency division and any self-oscillation frequency which may be present.

### 4. Input dc offset

Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV dc offset voltage between the  $RF_{in}$  and  $RF_{in}$  ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 k $\Omega$  resistor between the unused RF input to a contact point at the  $V_{EE}$  potential will result in an offset of  $\sim 25\text{ mV}$  between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

## Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are dc connected on-chip to the  $V_{CC}$  contact through on-chip 50  $\Omega$  resistors. Under any bias conditions where  $V_{CC}$  is not dc grounded, the RF ports should be ac coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where  $V_{CC}$  is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be “floated” and bias applied as the difference between  $V_{CC}$  and  $V_{EE}$ .

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50  $\Omega$  matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved “Spitback” performance ( $\sim 20\text{ dB}$ ) and input sensitivity can be achieved by terminating the unused  $RF_{out}$  port to  $V_{CC}$  through 50  $\Omega$  (positive supply) or to ground via a 50  $\Omega$  termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

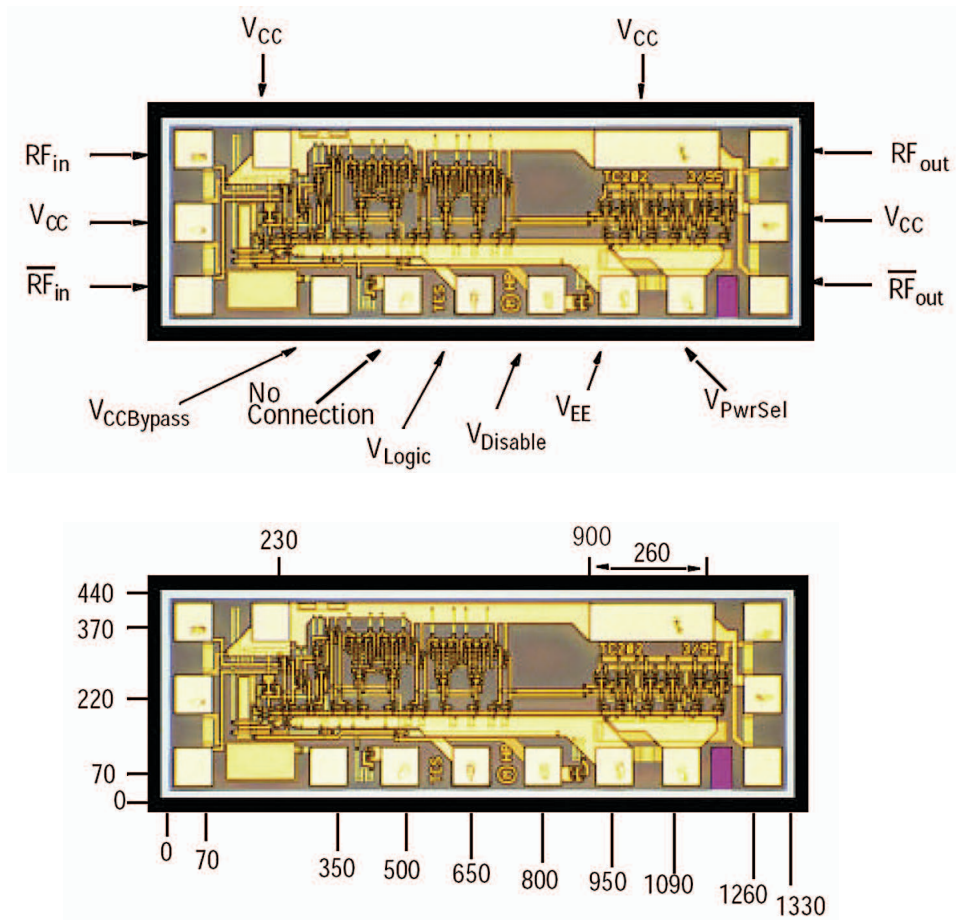
MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

## Optional dc Operating Values/Logic Levels

( $T_A = 25\text{ }^\circ\text{C}$ )

Function	Symbol	Conditions	Min (volts/mA)	Typ (volts/mA)	Max (volts/mA)
Logic Threshold <sup>1</sup>	$V_{Logic}$		$V_{CC}-1.5$	$V_{CC}-1.35$	$V_{CC}-1.2$
Input Disable	$V_{Disable(High)}$ [Disable]		$V_{Logic} + 0.25$	$V_{Logic}$	$V_{CC}$
Input Disable	$V_{Disable(Low)}$ [Enable]		$V_{EE}$	$V_{Logic}$	$V_{Logic} - 0.25$
Input Disable	$I_{Disable}$	$V_D > V_{EE}+3$	$V_{Disable} - V_{EE} - 3)/500$	$V_{Disable} - V_{EE} - 3)/500$	$V_{Disable} - V_{EE} - 3)/500$
Input Disable	$I_{Disable}$	$V_D < V_{EE}+3$	0	0	0

1. Acceptable voltage range when applied from external source.

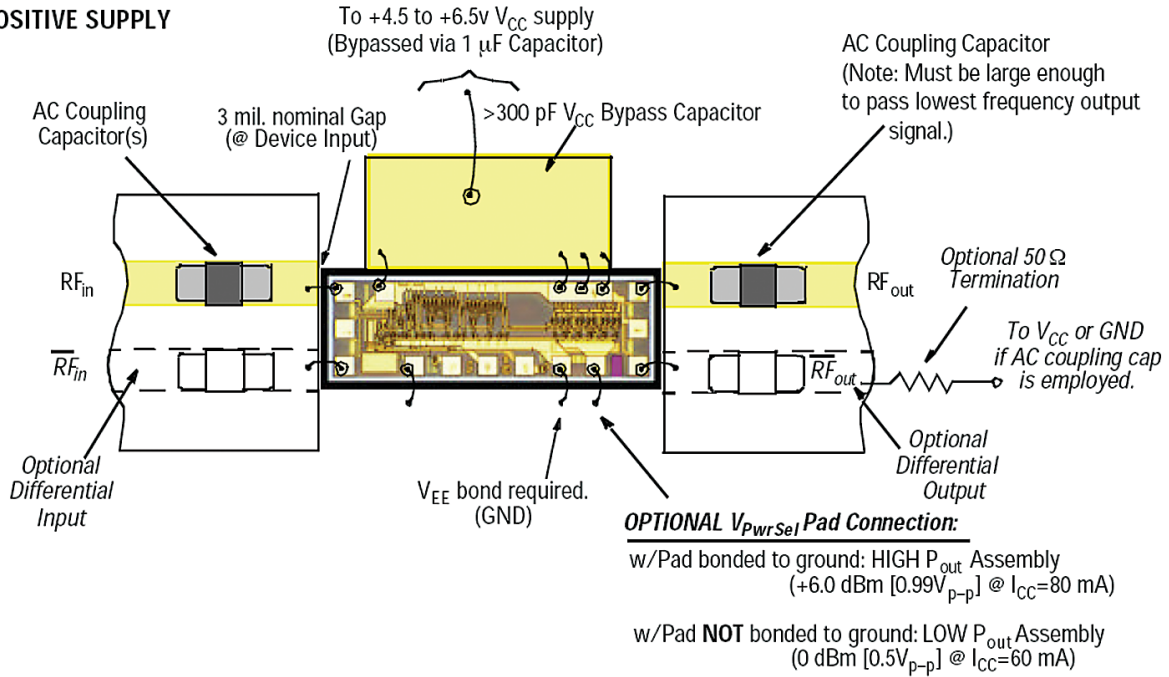


### Notes:

1. All dimensions in micrometers.
2. All pad dim:  $70 \times 70\text{ }\mu\text{m}$  (except where noted).
3. Tolerances:  $\pm 10\text{ }\mu\text{m}$
4. Chip thickness:  $127 \pm 15\text{ }\mu\text{m}$

Figure 2. Pad locations and chip dimensions

**POSITIVE SUPPLY**



**NEGATIVE SUPPLY**

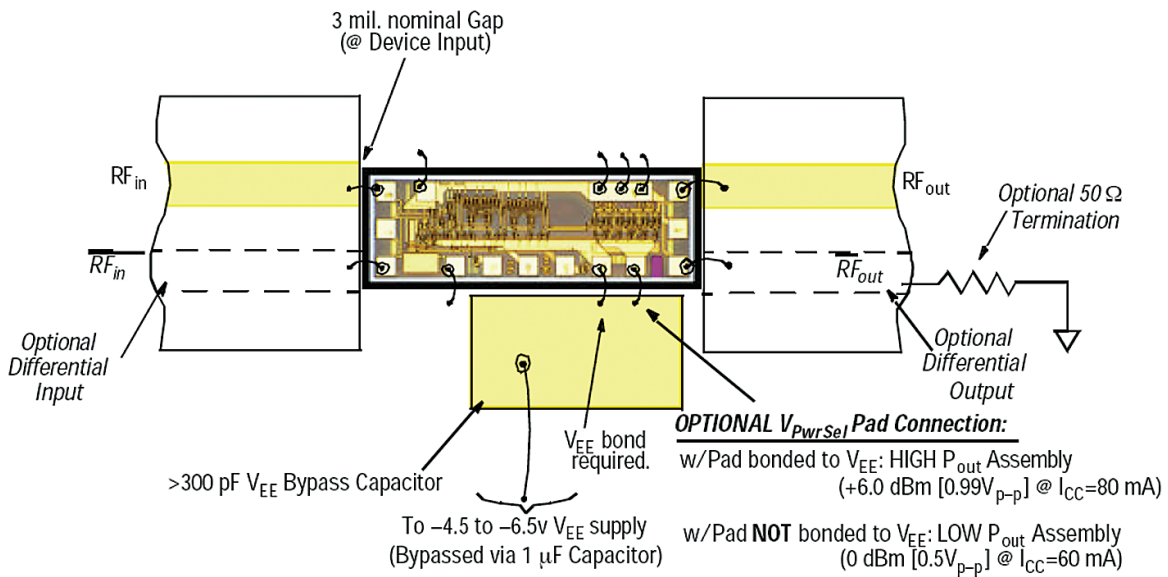


Figure 3. Assembly diagrams



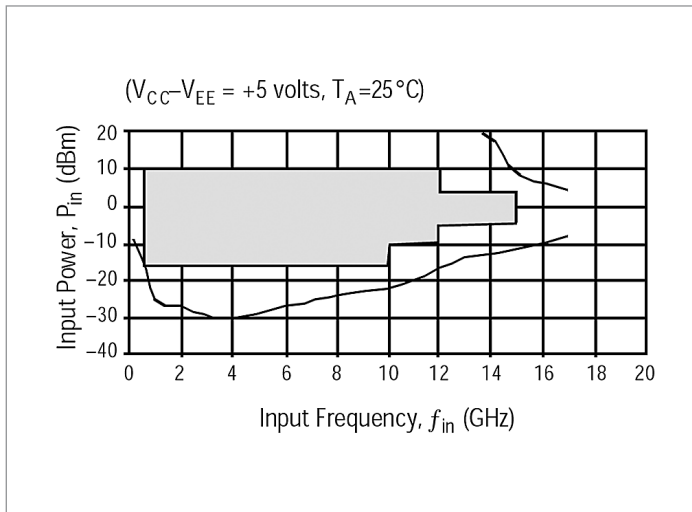


Figure 4. Typical input sensitivity window

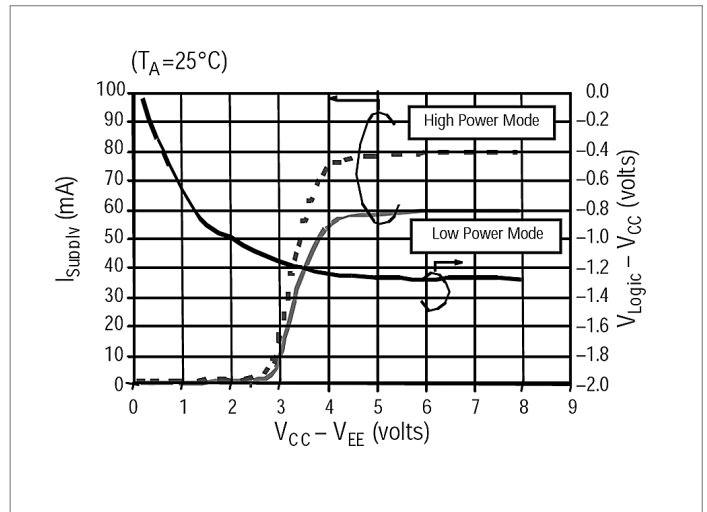


Figure 5. Typical supply current &  $V_{Logic}$  vs. supply voltage

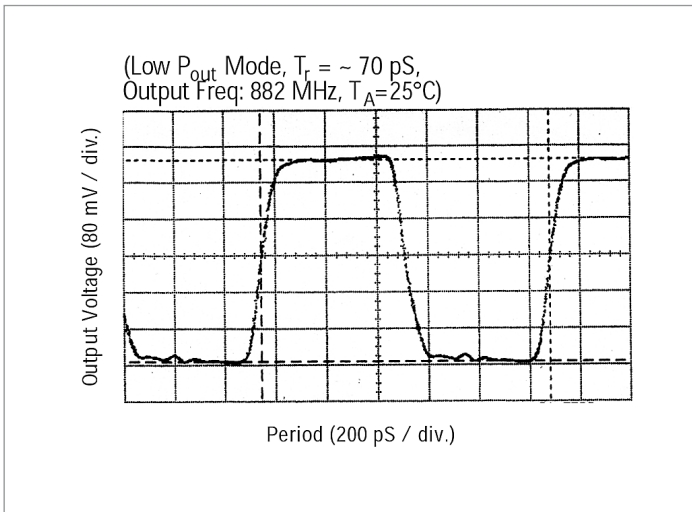


Figure 6. Typical output voltage waveform

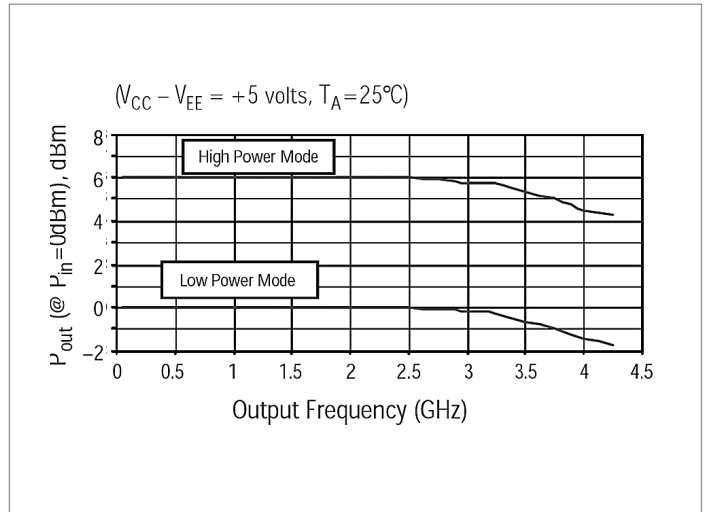


Figure 7. Typical output power vs. output frequency,  $f_{out}$  (GHz)

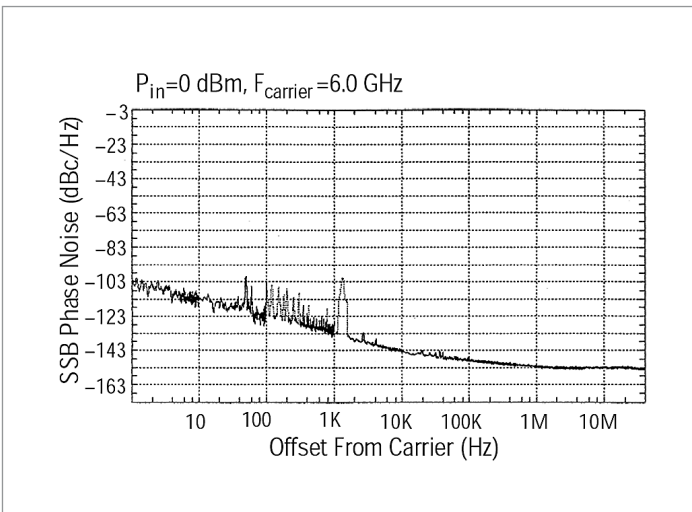


Figure 8. Typical phase noise performance

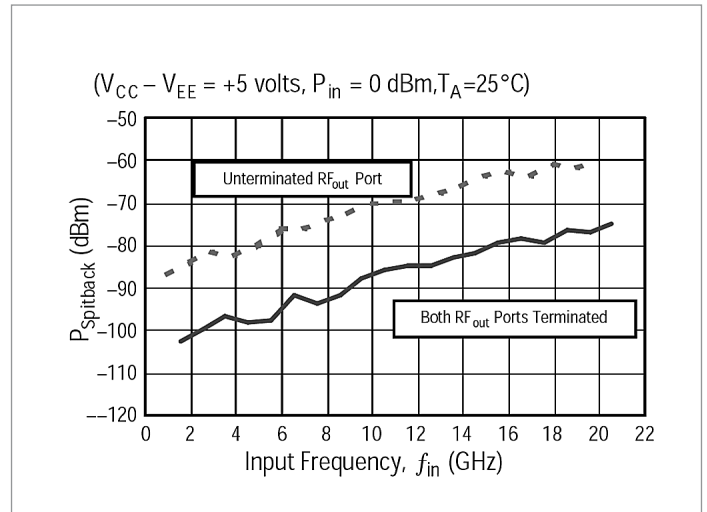


Figure 9. Typical "spitback" power  $P(f_{out})$  appearing at RF input port



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