NCP436, NCP437

3A Ultra-Small Controlled Load Switch with Auto-Discharge Path

The NCP436 and NCP437 are very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail for the NCP437 part only.

Proposed in a wide input voltage range from 1.0 V to 3.6 V, in a small 1 x 1.5 mm WLCSP6, pitch 0.5 mm.

Features

- 1.0 V − 3.6 V Operating Range
- 20 mΩ P MOSFET at 3.6 V
- DC Current Up to 3 A
- Output Auto−discharge
- Active High EN Pin
- WLCSP6 1 x 1.5 mm
- These are Pb−Free Devices

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

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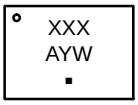
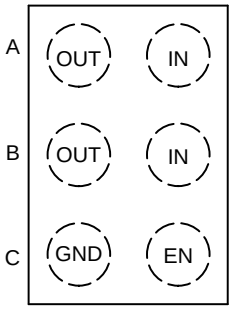
MARKING DIAGRAM

WLCSP6
CASE 567FH



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

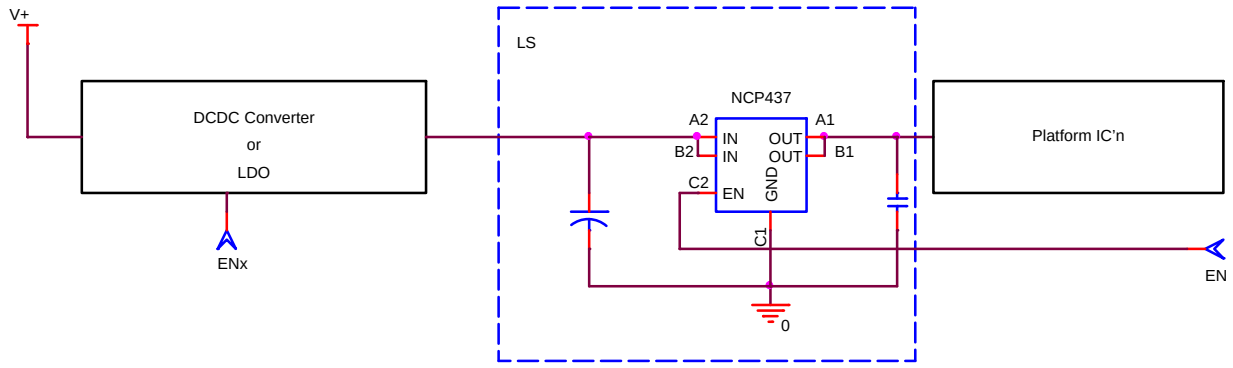


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

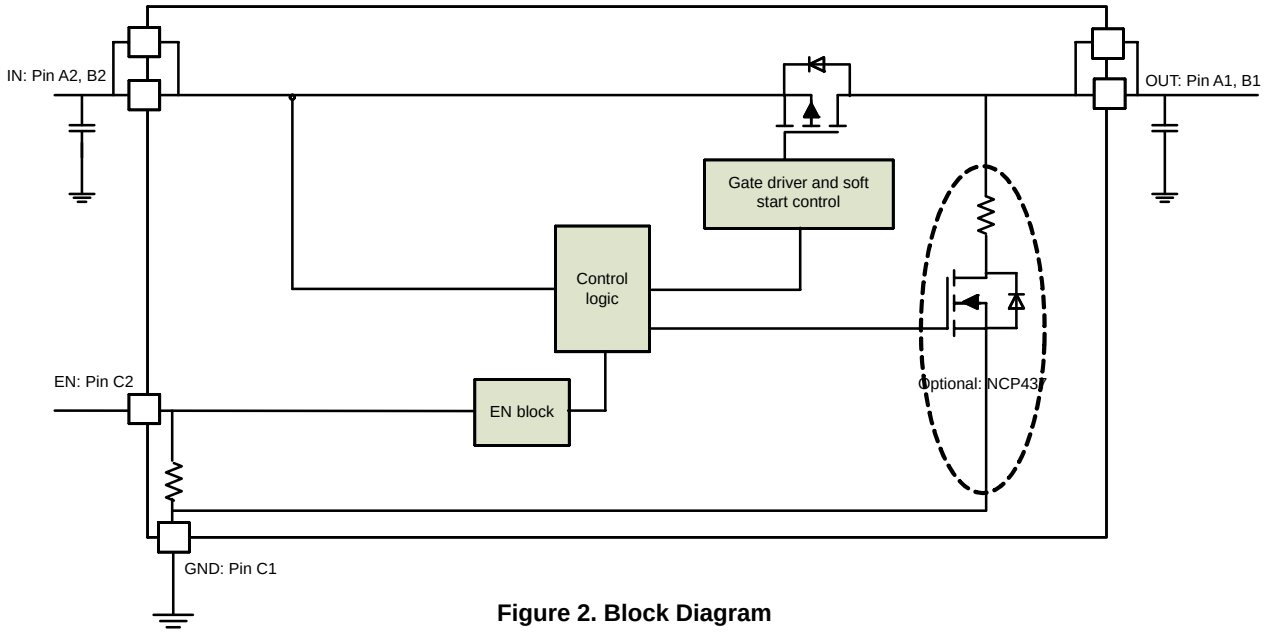


Figure 2. Block Diagram

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{EN} , V_{IN}, V_{OUT}	IN, OUT, EN, Pins: (Note 1)	−0.3 to + 4	V
V_{IN} , V_{OUT}	From IN to OUT Pins: Input/Output (Note 1)	0 to + 4	V
T_J	Maximum Junction Temperature	−40 to + 125	°C
ESD HBM	Human Body Model (HBM) ESD Rating are (Notes 2 and 3)	8000	V
ESD MM	Machine Model (MM) ESD Rating are (Notes 2 and 3)	250	V
ESD CDM	Charge Device Model (CDM) ESD Rating are (Notes 2 and 3)	2000	V
LU	Latch−up Protection (Note) − Pins IN, OUT, EN	100	mA
T_{STG}	Storage Temperature Range	−40 to + 150	°C
MSL	Moisture Sensitivity (Note 2)	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108.
2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
3. This device series contains ESD protection and passes the following tests
   Human Body Model (HBM) ±8.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
4. Latch−up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 Class II.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.0		3.6	V
V_{EN}	Enable Voltage			0		3.6	
T_A	Ambient Temperature Range			−40	25	+85	°C
T_J	Junction Temperature Range			−40	25	+125	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			100		°C/W
I_{OUT}	Maximum DC current					3	A
P_D	Power Dissipation Rating (Note 6)	$T_A \le 25°C$	WLCSP package		0.66		W
		$T_A = 85°C$	WLCSP package		0.26		W

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.3 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 3.6 V	I = 200 mA, 25°C		15	26	mΩ
			I = 200 mA, T_A = 85°C			28	
			T_J = 125°C			29	
		V_{IN} = 2.5 V	I = 200 mA, 25°C		18	30	
			I = 200 mA, T_A = 85°C			32	
			T_J = 125°C			35	
		V_{IN} = 1.8 V	I = 200 mA, 25°C		23	40	
			I = 200 mA, Full Ta			42	
			T_J = 125°C			44	
		V_{IN} = 1.2 V	I = 200 mA, 25°C		45	80	
			I = 200 mA, Full Ta			84	
			T_J = 125°C			85	
		V_{IN} = 1.1 V	I = 200 mA, 25°C		62		
R_{dis}	Output discharge path	V_{IN} = 3.3 V	EN = low	50	65	90	Ω
V_{IH}	High−level input voltage			1.1			V
V_{IL}	Low−level input voltage					0.5	
QUIESCENT CURRENT							
I_{std}	Standby current	V_{IN} = 3.3 V	EN = low, No load		0.01	0.6	μA
Iq	Quiescent current	V_{IN} = 3.3 V	EN = high, No load		0.2	0.6	
TIMINGS							
T_{EN}	Enable time	V_{IN} = 3.6 V (Note 8)	R_L = 25 Ω, C_{OUT} = 1 μF	20	39	55	μs
T_R	Output rise time		R_L = 25 Ω, C_{OUT} = 1 μF	10	25	40	
T_{ON}	ON time (T_{EN} + T_R)		R_L = 25 Ω, C_{OUT} = 1 μF	30	64	95	
T_{DIS}	Disable time		R_L = 25 Ω, C_{OUT} = 1 μF		20		
T_F	Output fall time		NCP437. R_L = 25 Ω, C_{OUT} = 1 μF	20	55	80	

7. Guaranteed by design and characterization
8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

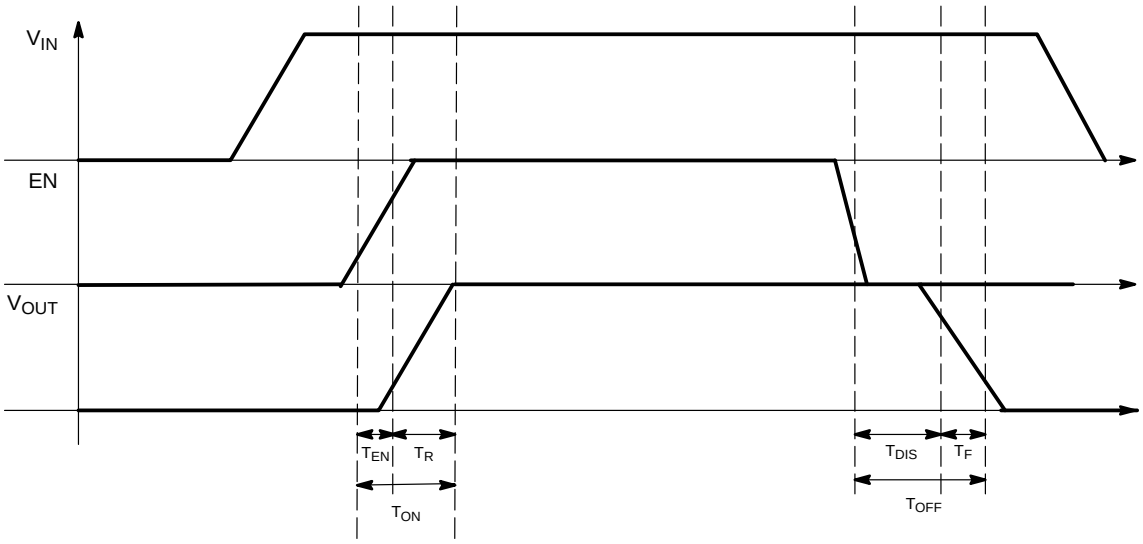


Figure 3. Enable, Rise and Fall Time

FUNCTIONAL DESCRIPTION

Overview

The NCP437 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.0 V to 3.6 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of V_{IN} of 1.2 V and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.2 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at 65 Ω.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = R_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP437 integrates an up to 3 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across two internal inners.

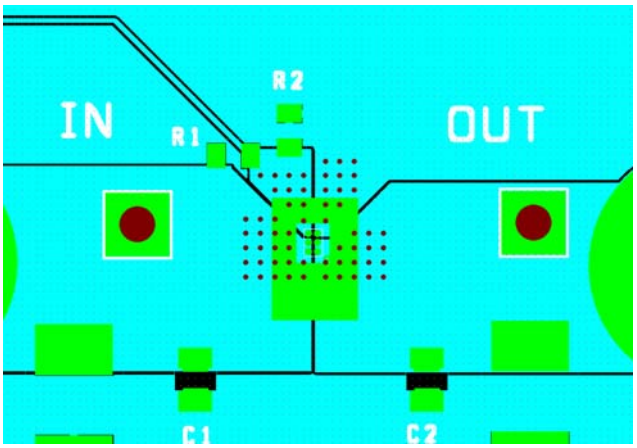


Figure 4.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J: Junction Temperature.
T_A: Ambient Temperature.
R_θ = Thermal resistance between IC and air, through PCB.
$R_{DS(on)}$: Intrinsic resistance of the IC MOSFET.
I: Load DC current.

Taking into account of R_θ obtain with:

- 1 oz, 2 layers: 100°C/W.

At 3 A, 25°C ambient temperature, $R_{DS(on}$ 20 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J = R_{\theta JA} \times P_D = 25 + \left(0.02 \times 3^2\right) \times 100 = 43^\circ C$$

Taking into account of R_θ obtain with:

- 2 oz, 4 layers: 60°C/W.

At 3 A, 65°C ambient temperature, $R_{DS(on)}$ 24 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J = T_A + R_\theta \times P_D = 65 + \left(0.024 \times 3^2\right) \times 60 = 78^\circ C$$

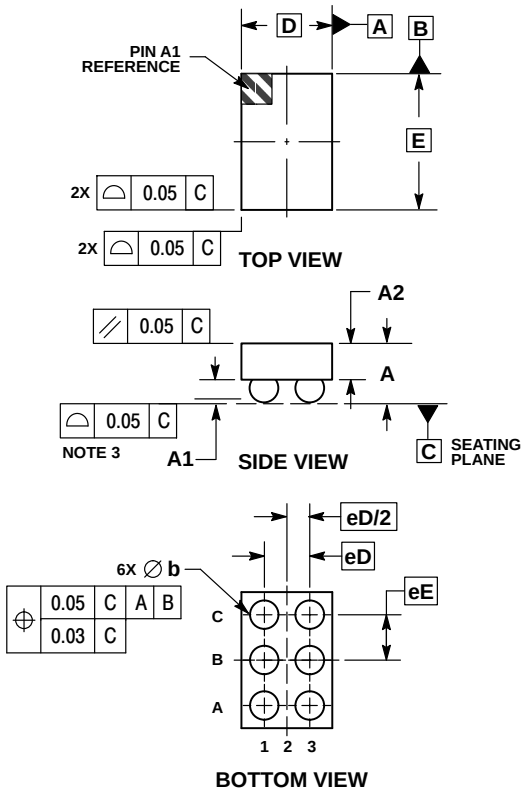
ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCP437FCT2G	AR	Auto discharge	WLCSP 1 x 1.5 mm (Pb−Free)	3000 / Tape & Reel
NCP436FCT2G	AQ	Without Auto discharge	WLCSP 1 x 1.5 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

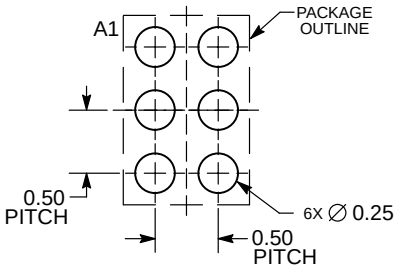
WLCSP6, 1.00x1.50
CASE 567FH
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.54	0.63
A1	0.22	0.28
A2	0.33 REF	
b	0.29	0.34
D	1.00 BSC	
E	1.50 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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