NCP561

150 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP561 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP561 series features an ultralow quiescent current of 3.0 μA. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

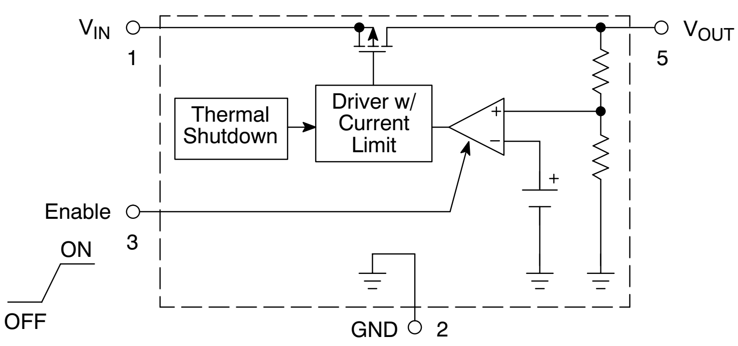
The NCP561 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 1.0 μF. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are 1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V and 5.0 V.

Features

- Low Quiescent Current of 3.0 μA Typical
- Low Dropout Voltage of 170 mV at 150 mA
- Low Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Industrial Temperature Range of −40°C to 85°C
- Pb−Free Packages are Available

Typical Applications

- Battery Powered Instruments
- Hand−Held Instruments
- Camcorders and Cameras



This device contains 28 active transistors

Figure 1. Representative Block Diagram

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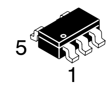
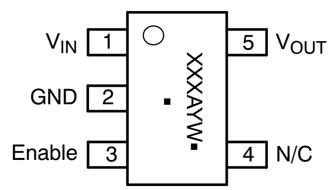


TSOP−5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



(Top View)

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{IN}	Positive power supply input voltage.
2	GND	Power supply ground.
3	Enable	This input is used to place the device into low-power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to V_{IN}.
4	N/C	No internal connection.
5	V_{OUT}	Regulated output voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	6.0	V
Enable Voltage	Enable	−0.3 to V_{IN} +0.3	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} +0.3	V
Power Dissipation and Thermal Characteristics Power Dissipation Thermal Resistance, Junction-to-Ambient	 P_D $R_{\theta JA}$	 Internally Limited 250	 W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL-STD-883, Method 3015
   Machine Model Method 200 V
2. Latchup capability (85°C) ±100 mA DC with trigger voltage.

ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT(nom)}$ + 1.0 V, V_{enable} = V_{IN}, C_{IN} = 1.0 μF, C_{OUT} = 1.0 μF, T_J = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{OUT} = 1.0 mA) 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V	V_{OUT}	 1.455 1.746 2.425 2.646 2.744 2.940 3.234 4.90	 1.5 1.8 2.5 2.7 2.8 3.0 3.3 5.0	 1.545 1.854 2.575 2.754 2.856 3.060 3.366 5.10	V
Line Regulation 1.5 V−4.4 V (V_{IN} = $V_{o(nom)}$ + 1.0 V to 6.0 V) 4.5 V−5.0 V (V_{IN} = 5.5 V to 6.0 V)	Reg_{line}	 – –	 10 10	 20 20	mV
Load Regulation (I_{OUT} = 10 mA to 150 mA)	Reg_{load}	–	30	60	mV
Output Current (V_{OUT} = (V_{OUT} at I_{out} = 150 mA) −3.0%) 1.5 V to 3.9 V (V_{IN} = $V_{o(nom)}$ + 2.0 V) 4.0 V to 5.0 V (V_{IN} = 6.0 V)	$I_{o(nom)}$	 150 150	 – –	 – –	mA
Dropout Voltage (T_A = −40°C to 85°C, I_{OUT} = 150 mA, Measured at V_{OUT} − 3.0%) 1.5 V − 1.7 V 1.8 V − 2.4 V 2.5 V − 2.7 V 2.8 V − 3.2 V 3.3 V − 4.9 V 5.0 V	V_{IN}−V_{OUT}	 – – – – – –	 330 240 150 140 130 120	 500 360 250 230 200 190	mV
Quiescent Current (Enable Input = 0 V) (Enable Input = V_{IN}, I_{OUT} = 1.0 mA to $I_{o(nom)}$)	I_Q	 – –	 0.1 4.0	 1.0 8.0	μA
Output Short Circuit Current 1.5 V to 3.9 V (V_{IN} = $V_{o(nom)}$ + 2.0 V) 4.0 V to 5.0 V (V_{IN} = 6.0 V)	$I_{OUT(max)}$	 160 160	 400 400	 800 800	mA
Output Voltage Noise (f = 20 Hz to 100 kHz, V_{OUT} = 3.0, V I_{OUT} = 1.0 V)	V_n	–	60	–	μVrms
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(en)}$	 1.3 –	 – –	 – 0.2	V
Output Voltage Temperature Coefficient	T_C	–	±100	–	ppm/°C

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

TYPICAL CHARACTERISTICS

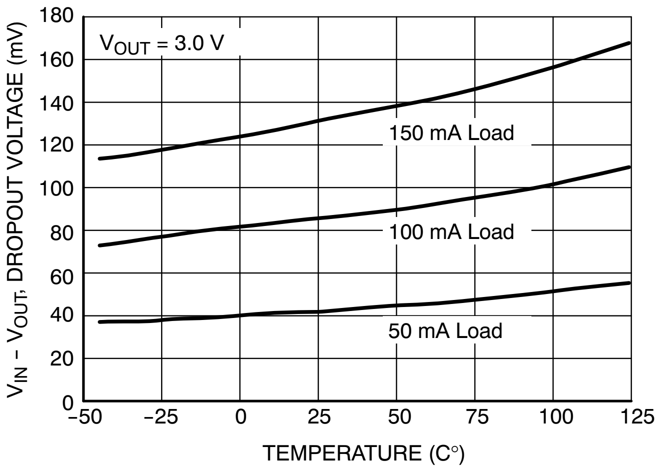


Figure 2. Dropout Voltage vs. Temperature

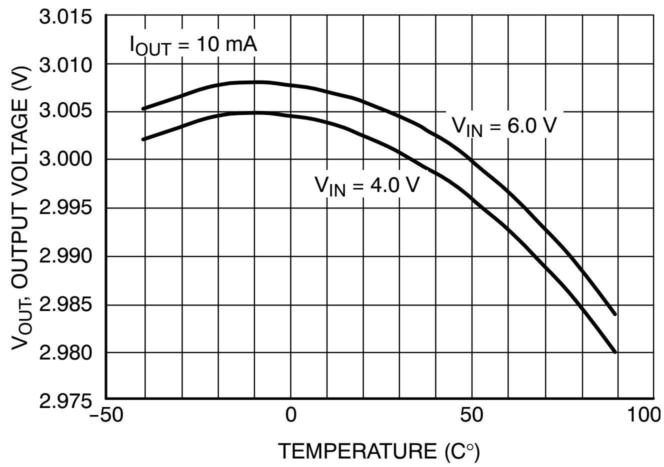


Figure 3. Output Voltages vs. Temperature

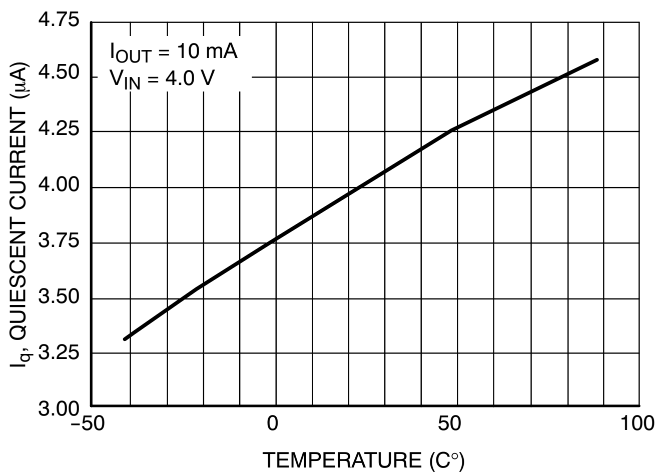


Figure 4. Quiescent Current vs. Temperature

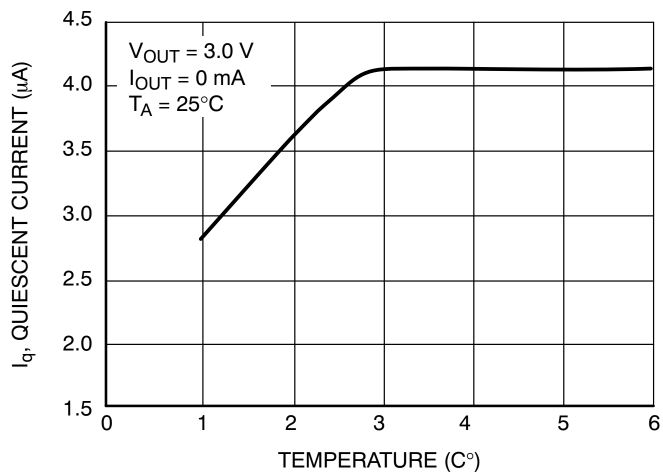


Figure 5. Quiescent Current vs. Input Voltage

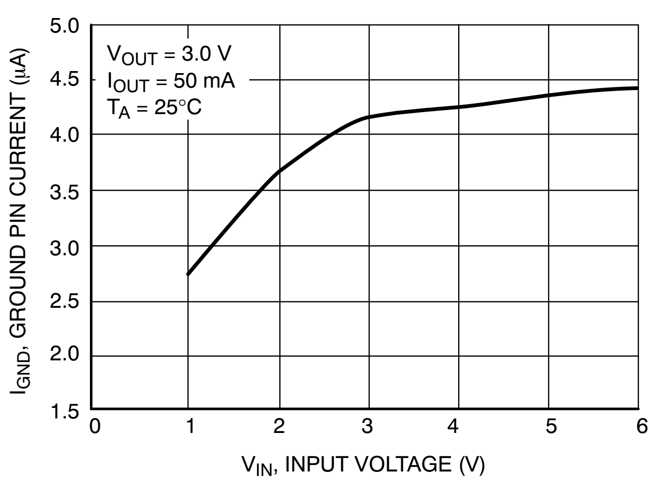


Figure 6. Ground Current vs. Input Voltage

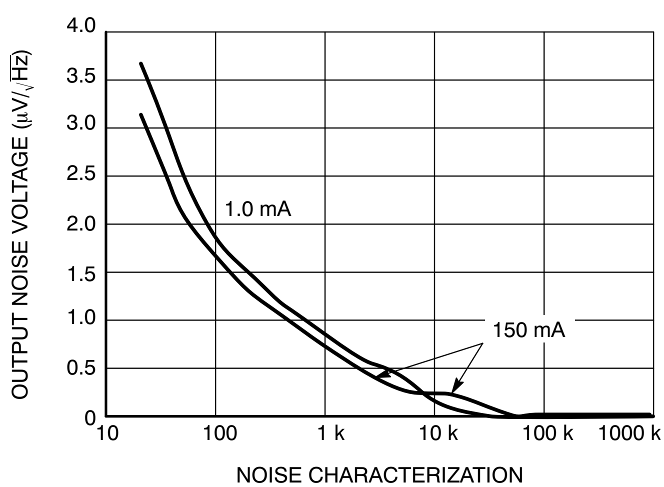


Figure 7. Output Noise Voltage

TYPICAL CHARACTERISTICS

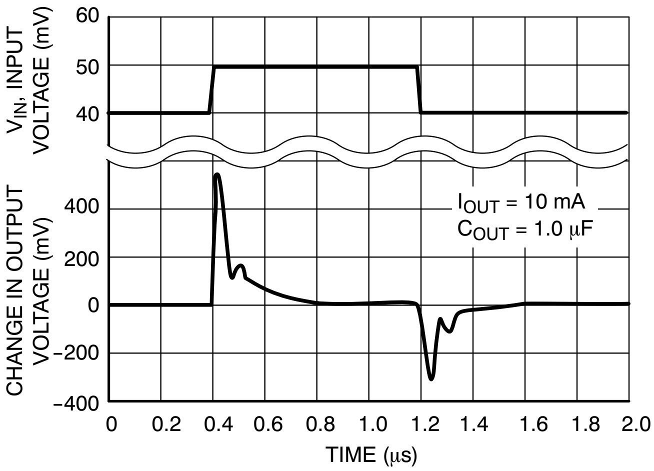


Figure 8. Line Transient Response

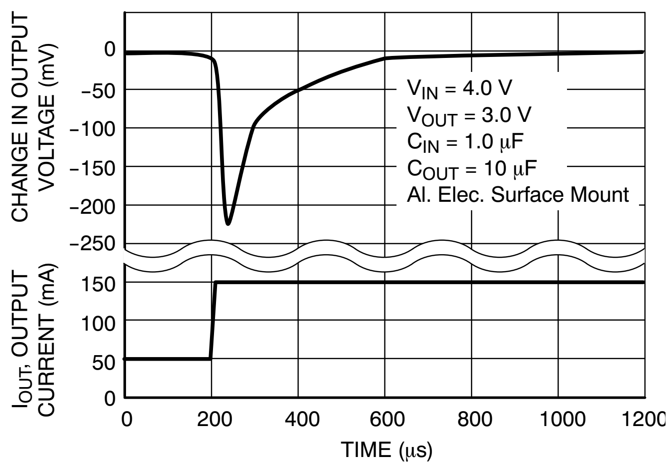


Figure 9. Load Transient Response

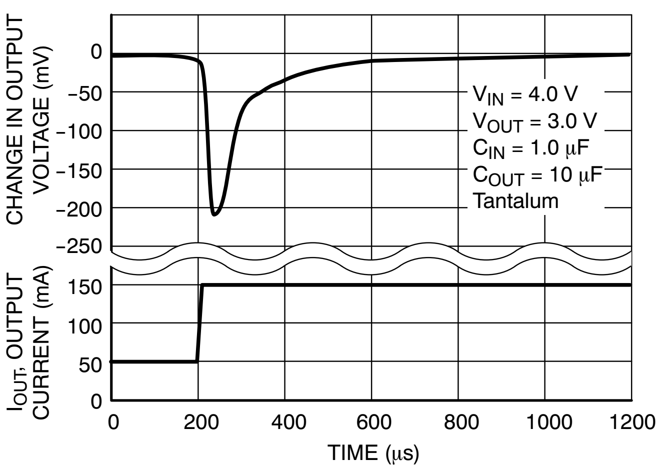


Figure 10. Load Transient Response

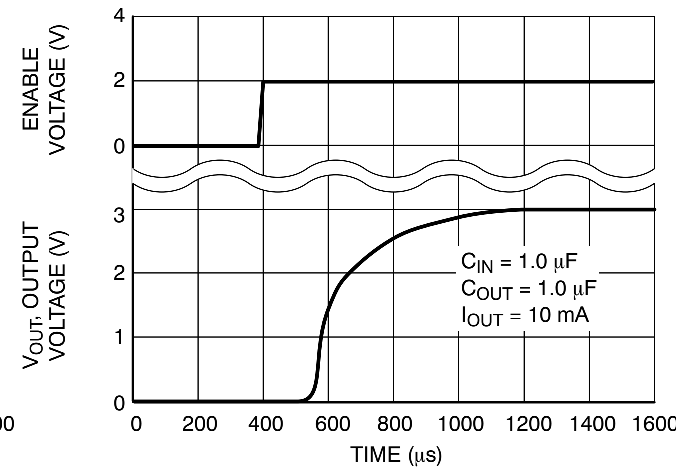


Figure 11. Turn−On Response

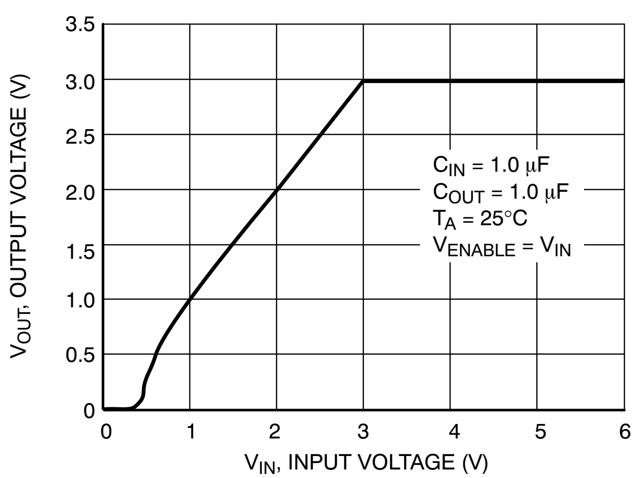


Figure 12. Output Voltage vs. Input Voltage

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

APPLICATIONS INFORMATION

A typical application circuit for the NCP561 series is shown in Figure 13.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP561 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

Output Decoupling (C2)

The NCP561 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K, or C3216X7R1C105K

Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{IN}.

Hints

Please be sure the V_{IN} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads a short as possible.

Thermal

As power across the NCP561 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP561 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the NCP561 can dissipate up to 400 mW @ 25°C.

The power dissipated by the NCP561 can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd}(I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{INMAX} = \frac{P_{TOT} + V_{OUT} * I_{OUT}}{I_{GND} + I_{OUT}}$$

If a 150 mA output current is needed then the ground current from the data sheet is 4.0 μA. For an NCP561SN30T1 (3.0 V), the maximum input voltage will then be 5.6 V.

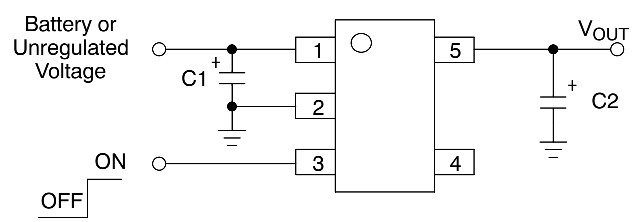


Figure 13. Typical Application Circuit

APPLICATION CIRCUITS

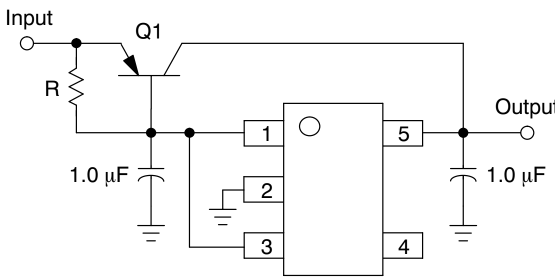


Figure 14. Current Boost Regulator

The NCP561 series can be current boosted with a PNP transistor. Resistor R in conjunction with V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by V_{BE} of the pass resistor.

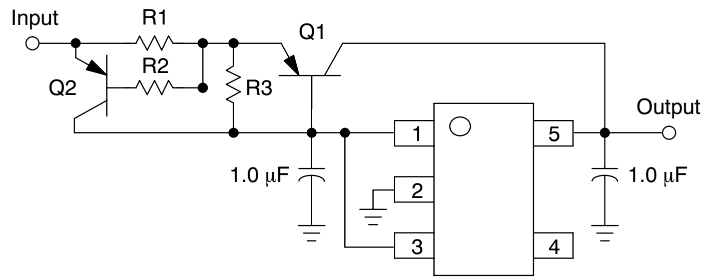


Figure 15. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the V_{BE} of Q2 and R1. I_{SC} = ((V_{BEQ2} − ib * R2) / R1) + $I_{O(max)\ Regulator}$

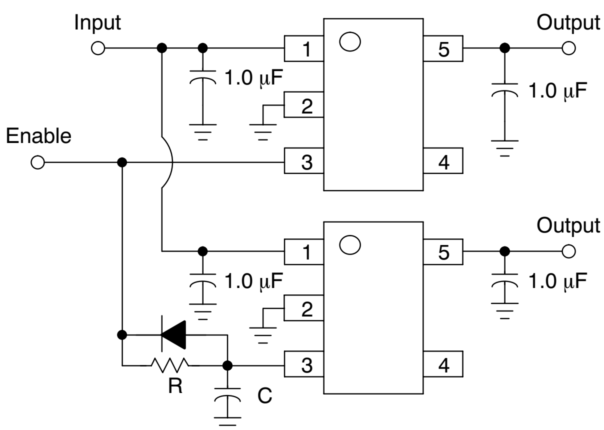


Figure 16. Delayed Turn−on

If a delayed turn−on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C, will delay the turn−on of the bottom regulator.

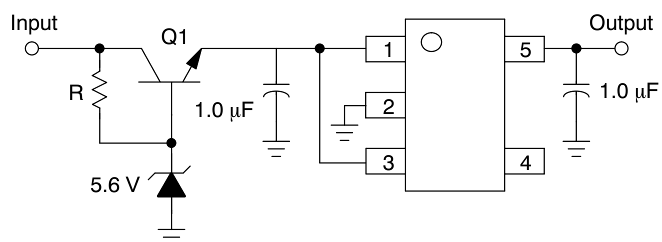


Figure 17. Input Voltages Greater than 6.0 V

A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP561 series with the addition of a simple pre−regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output (V_{OUT}) is shorted to GND.

ORDERING INFORMATION

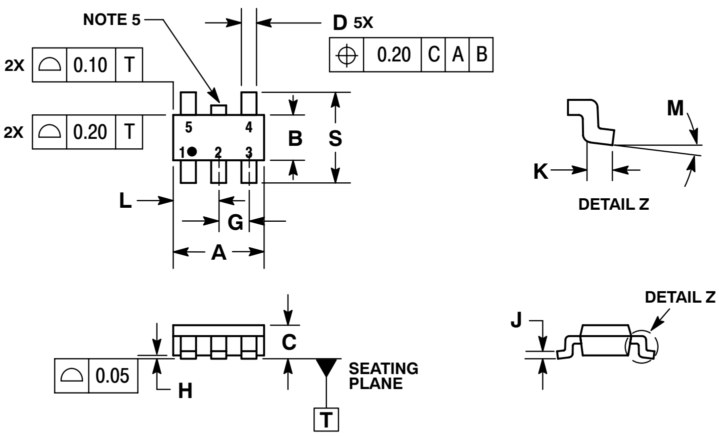
Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP561SN15T1	1.5	LDA	TSOP−5	3000 / 7″ Tape & Reel
NCP561SN15T1G	1.5	LDA	TSOP−5 (Pb−Free)	
NCP561SN18T1	1.8	LEV	TSOP−5	
NCP561SN18T1G	1.8	LEV	TSOP−5 (Pb−Free)	
NCP561SN25T1	2.5	LDC	TSOP−5	
NCP561SN25T1G	2.5	LDC	TSOP−5 (Pb−Free)	
NCP561SN27T1	2.7	LEX	TSOP−5	
NCP561SN27T1G	2.7	LEX	TSOP−5 (Pb−Free)	
NCP561SN28T1	2.8	LDD	TSOP−5	
NCP561SN28T1G	2.8	LDD	TSOP−5 (Pb−Free)	
NCP561SN30T1	3.0	LDE	TSOP−5	
NCP561SN30T1G	3.0	LDE	TSOP−5 (Pb−Free)	
NCP561SN33T1	3.3	LDF	TSOP−5	
NCP561SN33T1G	3.3	LDF	TSOP−5 (Pb−Free)	
NCP561SN50T1	5.0	LDH	TSOP−5	
NCP561SN50T1G	5.0	LDH	TSOP−5 (Pb−Free)	

NOTE: Additional voltages are available upon request by contacting your ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

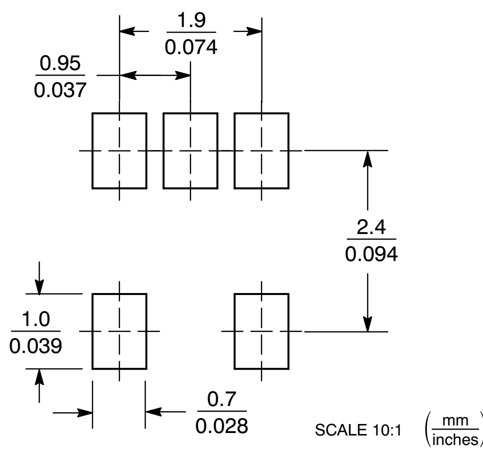
TSOP−5
(SOT23−5, SC59−5)
SN SUFFIX
CASE 483−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
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