3.6A 5V RESETTABLE ELECTRONIC FUSE

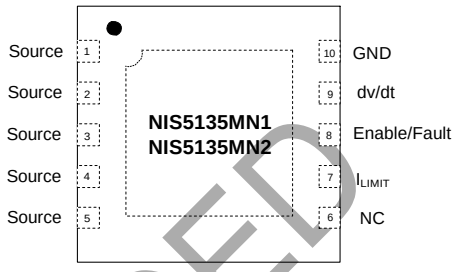
Description

The NIS5135 is a self-protected resettable electronic fuse designed for consumer applications such as hard disk drives to industrial applications to enhance system reliability against catastrophic and shutdown failures.

To support a wide range of demanding applications, the design has been optimized to operate over the supply range of 3.1V to 18V. For robustness and protection, the device integrates a low $R_{DS(ON)}$ NMOS buffer power device along with an undervoltage lockout, overvoltage clamp, a current limit, a dv/dt control and a thermal shutdown circuit. The overvoltage circuit limits the output voltage without shutting the device down to allow the load to continue operating during overvoltage. Thermal shutdown can be either latching type (NIS5135MN1) or auto-retry type (NIS5135MN2).

Pin Assignments

(Top View)



U-DFN3030-10

Features

- 3.1V to 18V Operating Input Voltage
- Integrated NMOS Power Device with $R_{DS(ON)}$ of 30mΩ Typical
- Internal Current Limit - No External Current Sense Resistor in Load Path
- Undervoltage Lockout
- Over Voltage Clamp (NIS5135MN1 and NIS5135MN2)
- Thermal Shutdown
- -40°C to +150°C Operating Junction Temperature
- ESD Ratings: HBM > 1500V; MM 200V
- Small Low Profile U-DFN3030-10 package
- **Totally Lead Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Hard Disk Drives
- Solid State Drives (SSD)
- Set-top Boxes
- DVDs and Blu-ray Disc Drivers
- Mother Board Power Management
- Printer Load Power Management
- Fan Drives

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuits

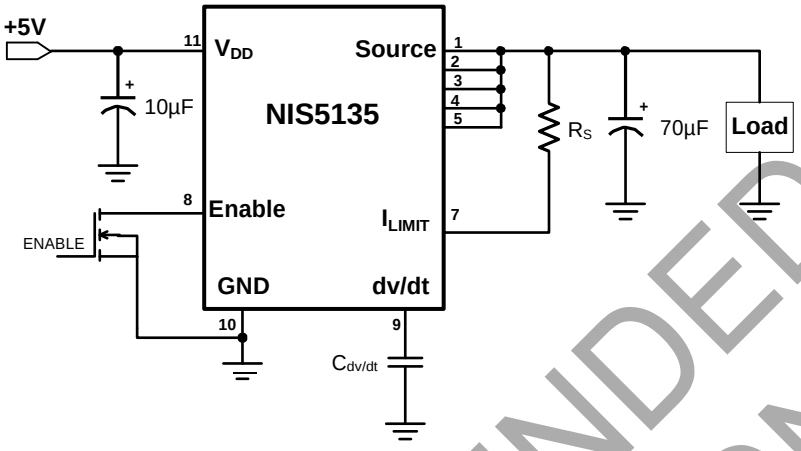


Figure 1. Application Circuit with Direct Current Sensing

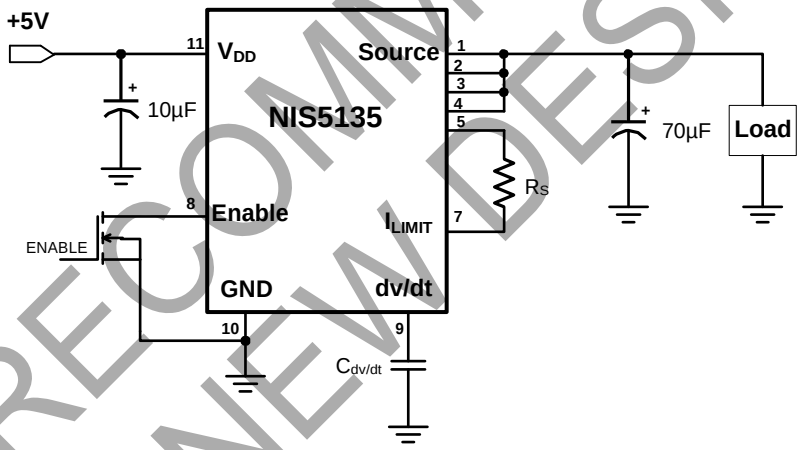


Figure 2. Application Circuit with Kelvin Current Sensing

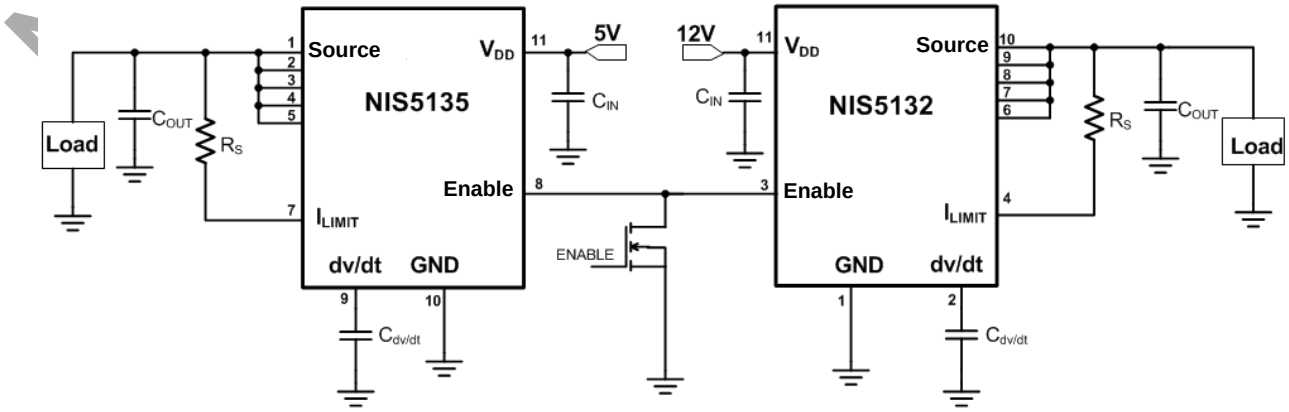
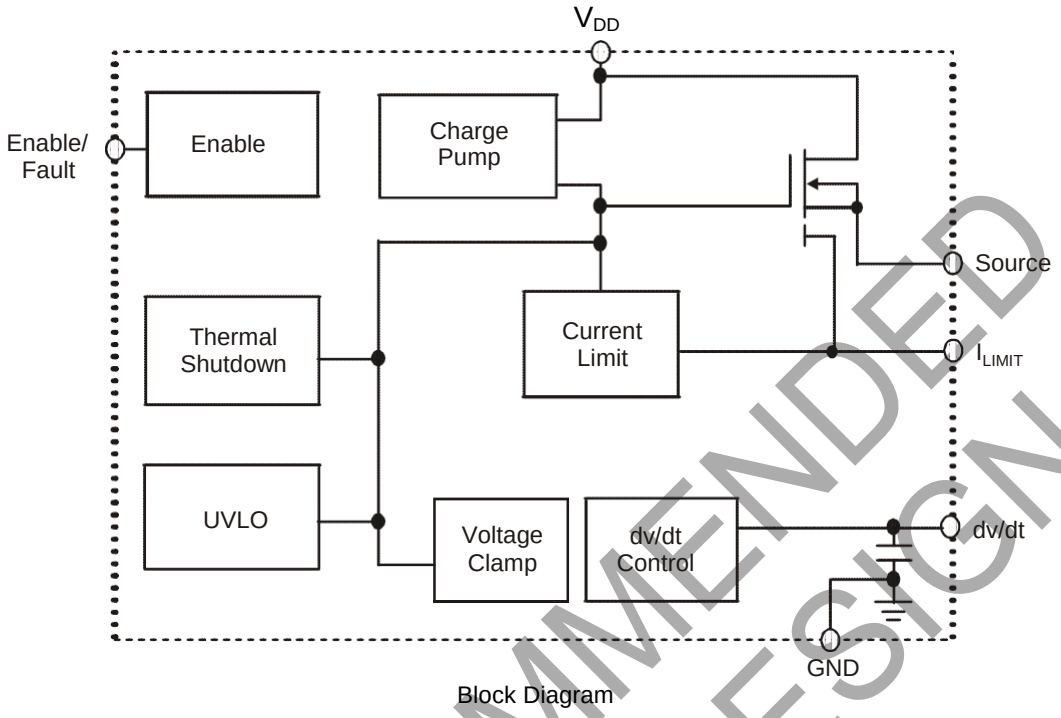


Figure 3. Application Circuit with Common Thermal Shutdown

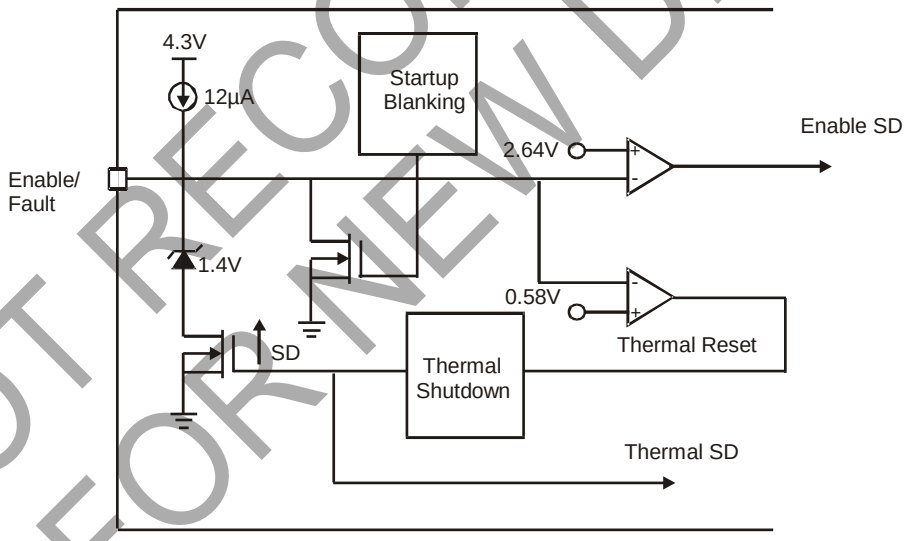
Pin Descriptions

Pin Number	Pin Name	Function
1 to 5	Source	The internal NMOS power device's Source pins: These pins are the Source of internal power device and also the output terminal of the electronic fuse.
6	NC	No internal connection to device Internal NMOS power device turn-on time adjustment pin: If this pin is left unconnected, the internal capacitor ensures the turn-on ramp is over a period of 2ms typical. If an additional delay is required, connect a capacitor from this pin to the ground.
7	I_{LIMIT}	Current limit setting pin: A resistor between Source pins and this pin sets the overload and short-circuit current limit thresholds.
8	Enable/Fault	Tri-state bi-directional interface pin: The output can be disabled by pulling this pin to ground through an open drain or an open collector. Additionally, this pin output goes to an intermediate state to indicate that the device is in thermal shutdown state. This pin can also be connected together with other NIS5135 devices to cause a system-wide simultaneous shutdown during thermal events.
9	dv/dt	Internal NMOS power device turn-on time adjustment pin: If this pin is is left unconnected, the internal capacitor ensures the turn-on ramp is over a period of 2ms typical. If an additional delay is required, connect a capacitor from this pin to the ground.
10	GND	Ground pin
Exposed PAD	V_{DD}	Positive input voltage to the device

Functional Block Diagram



Block Diagram



Enable/Fault Function Circuit

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Characteristic		Value	Unit
V_{DD}	Input Voltage in Steady State Operating Conditions (Note 5)		-0.6 to +18	V
	Input Voltage - Transient (100ms)		-0.6 to +25	
θ_{JA}	Junction to Air Thermal Resistance	0.1 in^2 (Note 6)	227	°C/W
		0.5 in^2 (Note 6)	95	
θ_{JL}	Junction to Lead Thermal Resistance		27	
θ_{JC}	Junction to Case Thermal Resistance		20	
P_{DMAX}	Package Power Dissipation at T_A = +25°C		1.3	W
—	Thermal Derating Above +25°C		10.4	mW/°C
T_S	Storage Temperature Range		-55 to +155	°C
T_J	Operating Junction Temperature (Note 7)		-40 to +150	°C
T_L	Lead Temperature During Soldering (10s)		+260	°C

Notes:
4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Negative voltage will not damage the device provided that the power dissipation is within the package dissipation rating.
6. 1 oz copper on double sided FR-4 PCB.
7. Thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperature above the maximum rating for extended period.

Recommended Operating Conditions

Symbol	Characteristic	Test Condition	Rating	Unit
V_{DD}	Supply Voltage	Operating	3.1 to 18.0	V
T_J	Operating Juntion Temperature Range	Operating	-40 to +150	°C

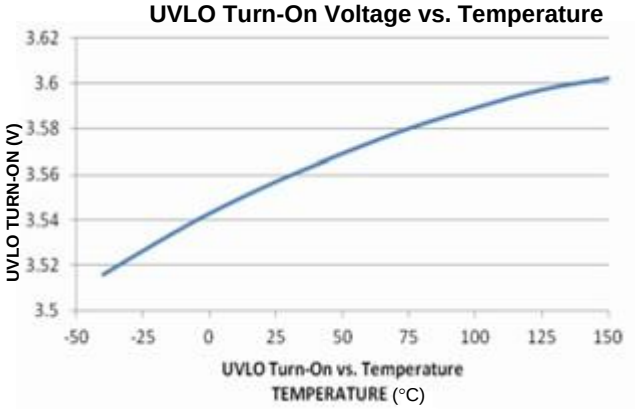
Electrical Characteristics (V_{DD} = 5V, C_L = 70µF, dv/dt pin open, R_{LIMIT} = 10Ω, and T_A = +25°C, unless otherwise noted.)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
Device						
I_{BIAS}	Bias Current	Device Operational	—	0.8	1.5	mA
I_{BIAS_SD}	Bias Current during Shutdown	Device Shutdown	—	0.4	—	mA
V_{DD_MIN}	Minimum Operating Voltage Once Successfully Started Up	—	—	—	3.1	V
NMOS Power Device						
t_{DLY}	Chip Enable Dealy Time	Enabling of the IC to I_D = 100mA (with 1A resistive load)	—	220	—	µs
$R_{DS(ON)}$	NMOS Drain to Source Kelvin ON Resistance (Note 8)	NMOS fully on	20	30	40	mΩ
		NMOS fully on, T_J = +140°C	—	45	—	
V_{OUT_OFF}	Off State Output Voltage	V_{DD} = 10V, V_{GS} = 0V, R_L = ∞	—	0.05	0.2	V
I_D	Continuous Current (Note 9)	T_A = +25°C, 0.5 in.^{2} pad	—	3.6	—	A
		T_A = +80°C, min copper	—	1.7	—	
—	Output Capacitance	V_{DS} = 12V, V_{GS} = 0V, f = 1MHz	—	230	—	pF
dv/dt Ramp						
t_{SLEW}	Output Voltage Ramp Time	Device enable to V_{DS} = 11.7V	0.7	1.4	2.4	ms
V_{C_MAX}	Maximum Capacitor Voltage	—	—	—	V_{DD}	V
Under/Overvoltage Protection						
V_{UVLO}	Undervoltage Lockout Threshold	Turn on, Voltage rising	3.2	3.6	4.0	V
V_{UVLO_HYST}	Undervoltage Lockout Hysteresis	—	—	0.40	—	V
V_{CLAMP}	Overvoltage Clamp Limit (Note 10)	During over voltage protection, V_{DD} = 18V	5.95	6.65	7.35	V
Current Limit						
I_{LIMIT_SS}	Kelvin Short Circuit Current Limit (Note 11)	R_{LIMIT} = 11Ω	2.3	3.1	4.4	A
I_{LIMIT_OL}	Kelvin Over Load Current Limit (Note 11)	R_{LIMIT} = 11Ω	—	3.5	—	A
Thermal Protection						
T_{SD}	Thermal Shutdown Junction Temperature Threshold (Note 9)	Temperature rising	+150	+175	+200	°C
T_{SD_HYST}	Thermal Shutdown Hysteresis in Non Latching Devices	—	—	+45	—	°C
Enable/Fault						
V_{EN_LOW}	Enable Logic Level Low Voltage	Output disabled	0.35	0.58	0.81	V
V_{EN_MID}	Enable Logic Level Mid Voltage	Output disabled, Thermal fault	0.82	1.4	1.95	V
V_{EN_HI}	Enable Logic Level High	Output enabled	1.96	2.64	3.3	V
V_{EN_MAX}	High State Maximum Voltage	—	3.4	4.3	5.3	V
I_{EN_SINK}	Logic Low Sink Current	V_{ENABLE} = 0V	—	-12	-20	µA
I_{EN_LKG}	Logic High Leakage Current for External Switch	V_{ENABLE} = 3.3V	—	—	1.0	µA
Fanout	Maximum Fanout – Number of device that can be connected together to this pin for simultaneous shutdown	—	—	—	3.0	Units

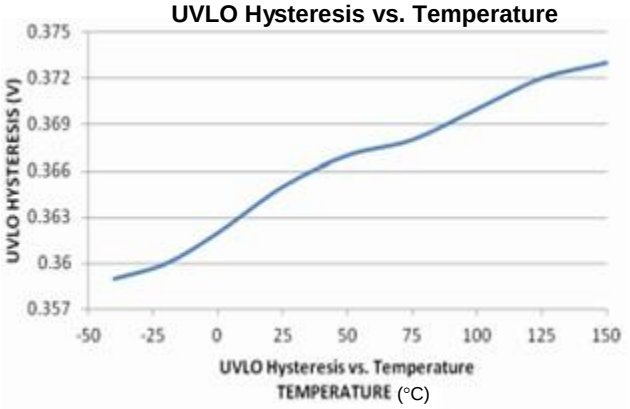
Notes:
8. Pulse test with pulse width of 300µs, duty cycle 2%.
9. This parameter is not tested in production. It is guaranteed by design, process control and characterization.
10. Overvoltage clamp feature is available on in NIS5135MN1 and NIS5135MN2 versions.
11. Refer to application note on explanation on short circuit and overload conditions.

Performance Characteristics

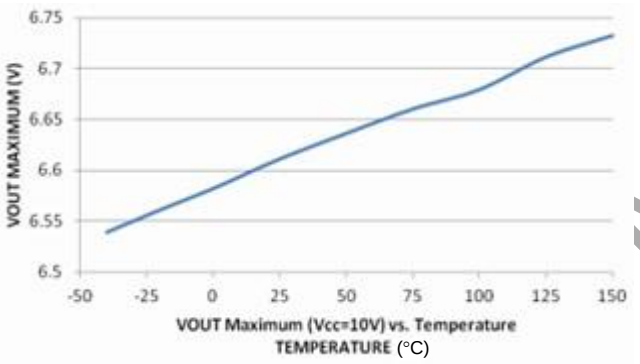
UVLO Turn-On Voltage vs. Temperature



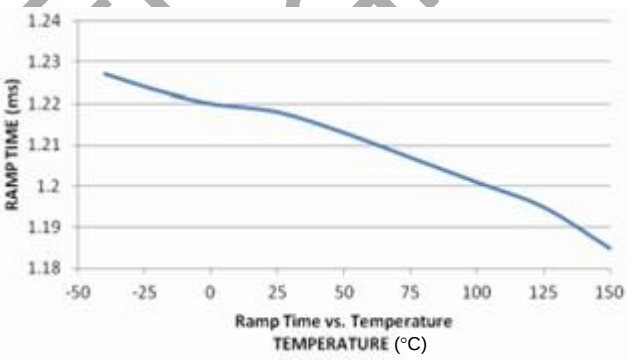
UVLO Hysteresis vs. Temperature



Output Clamp Voltage vs. Temperature

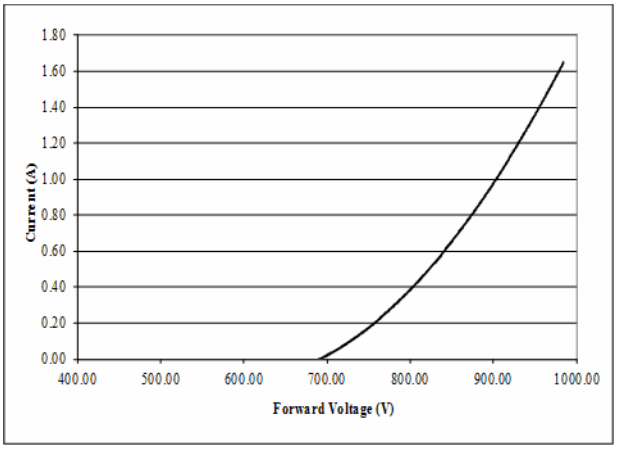


Output Voltage dv/dt Ramp Time vs. Temperature



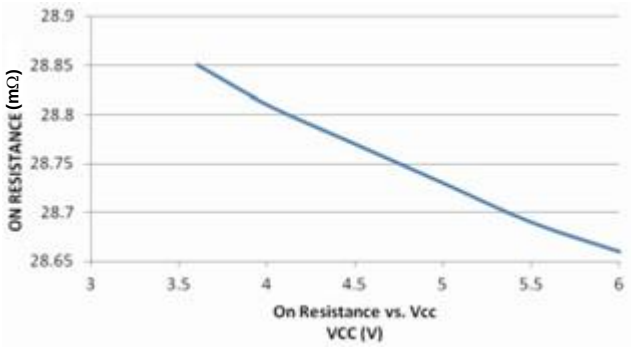
Input Transient Response

Body Diodes Forward Characteristics

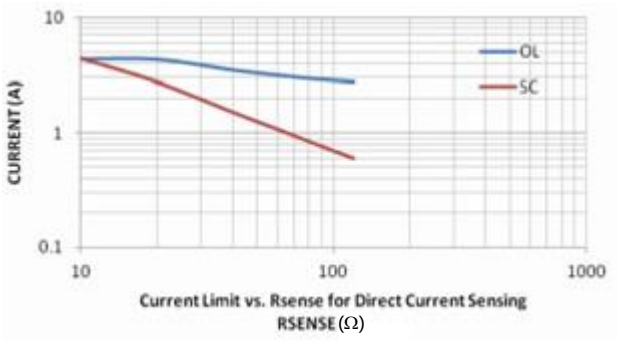


Performance Characteristics (Cont.)

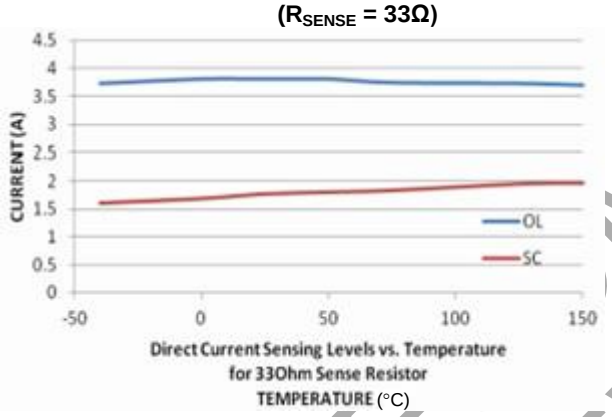
Power Device ON Resistance ($R_{DS(ON)}$) vs. V_{CC}



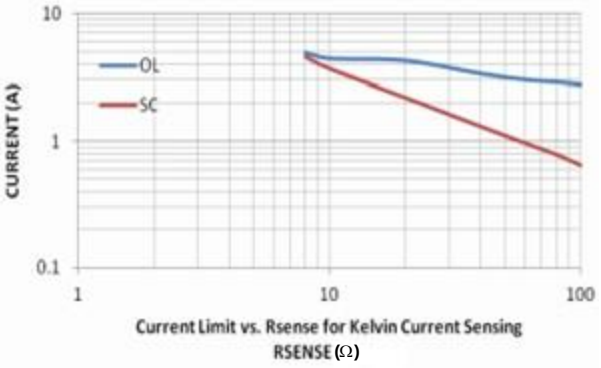
Current Limit vs. R_{SENSE} for Direct Current Sensing



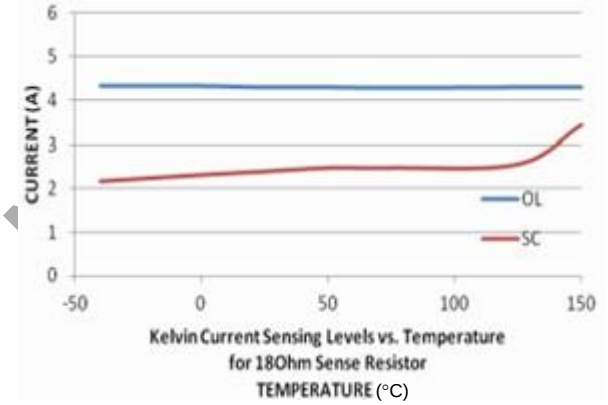
Direct Current Sensing Level vs. Temperature (R_{SENSE} = 33Ω)



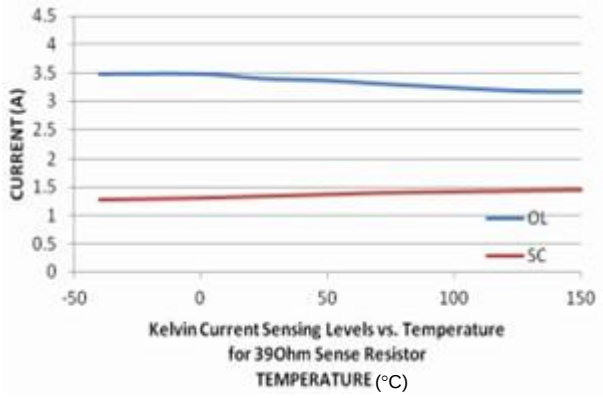
Current Limit vs. R_{SENSE} for Kelvin Current Sensing



Kelvin Current Sensing Levels vs. Temperature (R_{SENSE} = 18Ω)



Kelvin Current Sensing Levels vs. Temperature (R_{SENSE} = 39Ω)



Application Note

Theory of Operation

The NIS5135 is a self-protected, resettable electronic fuse. It monitors the input and output voltage, the output current and the die temperature. When the NIS5135 is powered up it will ramp up the output voltage based on the dv/dt setting (see description below) and current will begin to flow. The device current limit can be set with an external resistor, the ramp rate (dv/dt) can be adjusted with an external capacitor. The Overvoltage Clamp, Undervoltage Lockout and Thermal Protection are internally set.

Power Supply Considerations

Placing a high-value electrolytic capacitor or X7R (X5R) ceramic capacitor between V_{DD} to GND (10µF) and Source to GND (70µF) as close to the device as possible is highly recommended. This precaution reduces power-supply transients that may cause ringing on the input and load transients that may cause output voltage falls below input voltage resulting device over-heat.

Current Limit

The NIS5135 incorporates a sensefet with a reference and amplifier to control the current in the device. The sensefet uses a small fraction of the load current to measure the actual current. This reduces the losses as a smaller sense resistor can be used. The current can be measured directly with the R_s resistor connected between the load and the I_{LIMIT} pin (see Figure 1). That method includes the resistance of the bond wires in the current limiting circuit. A Kelvin connection (see Figure 2) can be used also; in that case one of the 5 source pins will be used and the voltage is measured on the die, eliminating the bond wire resistance. That reduces the Source pins to the load to four and therefore increases the on-resistance of the effuse to the load.

Overvoltage Clamp

The NIS5135MN1 and NIS5135MN2 monitor the input voltage and clamp it once it exceeds 6.65V. This will allow for transient on the input for short periods of time. If the input voltage stays above 6.65V for extended time the voltage drop across the FET with the load current will increase the die temperature and the thermal shutdown feature will protect the device and shut it down.

Undervoltage Lock Out

The input voltage of the NIS5135 is monitored by an UVLO circuit (undervoltage lockout) if the input voltage drops below this threshold the output transistor will be pulled into a high impedance state.

dv/dt

The NIS5135 has an integrated control circuit that forces a linear ramp on the output voltage raise regardless of the load impedance. Without connecting a capacitor on the dv/dt pin the ramp time is roughly 2ms. Adding an external capacitor can increase this ramp rate. The internal current source of 90µA will charge the external capacitor at a slow rate. It is recommended to utilize a ceramic capacitor.

The ramp time can be determined with the following equation:

$$t_{ramp} = 30e^{6}(50pF + C_{ext})$$

$$C_{ext} = \frac{t_{ramp}}{30e^{6}} - 50pF$$

C_{ext} in Farad
t_{ramp} in seconds

The ramp-up circuit is discharged and V_{OUT} starts from 0V when the units shut down after a fault, enable shutdown or input power cycle.

Enable/Fault

The NIS5135 has a tri state Enable/Fault pin. It is used to turn on and off the device with high and low signals from a GPIO, but can also indicate a thermal fault. When the Enable/Fault pin is pulled low, the output is turned off. When the Enable/Fault pin is pulled high, the output is turned on. In the event of a thermal fault, the Enable/Fault pin will be pulled low to an intermediate voltage by an internal circuit. This can be used to chain up to 4 NIS5135 together that during a thermal shut down the linked devices turn off as well.

Due to this fault indication capability, it should not be connected to any type of logic with an internal pull up device.

The NIS5135MN1 connected to a 2nd device will latch off until the Enable/Fault pin has been pulled to low and then allowed to go back up to a high signal, or if the power has been cycled. Once the part starts up again it will go through the start up ramp determined by the internal circuit or based on the externally connected capacitor on pin dv/dt.

The MN2 devices will auto restart once the part that indicated a thermal shutdown has cooled down. It will also go through the start up ramp.

Application Note (Cont.)

Enable/Fault (Cont.)

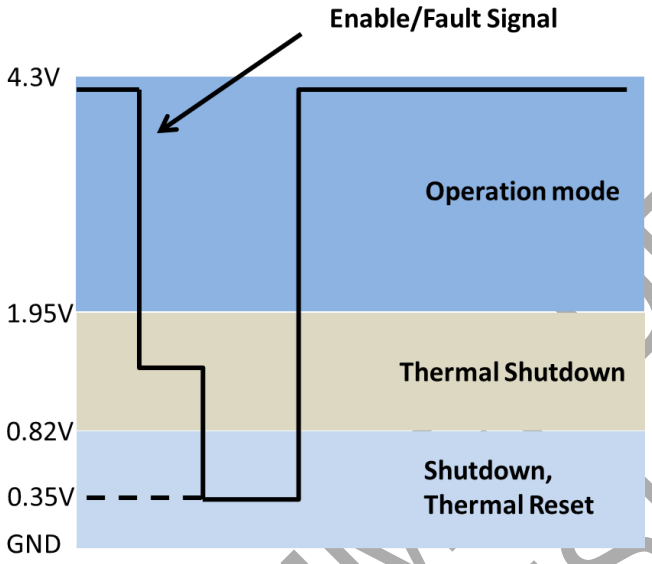


Figure 4. Enable/Fault Signal Levels

Thermal Protection

The NIS5135 has an integrated temperature sensing circuit that protects the die in the event of over temperature. The trip point has been intentionally set high at +175˚C to allow for increased trip times during high power transient events. The NIS5135 will shut down current flow to the output when the die temperature reaches +175°C. The NIS5135MN1 will restart after the Enable pin has been toggled or the input power has been cycled. The NIS5135MN2 will auto restart after the die temperature has been reduced by -45°C.

Even though the thermal trip point has been set high to allow for high current transients the circuit design should accomplish best thermal performance with good thermal layout of the PCB. It is not recommended to operate NIS5135 above +150°C over extended periods of time.

Ordering Information

NIS5135 XXX - XX - 7

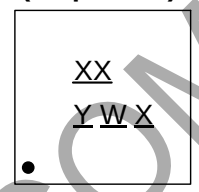
Feature Option	Package	Packing
MN1 : Thermal Latching with V_{CLAMP} MN2 : Thermal Auto-retry with V_{CLAMP}	FN : U-DFN3030-10	7 : Tape & Reel

Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
NIS5135MN1-FN-7	FN	U-DFN3030-10	3,000/Tape & Reel	-7
NIS5135MN2-FN-7	FN	U-DFN3030-10	3,000/Tape & Reel	-7

Marking Information

(1) Package Type: U-DFN3030-10

(Top View)



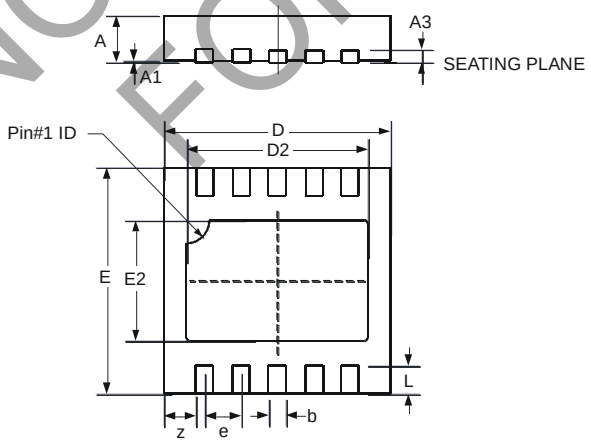
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal Code

Part Number	Package	Identification Code
NIS5135MN1-FN-7	U-DFN3030-10	M5
NIS5135MN2-FN-7	U-DFN3030-10	N5

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN3030-10

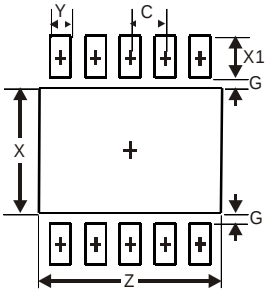


U-DFN3030-10			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	-	-	0.50
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
L	0.25	0.55	0.40
z	-	-	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

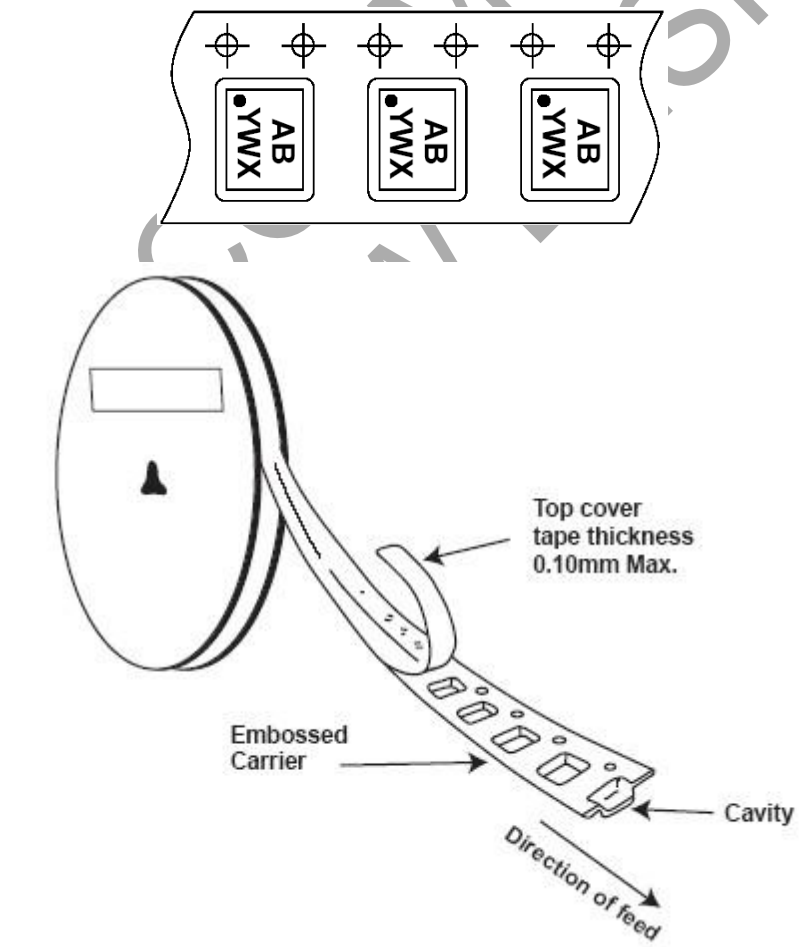
U-DFN3030-10



Dimensions	Value (in mm)
Z	2.60
G	0.15
X	1.80
X1	0.60
Y	0.30
C	0.50

Taping Orientation

(1) Package Type: U-DFN3030-10



Note: 12. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf.

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