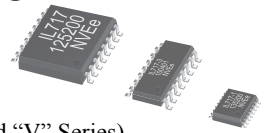
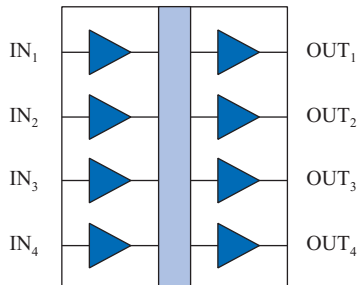


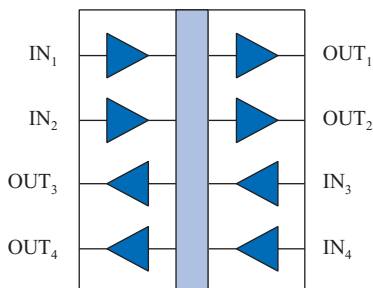
## High Speed Four-Channel Digital Isolators



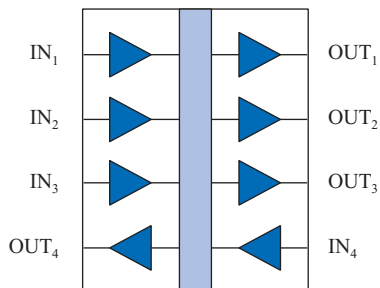
### Functional Diagrams



**IL715**



**IL716**



**IL717**

### Features

- High speed: 110 Mbps
- High temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (“T” and “V” Series)
- Very high isolation: 6 kV<sub>RMS</sub> Reinforced Isolation (V-Series)
- High working voltage: 1 kV<sub>RMS</sub> per VDE V 0884-10 (V-Series)
- 50 kV/ $\mu\text{s}$  typical common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- 1.2 mA/channel typical quiescent current
- 100 ps pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- 44000 year barrier life
- Excellent magnetic immunity
- VDE V 0884-10 certified; UL 1577 recognized
- 0.15" and 0.3" True 8™ mm 16-pin SOIC; 16-pin QSOP packages

### Applications

- ADCs and DACs
- Digital Fieldbus
- Multiplexed data transmission
- Board-to-board communication
- Ground loop elimination
- Parallel bus
- Logic level shifting
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV<sub>RMS</sub> rated IEC 60601-1 medical applications

### Description

NVE’s IL715, IL716, and IL717 four-channel high-speed digital isolators are CMOS devices manufactured with NVE’s patented\* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator.

Typical transient immunity of 50 kV/ $\mu\text{s}$  is unsurpassed. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

The IL715, IL716, and IL717 are available in 16-pin 0.3" and 0.15" SOIC, and ultraminiature QSOP packages.

Performance is specified over a temperature range of  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ . “T” and “V” Series parts have a maximum operating temperature of  $125^{\circ}\text{C}$ .

V-Series versions have an extremely high isolation voltage of 6 kV<sub>RMS</sub>.

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Junction Temperature	$T_J$	-55		150	°C	
Ambient Operating Temperature <sup>(1)</sup> “T” and “V” Versions	$T_A$	-40		100 125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature “T” and “V” Versions	$T_A$	-40		100 125	°C	
Junction Temperature “T” and “V” Versions	$T_J$	-40		110 125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	3.0		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	μs	

## Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	QSOP 0.15" SOIC 0.3" SOIC	4.03 4.03 8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.012	0.016		mm	
Leakage Current <sup>(5)</sup>			0.2		μA	240 $V_{RMS}$ , 60 Hz
Barrier Resistance <sup>(5)</sup>			$>10^{14}$		Ω	500 V
Barrier Capacitance <sup>(5)</sup>			4		pF	f = 1 MHz
Comparative Tracking Index	QSOP 0.15" SOIC 0.3" SOIC	≥175 ≥175 ≥600			$V_{RMS}$	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	1000 1500			$V_{RMS}$ $V_{DC}$	At maximum operating temperature
Surge Immunity (“V” Versions)	$V_{IOSM}$	12.8			kV <sub>PK</sub>	Per IEC 61000-4-5
Barrier Life			44000		Years	100°C, 1000 $V_{RMS}$ , 60% CL activation energy

## Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	$\theta_{JA}$		60 60 60		°C/W	Soldered to double-sided board; free air
Junction–Case (Top) Thermal Resistance	$\Psi_{JT}$		10 10 20		°C/W	
Power Dissipation	$P_D$			675 700 800	mW	

## Safety and Approvals

### VDE V 0884-10 (VDE V 0884-11 pending)

V-Series (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage ( $V_{IORM}$ ) 1000  $V_{RMS}$  (1415  $V_{PK}$ ); reinforced insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 6000  $V_{RMS}$
- Surge immunity ( $V_{IOSM}$ ) 12.8 k $V_{PK}$
- Surge rating 8 kV
- Transient overvoltage ( $V_{IOTM}$ ) 6000  $V_{PK}$
- Each part tested at 2387  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 6000  $V_{PK}$  for 60 sec.; then 2122  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600  $V_{RMS}$  (848  $V_{PK}$ ); basic insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 2500  $V_{RMS}$
- Transient overvoltage ( $V_{IOTM}$ ) 4000  $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	$T_S$	180	°C
Safety rating power (180°C)	$P_S$	270	mW
Supply current safety rating (total of supplies)	$I_S$	54	mA

### IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	QSOP	300 $V_{RMS}$
-3	0.15" SOIC	300 $V_{RMS}$
None	0.3" SOIC (standard)	300 $V_{RMS}$
V	0.3" SOIC (high isolation voltage)	1000 $V_{RMS}$

### UL 1577 (Component Recognition Program File Number E207481)

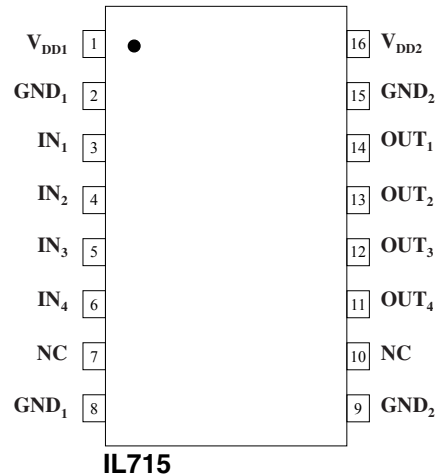
- 6 kV-rated V-Series parts tested at 7.2 k $V_{RMS}$  (10.2 k $V_{PK}$ ) for 1 second; each lot sample tested at 6 k $V_{RMS}$  (8485  $V_{PK}$ ) for 1 minute
- 2.5 kV-rated parts tested at 3000  $V_{RMS}$  (4240  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3530  $V_{PK}$ ) for 1 minute

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1

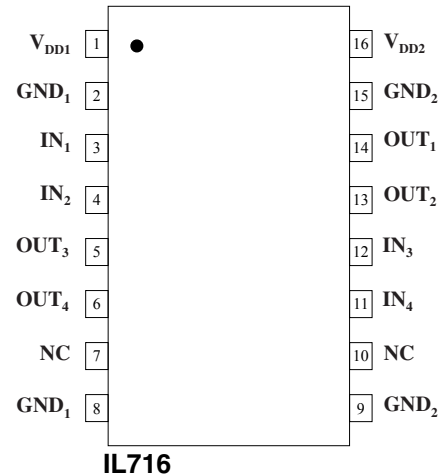
## IL715 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	IN <sub>4</sub>	Data in, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
10	NC	No connection
11	OUT <sub>4</sub>	Data out, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



## IL716 Pin Connections

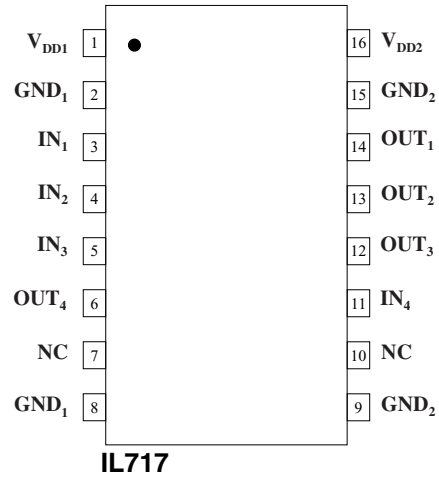
1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub> *
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



\*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

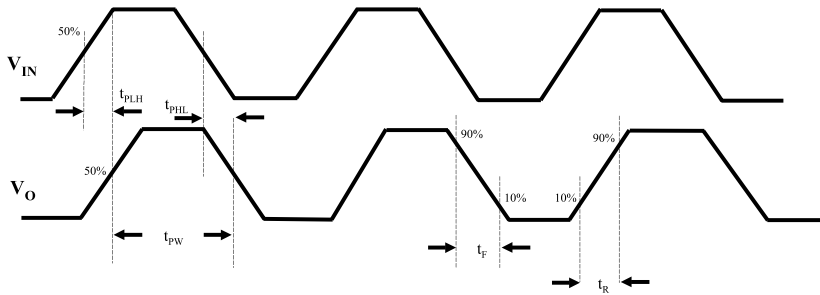
## IL717 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



\*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

## Timing Diagram



### Legend

t <sub>PLH</sub>	Propagation Delay, Low to High
t <sub>PHL</sub>	Propagation Delay, High to Low
t <sub>PW</sub>	Minimum Pulse Width
t <sub>R</sub>	Rise Time
t <sub>F</sub>	Fall Time

3.3 Volt Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current						
IL715 and IL715-3	I <sub>DD1</sub>		16	20	μA	
IL715-1			300	400	μA	
IL716			2.4	3.5	mA	
IL717			1.2	1.75	mA	
Output Quiescent Supply Current						
IL715	I <sub>DD2</sub>		4.8	7	mA	
IL716			2.4	3.5	mA	
IL717			3.6	5.25	mA	
Logic Input Current	I <sub>I</sub>	-10		10	μA	
Logic High Output Voltage	V <sub>OH</sub>	$V_{DD} - 0.1$ $0.8 \times V_{DD}$	$V_{DD}$ $0.9 \times V_{DD}$		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub> I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0 0.5	0.1 0.8	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub> I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>

Switching Specifications (V <sub>DD</sub> = 3.3 V)						
Maximum Data Rate		100	110		Mbps	C <sub>L</sub> = 15 pF
Pulse Width <sup>(7)</sup>	PW	10			ns	50% Points, V <sub>O</sub>
Propagation Delay Input to Output (High to Low)	t <sub>PHL</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)	t <sub>PLH</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion <sup>(2)</sup>	PWD		2	3	ns	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>	t <sub>PSK</sub>		4	6	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%–90%)	t <sub>R</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%–90%)	t <sub>F</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	CM <sub>IH</sub>  ,  CM <sub>IL</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
Channel-to-Channel Skew	t <sub>CSK</sub>		2	3	ns	C <sub>L</sub> = 15 pF
Dynamic Power Consumption <sup>(6)</sup>			140	240	μA/Mbps	per channel

Magnetic Field Immunity <sup>(8)</sup> (V <sub>DD2</sub> = 3V, 3V < V <sub>DD1</sub> < 5.5V)						
Power Frequency Magnetic Immunity	H <sub>PF</sub>	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>	1800	2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	K <sub>X</sub>		2.5			

5 Volt Electrical Specifications ( $T_{min}$ to $T_{max}$ unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current						
IL715 and IL715-3	$I_{DD1}$		24	30	$\mu\text{A}$	
IL715-1			350	500	$\mu\text{A}$	
IL716			3.6	5	$\text{mA}$	
IL717			1.8	2.5	$\text{mA}$	
Output Quiescent Supply Current						
IL715	$I_{DD2}$		7.2	10	$\text{mA}$	
IL716			3.6	5	$\text{mA}$	
IL717			5.4	7.5	$\text{mA}$	
Logic Input Current	$I_I$	-10		10	$\mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD} - 0.1$ $0.8 \times V_{DD}$	$V_{DD}$ $0.9 \times V_{DD}$		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$ $I_O = -4 \text{mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0 0.5	0.1 0.8	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$ $I_O = 4 \text{mA}, V_I = V_{IL}$

Switching Specifications ( $V_{DD} = 5\text{V}$ )						
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{pF}$
Pulse Width <sup>(7)</sup>	PW	10			ns	50% Points, $V_o$
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		10	15	ns	$C_L = 15 \text{pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		10	15	ns	$C_L = 15 \text{pF}$
Pulse Width Distortion <sup>(2)</sup>	PWD		2	3		$C_L = 15 \text{pF}$
Pulse Jitter <sup>(10)</sup>	$t_J$		100		ps	$C_L = 15 \text{pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{pF}$
Output Rise Time (10%–90%)	$t_R$		1	3	ns	$C_L = 15 \text{pF}$
Output Fall Time (10%–90%)	$t_F$		1	3	ns	$C_L = 15 \text{pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H , CM_L$	30	50		$\text{kV}/\mu\text{s}$	$V_{CM} = 1500 V_{DC}$ $t_{TRANSIENT} = 25 \text{ns}$
Channel-to-Channel Skew	$t_{CSK}$		2	3	ns	$C_L = 15 \text{pF}$
Dynamic Power Consumption <sup>(6)</sup>			200	340	$\mu\text{A}/\text{Mbps}$	per channel

Magnetic Field Immunity <sup>(8)</sup> ( $V_{DD2} = 5\text{V}, 3\text{V} < V_{DD1} < 5.5\text{V}$ )						
Power Frequency Magnetic Immunity	$H_{PF}$	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	$H_{PM}$	4000	4500		A/m	$t_p = 8\mu\text{s}$
Damped Oscillatory Magnetic Field	$H_{OSC}$	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	$K_X$		2.5			

**Notes (apply to both 3.3 V and 5 V specifications):**

- Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD is equal to PWD divided by pulse width.
- $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at 25°C.
- $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_o < 0.8 \text{V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
- Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
- Minimum pulse width is the minimum value at which specified PWD is guaranteed.
- The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
- External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 7).
- 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

**Application Information**

**Electrostatic Discharge Sensitivity**

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

**Electromagnetic Compatibility**

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

**EN50081-1**

Residential, Commercial & Light Industrial  
Methods EN55022, EN55014

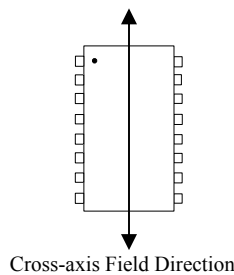
**EN50082-2: Industrial Environment**

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

**ENV50204**

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



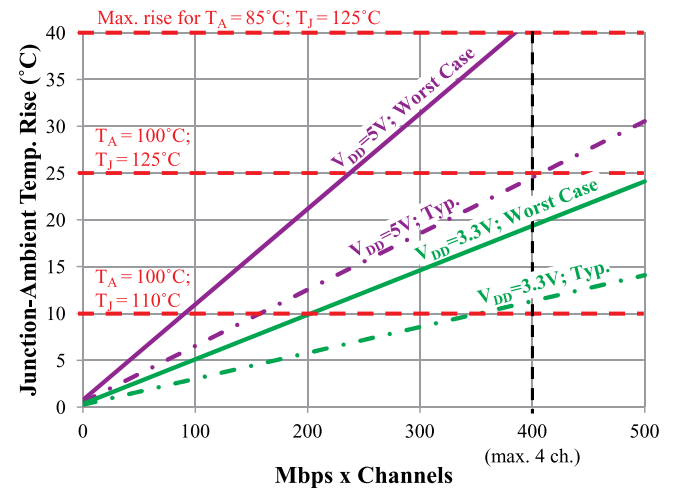
**Dynamic Power Consumption**

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

**Thermal Management**

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:



Standard-grade parts have a maximum junction temperature of 110°C. T-Series parts have a maximum operating junction temperature of 125°C for additional margin at extreme operating conditions.

**Power Supply Decoupling**

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND<sub>1</sub> and GND<sub>2</sub> are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V<sub>DD</sub> pins.

**Maintaining Creepage**

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

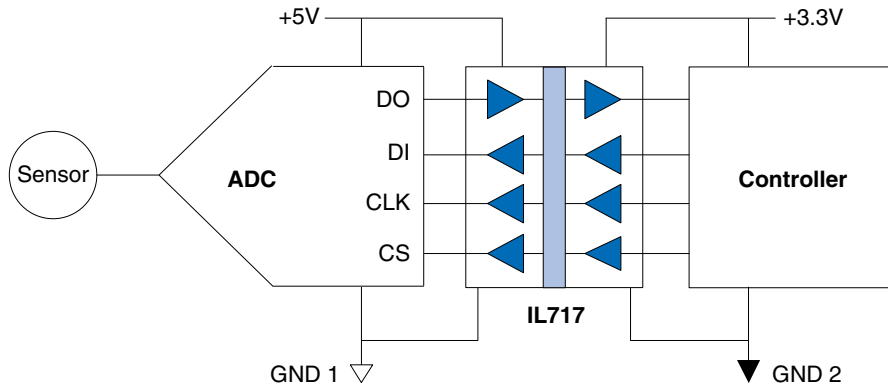
**Signal Status on Start-up and Shut Down**

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

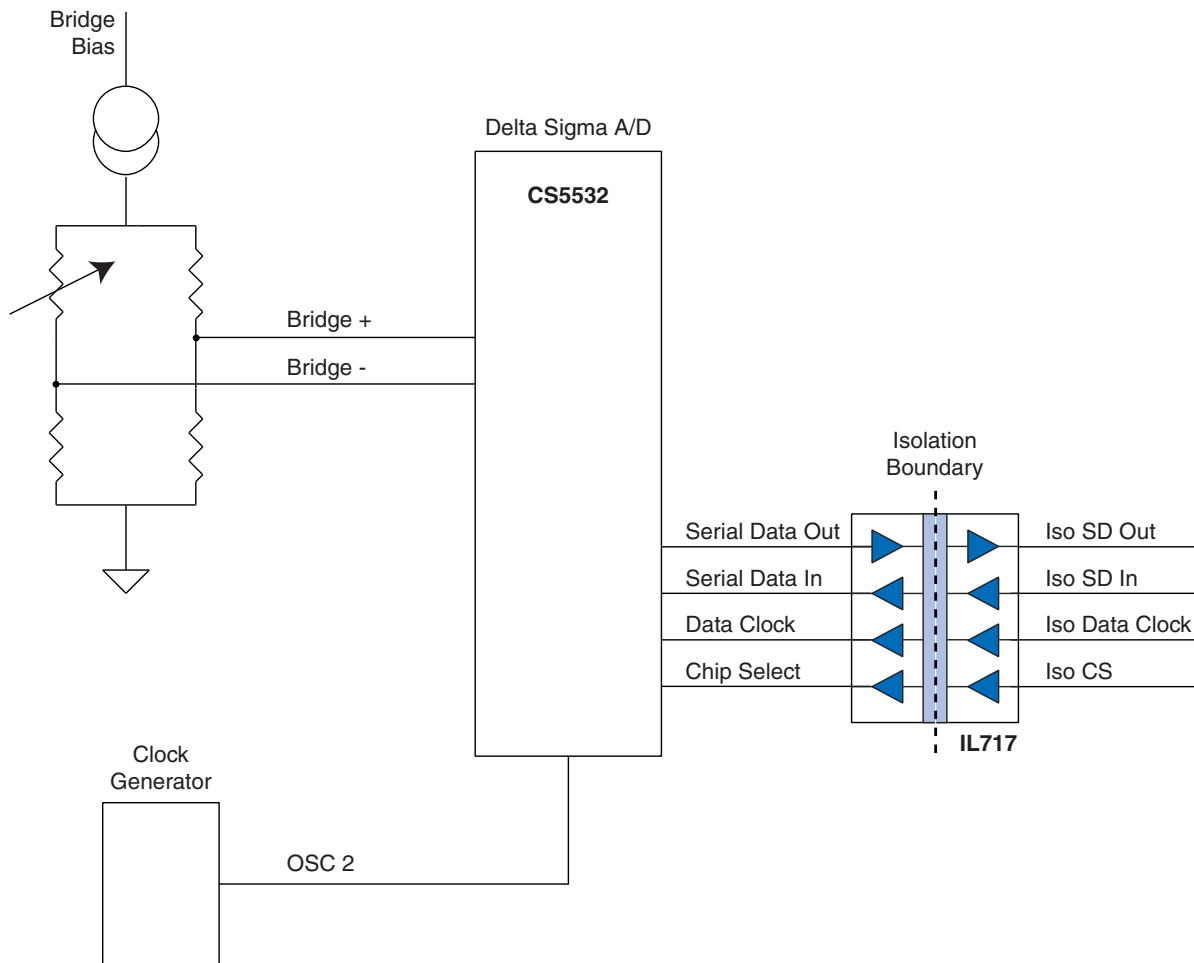


**Application Diagrams**

**Isolated Logic Level Shifters**



**Single-Channel Isolated Delta-Sigma A/D Converter**

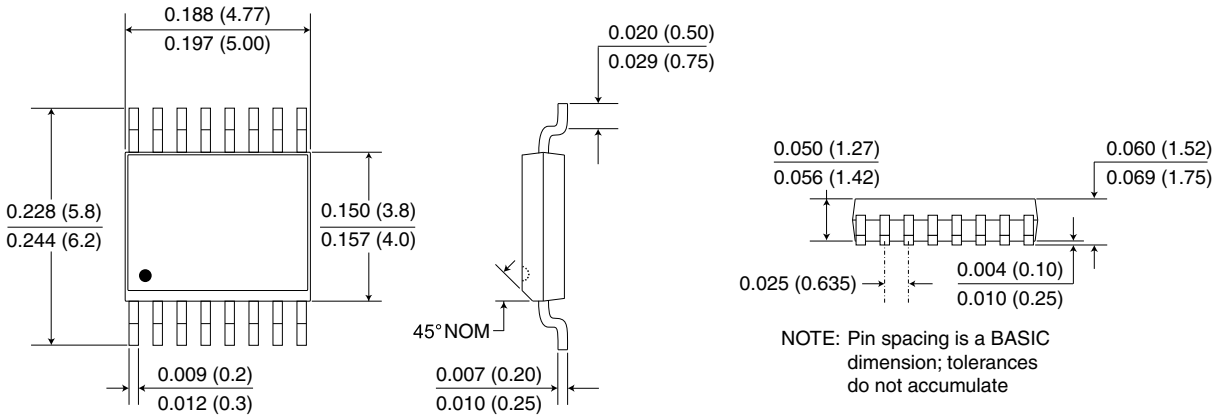


This circuit illustrates a typical single-channel delta-sigma ADC. The A/D is located on the bridge with no signal conditioning electronics between the bridge sensor and the ADC. In this case, the IL717 is the best choice for isolation. It isolates the control bus from the microcontroller. The system clock is located on the isolated side of the system.

**Package Drawings**

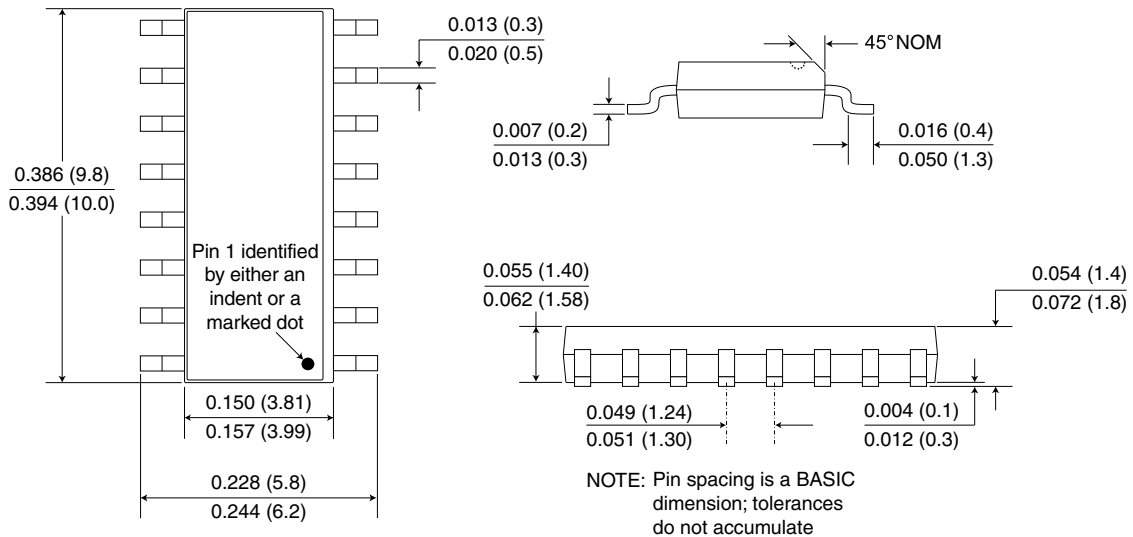
**Ultraminiature 16-pin QSOP Package (-1 suffix)**

Dimensions in inches (mm); scale = approx. 5X



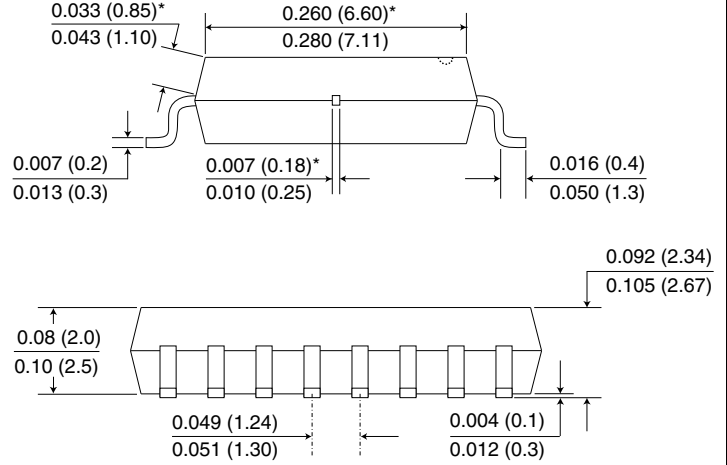
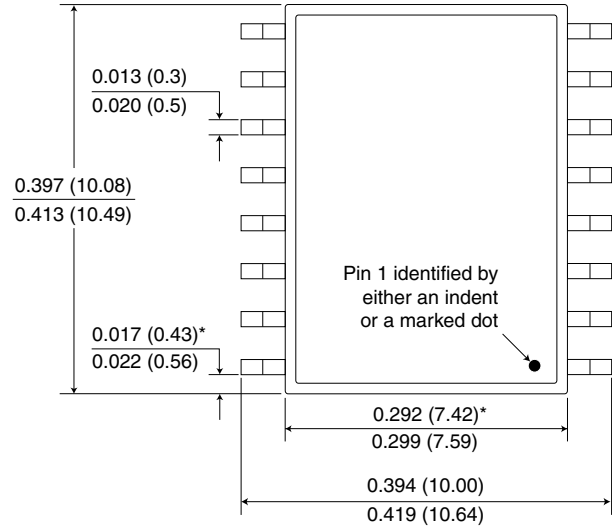
**0.15" 16-pin SOIC Package (-3 suffix)**

Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Package (no suffix)**

Dimensions in inches (mm); scale = approx. 5X



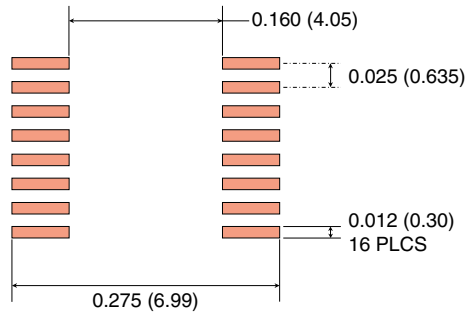
NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

**Recommended Pad Layouts**

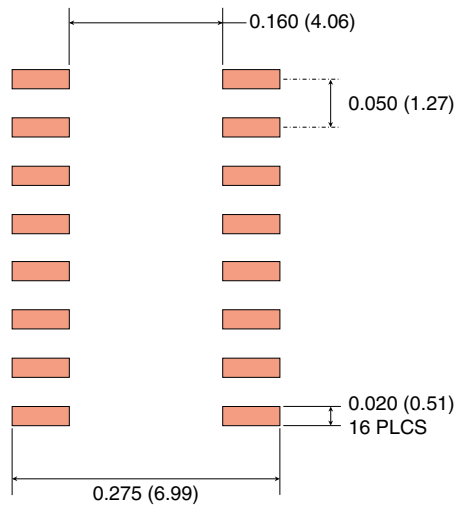
**4 mm x 5 mm 16-pin QSOP Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



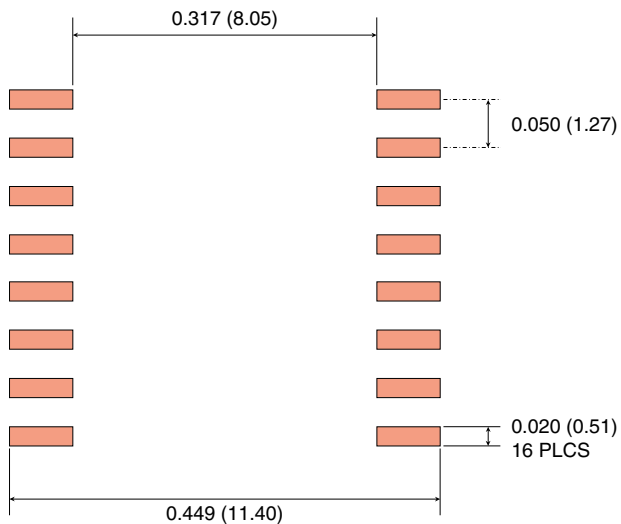
**0.15" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



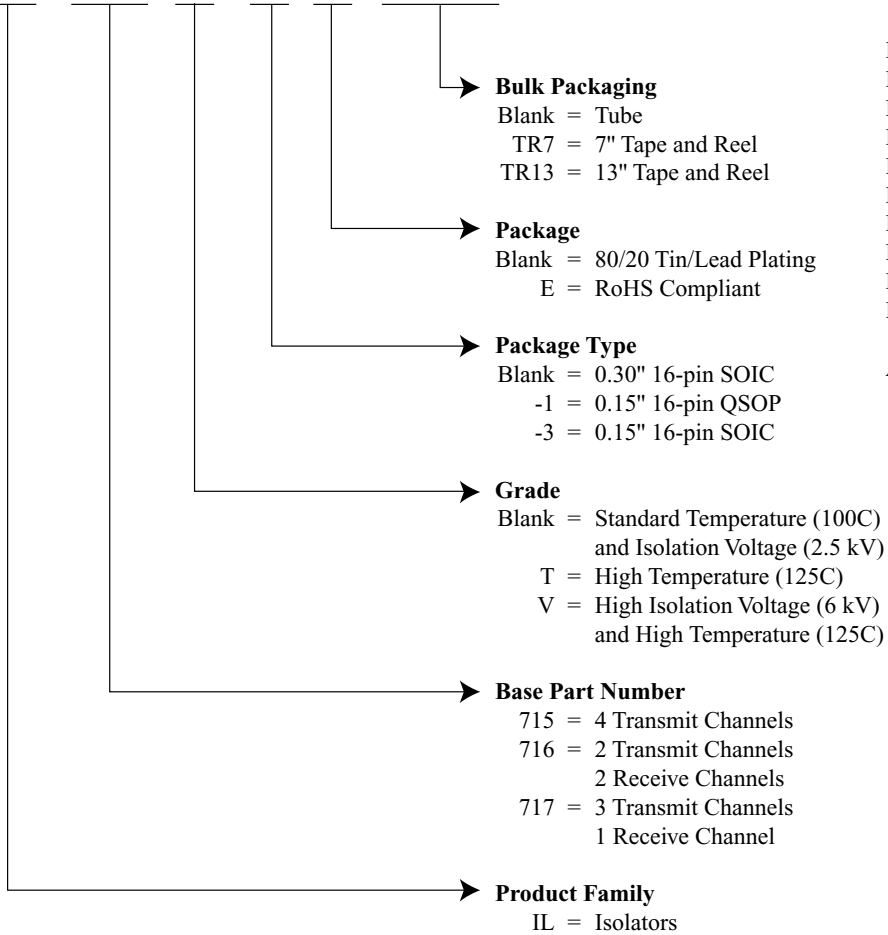
**Ordering Information**

**IL 716 T - 3 E TR13**

**Valid Part Numbers**

IL715	IL716	IL717
IL715E	IL716E	IL717E
IL715-1E	IL716-1E	IL716-1E
IL715-3	IL716-3	IL717-3
IL715-3E	IL716-3E	IL717-3E
IL715T	IL716T	IL717T
IL715TE	IL716TE	IL717TE
IL715T-3	IL716T-3	IL717T-3
IL715T-3E	IL716T-3E	IL717T-3E
IL715VE	IL716VE	IL717VE

All part types are available on tape and reel.



## Available Parts

Available Parts	Transmit Channels	Receive Channels	Maximum Temperature	Isolation Voltage (RMS)	Package	RoHS
IL715-1E	4	0	100°C	2.5 kV	QSOP	Y
IL715-3	4	0	100°C	2.5 kV	Narrow SOIC	N
IL715-3E	4	0	100°C	2.5 kV	Narrow SOIC	Y
IL715	4	0	100°C	2.5 kV	Wide SOIC	N
IL715E	4	0	100°C	2.5 kV	Wide SOIC	Y
IL715T-3	4	0	125°C	2.5 kV	Narrow SOIC	N
IL715T-3E	4	0	125°C	2.5 kV	Narrow SOIC	Y
IL715T	4	0	125°C	2.5 kV	Wide SOIC	Y
IL715TE	4	0	125°C	2.5 kV	Wide SOIC	N
IL715VE	4	0	125°C	6 kV	Wide SOIC	Y
IL716-1E	2	2	100°C	2.5 kV	QSOP	N
IL716-3	2	2	100°C	2.5 kV	Narrow SOIC	N
IL716-3E	2	2	100°C	2.5 kV	Narrow SOIC	Y
IL716	2	2	100°C	2.5 kV	Wide SOIC	N
IL716E	2	2	100°C	2.5 kV	Wide SOIC	Y
IL716T-3	2	2	125°C	2.5 kV	Narrow SOIC	N
IL716T-3E	2	2	125°C	2.5 kV	Narrow SOIC	Y
IL716T	2	2	125°C	2.5 kV	Wide SOIC	N
IL716TE	2	2	125°C	2.5 kV	Wide SOIC	Y
IL716VE	2	2	125°C	6 kV	Wide SOIC	Y
IL717-1E	3	1	100°C	2.5 kV	QSOP	Y
IL717-3	3	1	100°C	2.5 kV	Narrow SOIC	N
IL717-3E	3	1	100°C	2.5 kV	Narrow SOIC	Y
IL717	3	1	100°C	2.5 kV	Wide SOIC	N
IL717E	3	1	100°C	2.5 kV	Wide SOIC	Y
IL717T-3	3	1	125°C	2.5 kV	Narrow SOIC	N
IL717T-3E	3	1	125°C	2.5 kV	Narrow SOIC	Y
IL717T	3	1	125°C	2.5 kV	Wide SOIC	N
IL717TE	3	1	125°C	2.5 kV	Wide SOIC	Y
IL717VE	3	1	125°C	6 kV	Wide SOIC	Y

All part types are available on tape and reel.

**ISB-DS-001-IL715/6/7-AE**  
**November 2016**

**Changes**

- Updated VDE Reinforced Isolation file number and description.

**ISB-DS-001-IL715/6/7-AD**

**Changes**

- Clarified 600 V CTI specification is for 0.3" SOIC only (p. 2).
- Corrected typographical error in “Available Parts” table (p. 15).

**ISB-DS-001-IL715/6/7-AC**

**Changes**

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded “V” Version Surge Immunity specification to 12.8 kV.
- Upgraded “V” Version VDE 0884-10 rating to reinforced insulation.
- Corrected QSOP pin width dimension (p. 10).

**ISB-DS-001-IL715/6/7-AB**

**Changes**

- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to  $\geq 600$  Vrms.

**ISB-DS-001-IL715/6/7-AA**

**Changes**

- Added V-Series 5 kV isolation voltage versions.
- More detailed “Available Parts” table.

**ISB-DS-001-IL715/6/7-Z**

**Changes**

- Added package illustrations on first page.
- Added QSOP packages (-1 suffix).
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).
- Added “Thermal Management” paragraph in Applications section.

**ISB-DS-001-IL715/6/7-Y**

**Changes**

- IEC 60747-5-5 (VDE 0884) certification.

**ISB-DS-001-IL715/6/7-X**

**Changes**

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

**ISB-DS-001-IL715/6/7-W**

**Changes**

- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added high voltage endurance specification.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

**ISB-DS-001-IL715/6/7-V**

**Changes**

- Detailed isolation and barrier specifications.
- Cosmetic changes.

**ISB-DS-001-IL715/6/7-U**

**Changes**

- Tightened typical output quiescent supply spec. to 1.5 mA/channel at 3.3V.



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ISB-DS-001-IL715/6/7-AE

*November 2016*

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