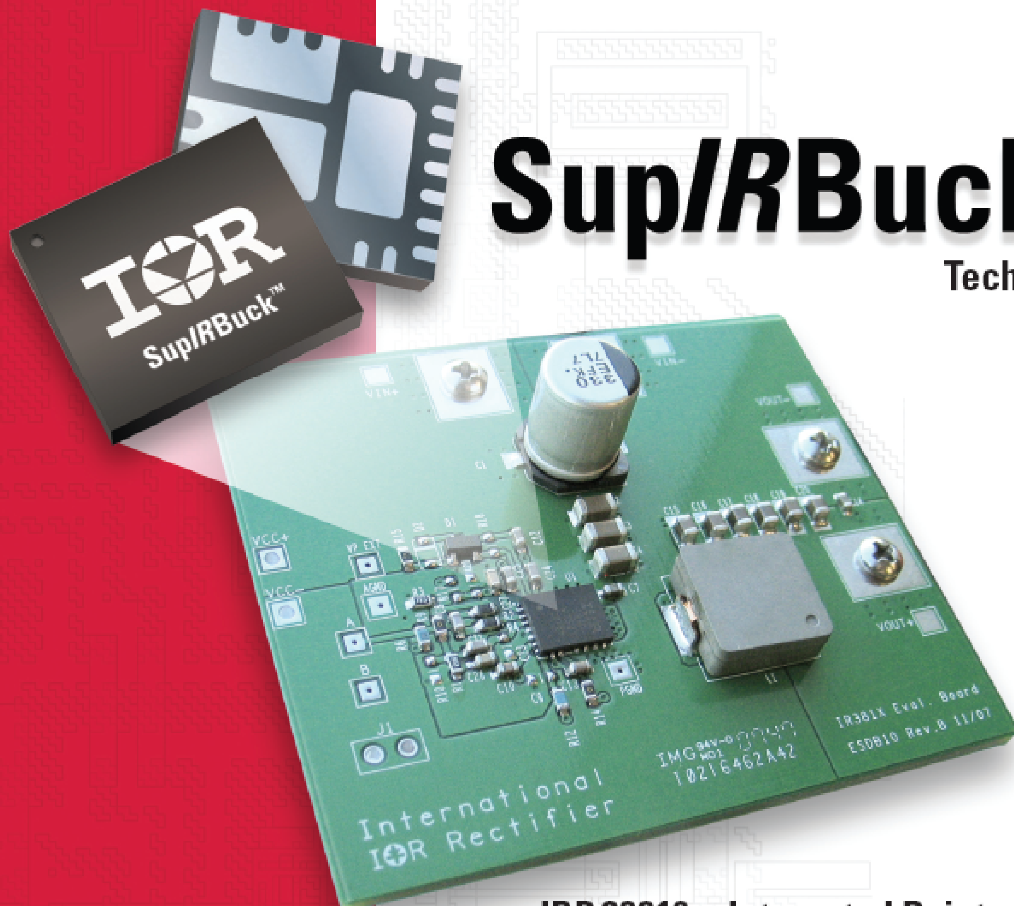
AC-DC | AUDIO | AUTOMOTIVE | LIGHTING | HI-REL | DC-DC | MOTION CONTROL



SupIRBuck™

Technology

IRDC3810 – Integrated Point of Load DC-DC Voltage Regulator

Featuring IR3810 Voltage Regulator

Programmable Soft Start; DDR Memory Tracking; Programmable Over Current Protection; Pre-Bias Start Up

600kHz Switching Frequency

$12V_{IN}$ to $0.75V_{OUT}$ @ 12A

International Rectifier

SupIRBuck™

USER GUIDE FOR IR3810 EVALUATION BOARD

DESCRIPTION

The IR3810 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3810 include, tracking capability for memory application, programmable soft-start ramp, precision 0.6V reference voltage, thermal protection, fixed 600kHz switching frequency requiring no external component, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3810 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3810 is available in the IR3810 data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- Tracking Input
- V_{out} = 0.75V @ 0- 12A V_p:0.6V
- L= 0.36uH
- C_{in}= 3x10uF (ceramic 1206) + 330uF (electrolytic)
- C_{out}= 6x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-.   A maximum 12A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3810 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). These inputs are connected on the board with a zero ohm resistor (R15). Separate supplies can be applied to these inputs. *Vcc input cannot be connected unless R15 is removed.* Vcc input should be a well regulated 5V-12V supply and it would be connected to Vcc+ and Vcc-.

Vp pin is connected to the internal reference (Vref) via R14 as the default configuration. External input can be applied to Vp. *For tacking applications, R14 should be removed, R17 should be inserted, and the external tracking source should be applied between Vp_Ext and Agnd.* The value of R17 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. *For proper operation of IR3810, the voltage at Vp pin should be kept between 0.2V to 1.0V and it should be applied whenever the voltage at Soft-Start pin is greater than 1V.*

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Optional Vcc input
Vcc-	Ground for optional Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out}
Vp_Ext	Optional Tracking input
Agnd	Analog (Signal) Ground

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3810 SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the charge-pump capacitor and feedback components are located close to IR3810. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck.

To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

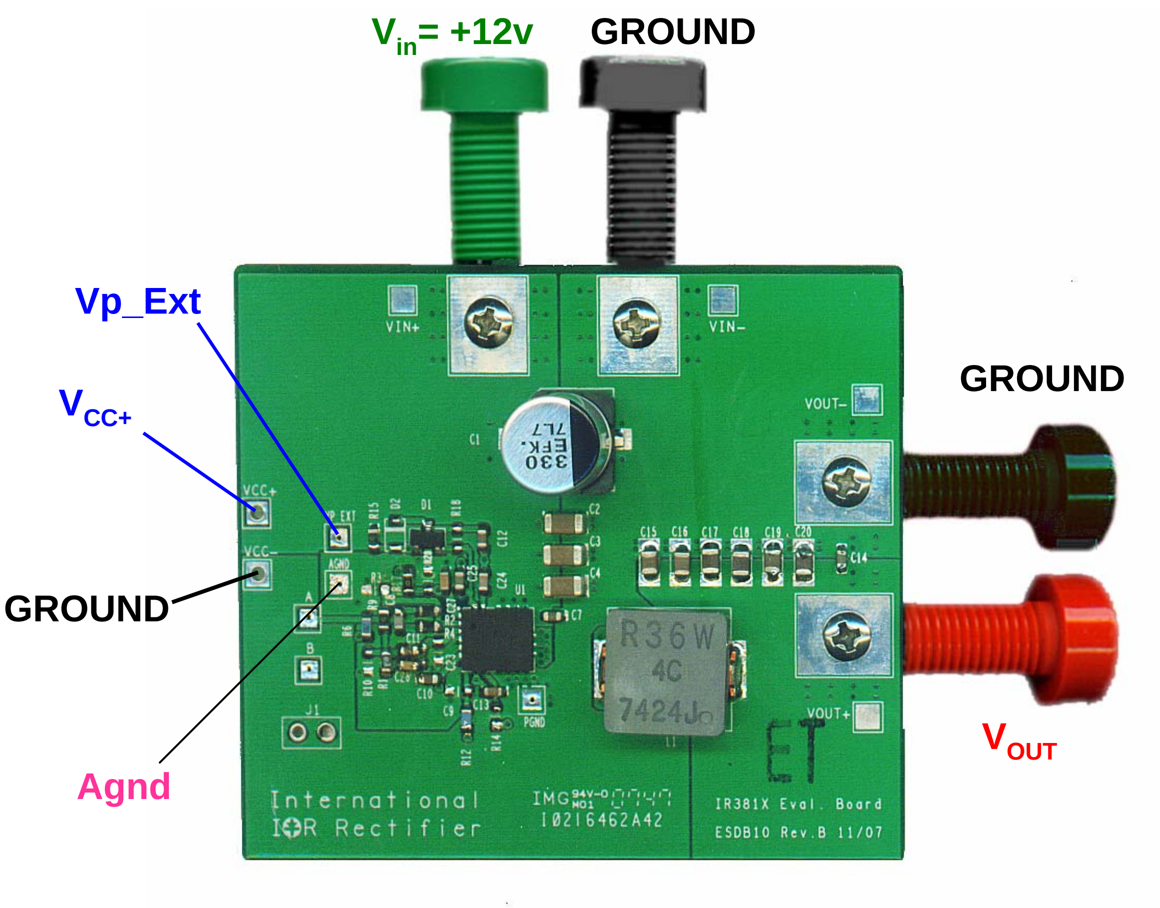


Fig. 1: Connection diagram of IR3810 evaluation board

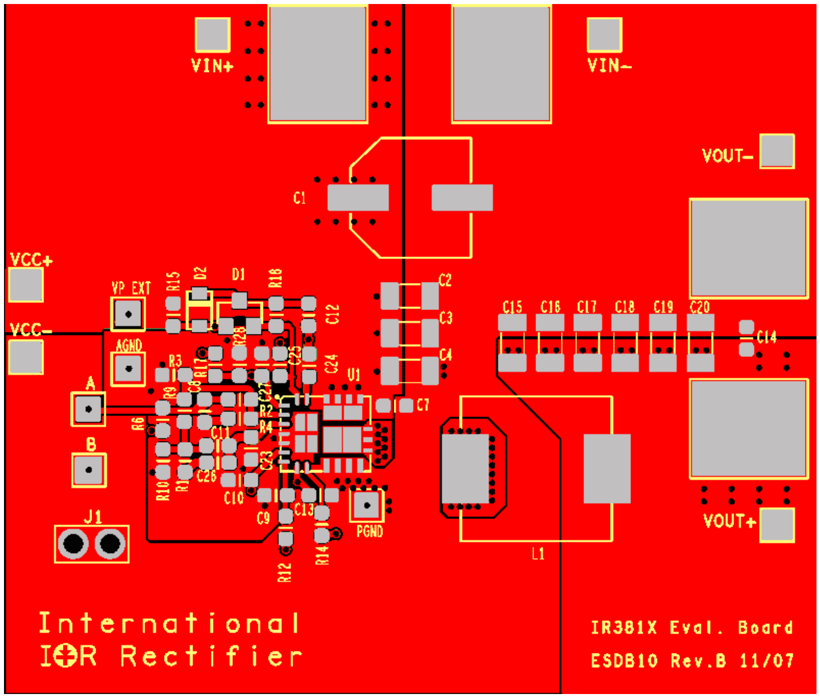


Fig. 2: Board layout, top overlay

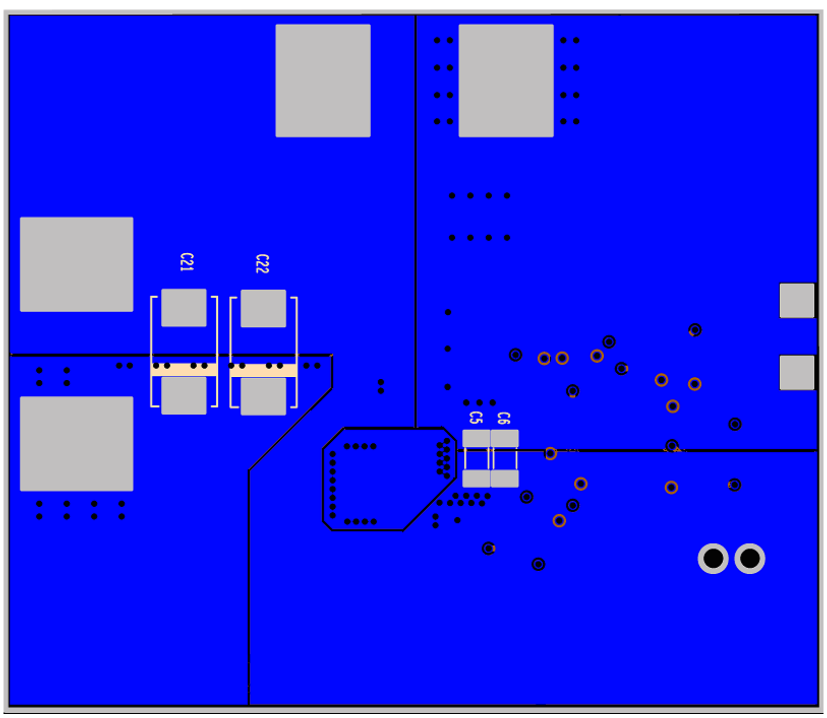


Fig. 3: Board layout, bottom overlay (rear view)

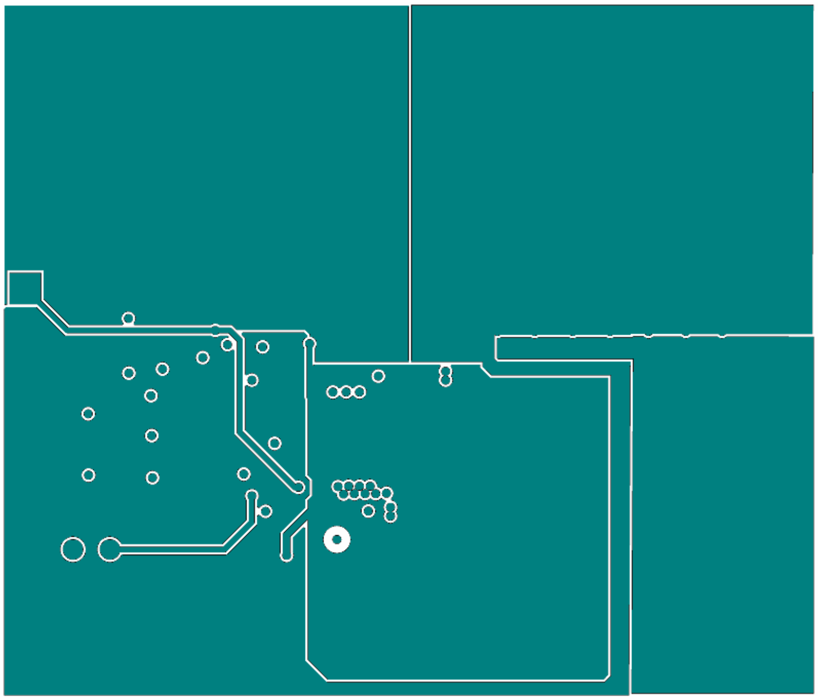


Fig. 4: Board layout, mid-layer I

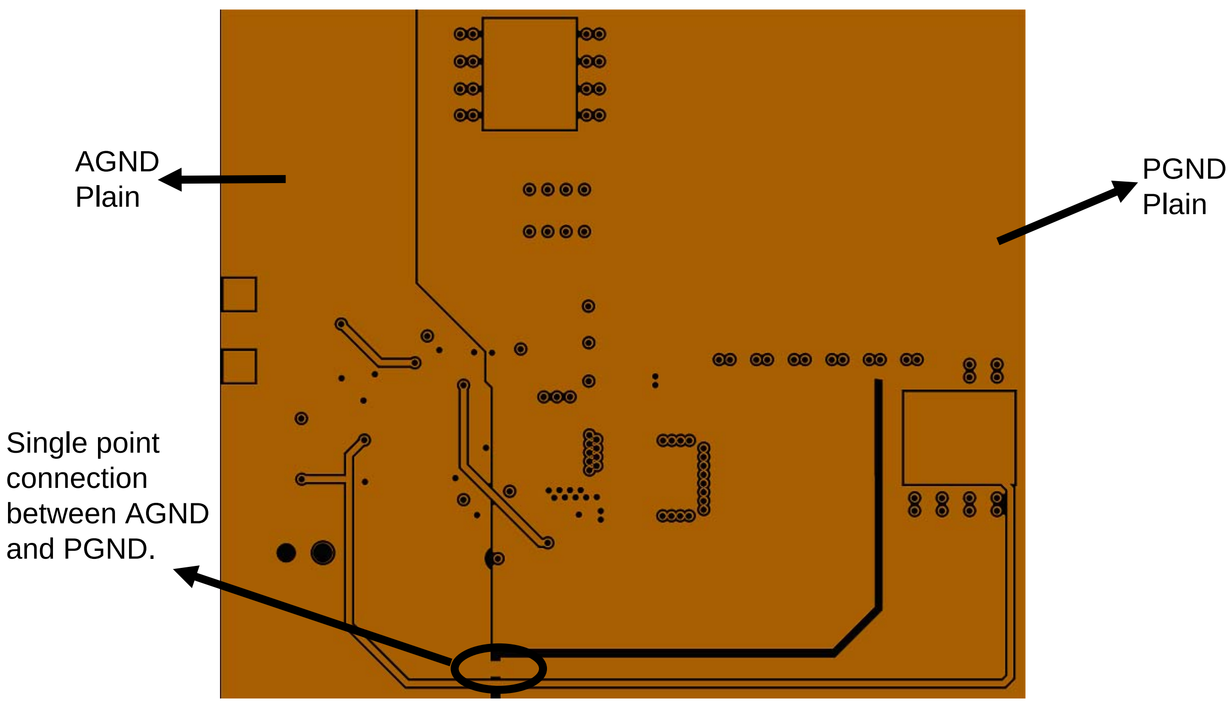


Fig. 5: Board layout, mid-layer II

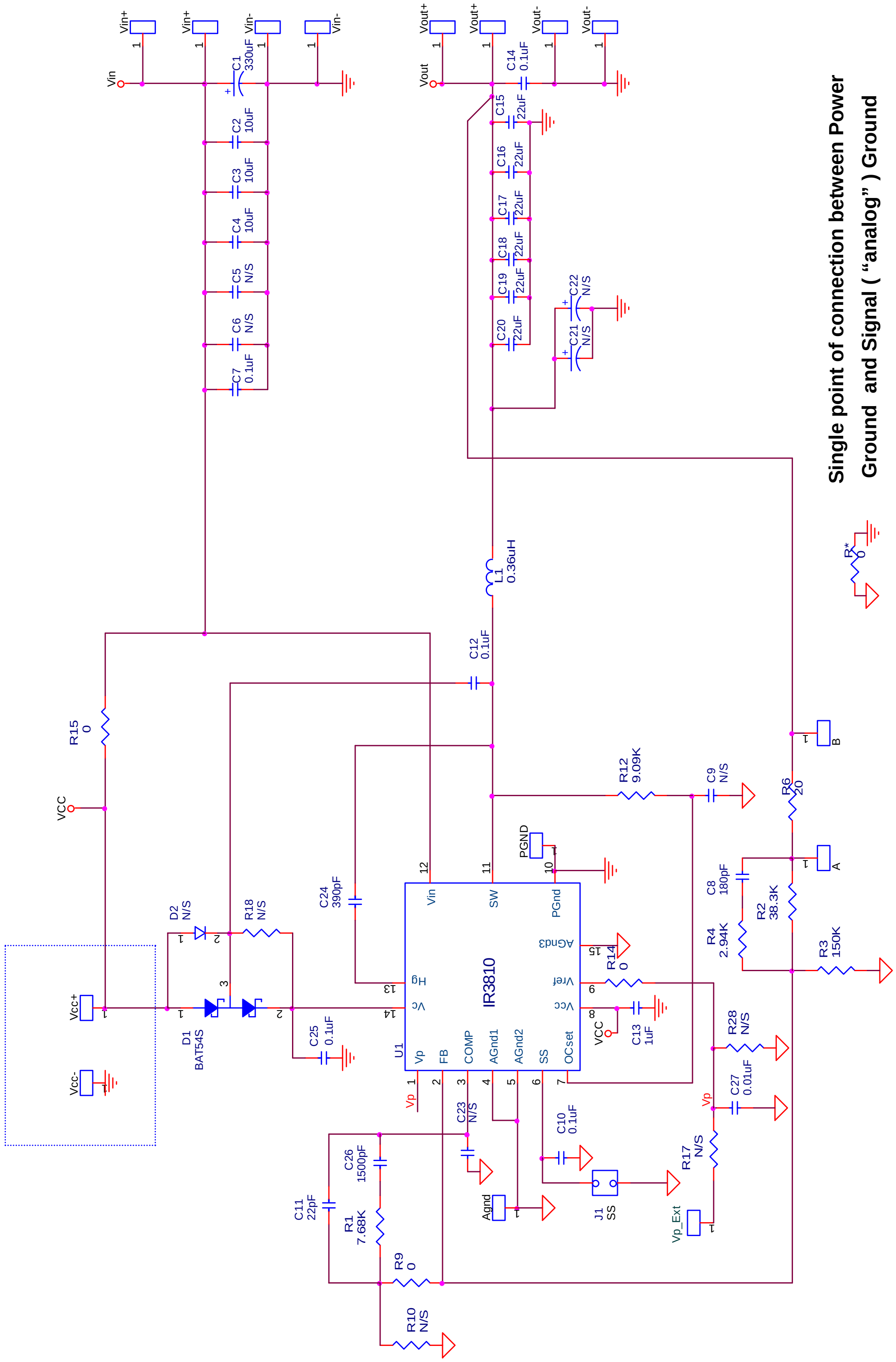


Fig. 6: Schematic of the IR3810 evaluation board

Bill of Materials

Item	Quantity	Designator	Value	Description	Size	Manufacturer	Mfr. Part Number
1	1	C1	330uF	SMD Electrolytic, 25V, 20%	SMD	Panasonic	EEV-FK1E331P
2	3	C2 C3 C4	10uF	Ceramic, 16V, X7R, 10%	1206	Panasonic	ECJ-3YX1C106K
3	5	C7 C10 C12 C14 C25	0.1uF	Ceramic, 50V, X7R, 10%	0603	Panasonic	ECJ-1VB1H104K
4	1	C27	0.01uF	Ceramic, 16V, X7R, 10%	0603	Panasonic	ECJ-1VB1C103K
5	1	C8	180pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H181JA01
6	1	C11	22pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H220JA01
7	1	C13	1uF	Ceramic, 16V, X5R, 10%	0603	Panasonic	ECJ-1VB1C105K
8	6	C15 C16 C17 C18 C19 C20	22uF	Ceramic, 6.3V, X5R, 20%	0805	Panasonic	ECJ-2FB0J226M
9	1	C24	390pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H391JA01
10	1	C26	1500pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H152JA01
11	1	D1	BAT54S	Diode Schottky ,40V, 200mA	SOT-23	Fairchild	BAT54S
12	1	L1	0.36uH	SMT Inductor, 1.1mOhm, 20%	11.5x 10mm	Panasonic	ETQP4LR36WFC
13	1	R1	7.68K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06037K68FKEA
14	1	R3	150K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW0603150KFKEA
15	1	R2	38.3K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060338K3FKEA
16	1	R4	2.94K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06032K94FKEA
17	1	R6	20	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060320R0FKEA
18	3	R9 R14 R15	0	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06030000Z0EA
19	1	R12	9.09K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06039K09FKEA
20	1	U1	IR3810	600kHz, 12A, SupIRBuck Module	5x6mm	International Rectifier	IR3810
21	2	-	-	Banana Jack, Insulated Solder Terminal, Black	-	Johnson Components	105-0853-001
22	1	-	-	Banana Jack- Insulated Solder Terminal, Red	-	Johnson Components	105-0852-001
23	1	-	-	Banana Jack- Insulated Solder Terminal, Green	-	Johnson Components	105-0854-001

TYPICAL OPERATING WAVEFORMS

Vin=Vcc=12.0V, Vp=0- 0.6V, Vo=0.75V, Io=0- 12A, Room Temperature, No Air Flow

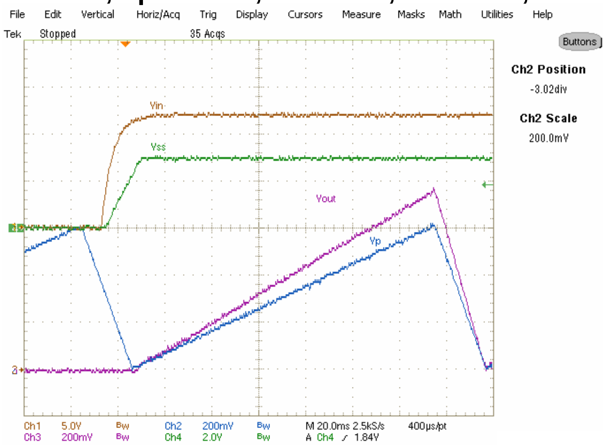


Fig. 7: Start up at 12A Load
Ch_1:V_{in}, Ch_2:V_p, Ch_3:V_{out}, Ch_4:V_{ss}

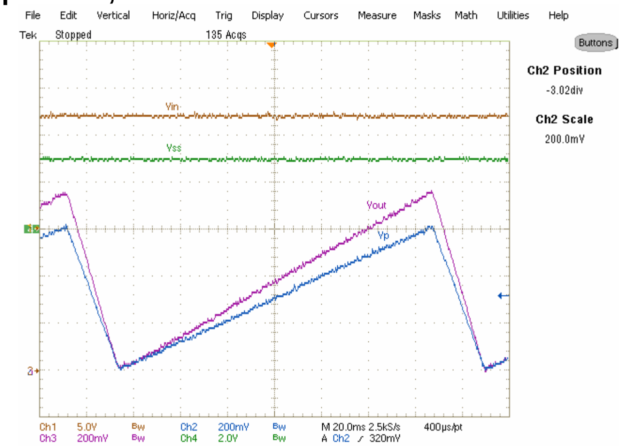


Fig. 8: Tracking Operation V_p: 0- 0.6V , 12A Load
Ch_1:V_{in}, Ch_2:V_p, Ch_3:V_{out}, Ch_4:V_{ss}

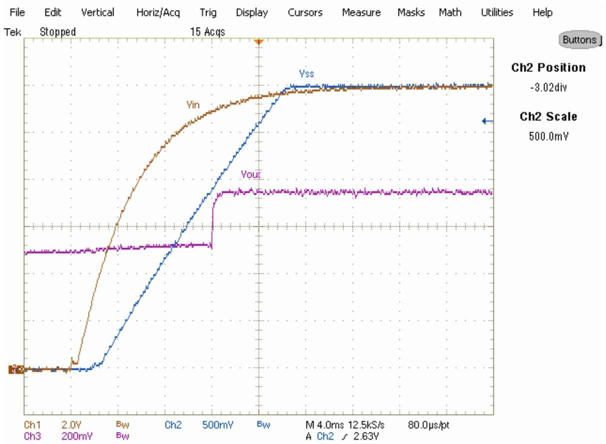


Fig. 9: Start up with 0.5V PreBias, V_p:0.6V, 0A Load, Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}

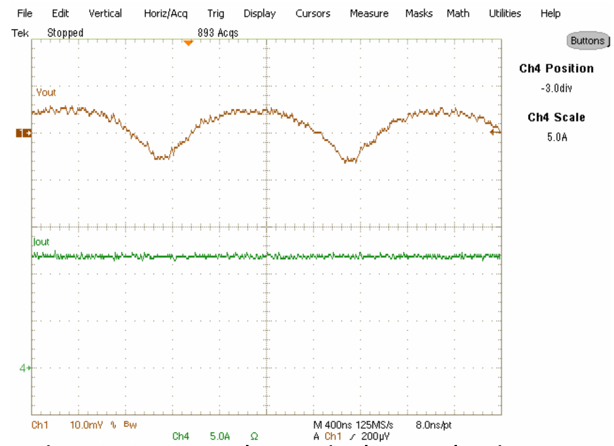


Fig. 10: Output Voltage Ripple, 12A load, V_p:0.6V, Ch_1: V_{out} , Ch_4: I_{out}

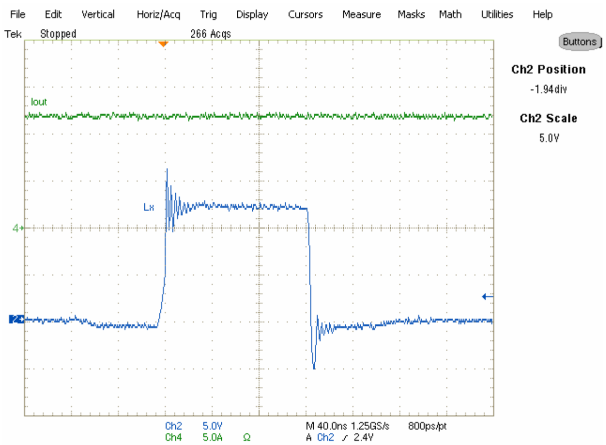


Fig. 11: Inductor node at 12A load, V_p:0.6V, Ch_2:LX, Ch_4:I_{out}

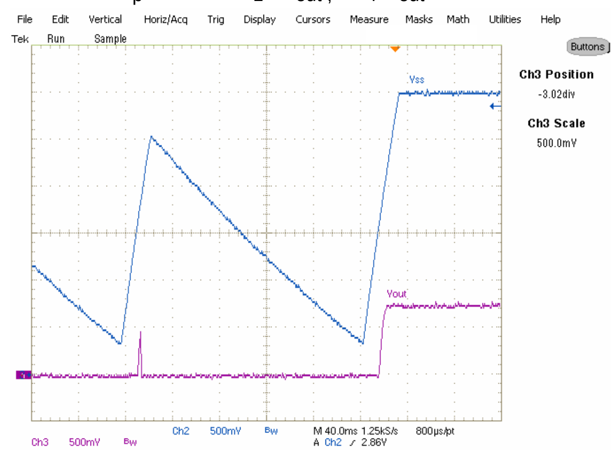


Fig. 12: Short (Hiccup) Recovery, V_p:0.6V
Ch_2:V_{SS} , Ch_3:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin=Vcc=12V, Vo=0.75V, Io=6A-12A, Room Temperature, No Air Flow

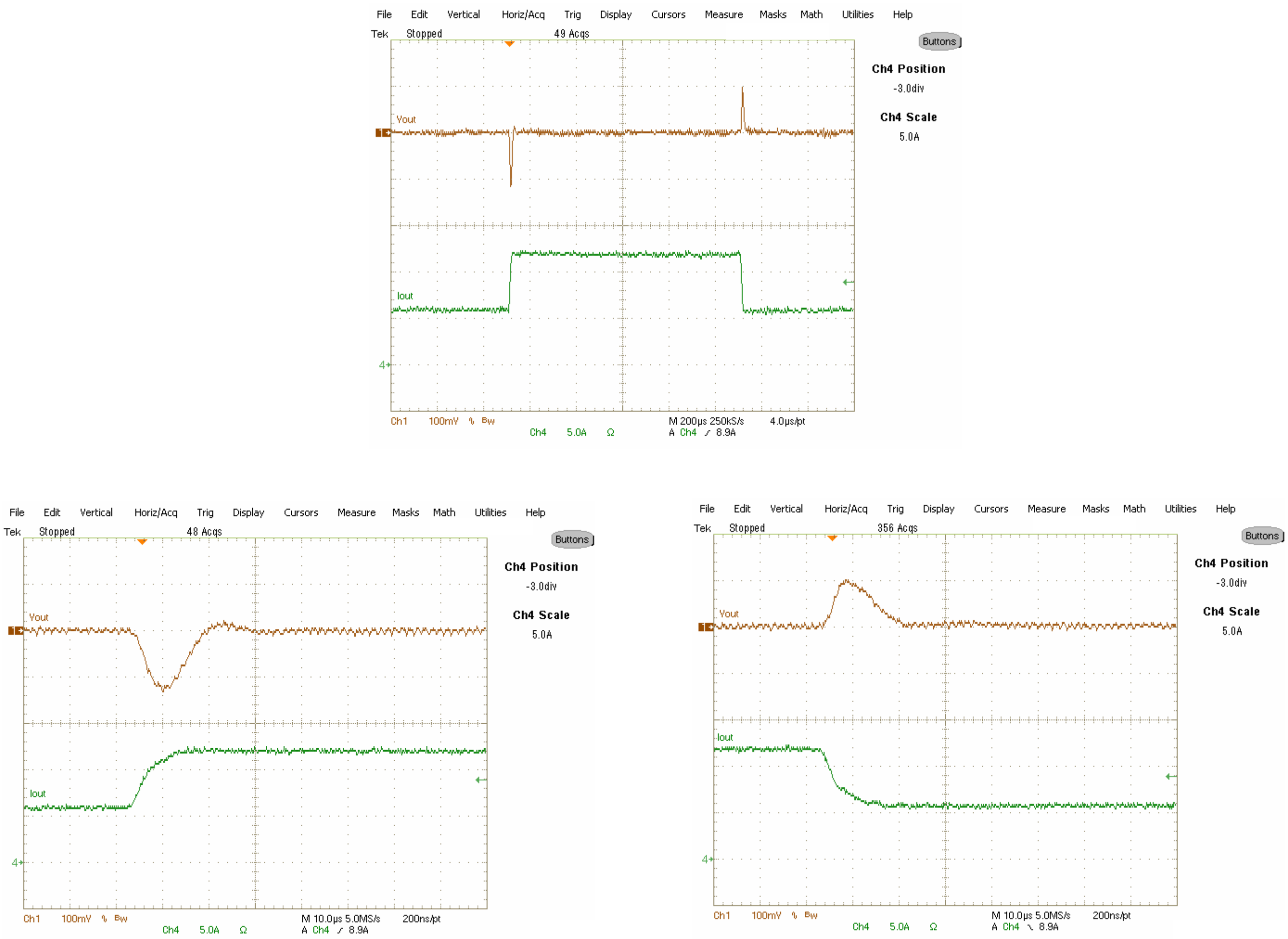


Fig. 13: Transient Response, 6A to 12A step

Ch_3:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=Vcc=12V, Vo=0.75V, Io=12A, Room Temperature, No Air Flow

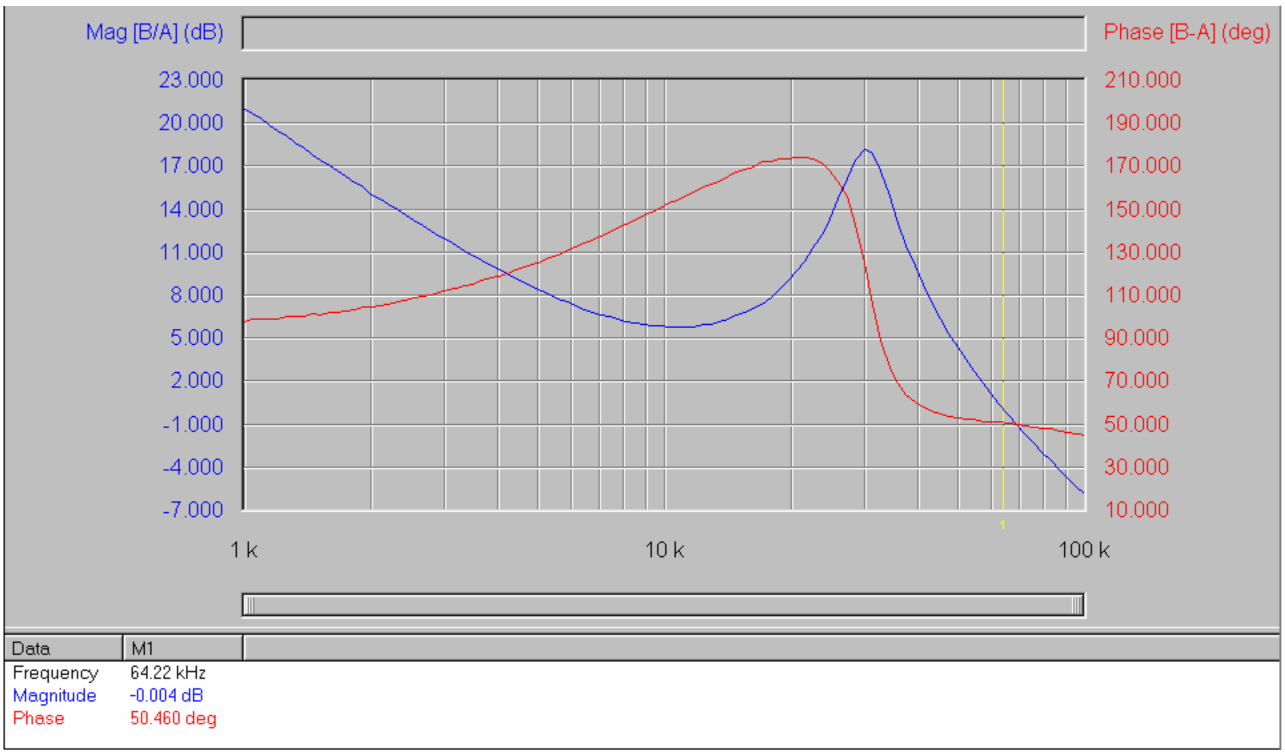


Fig. 14: Bode Plot at 12A load shows a bandwidth of 64.2kHz and phase margin of 50.5 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=0.75V, Io=0- 12A, Room Temperature, No Air Flow

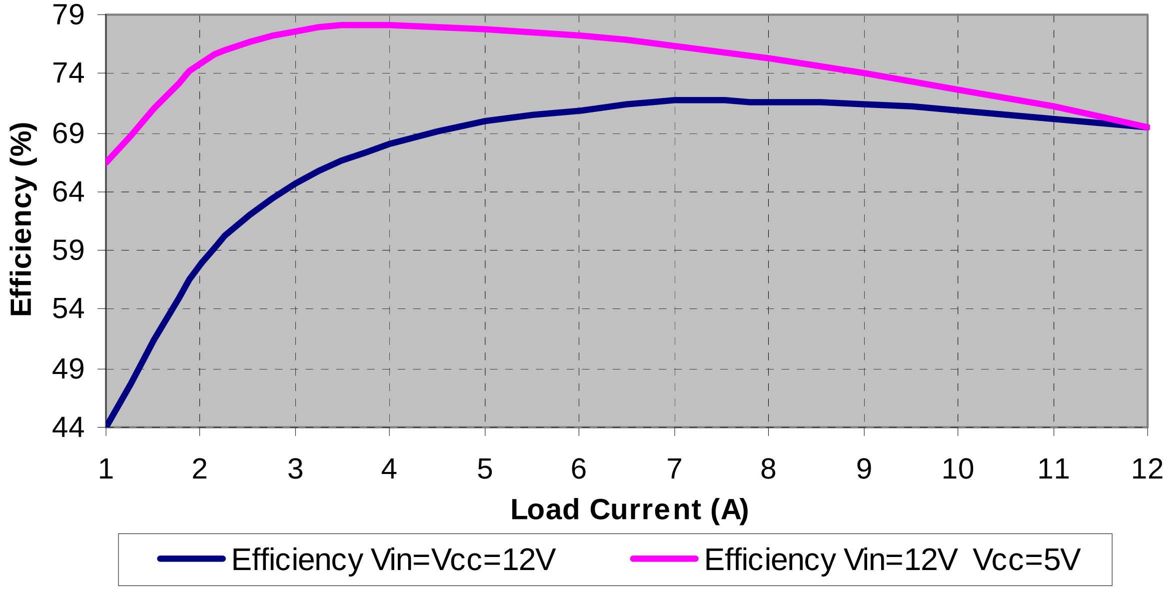


Fig.15: Efficiency versus load current

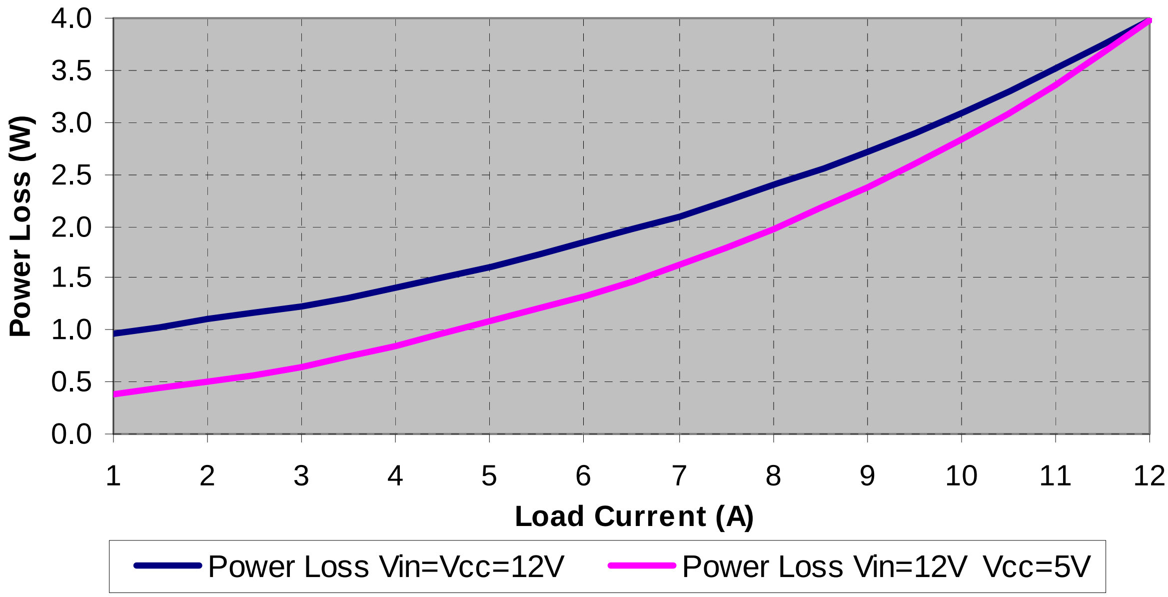


Fig.16: Power loss versus load current

THERMAL IMAGES
Vin=Vcc=12V, Vo=0.75V, Io=12A, Room Temperature, 200LFM

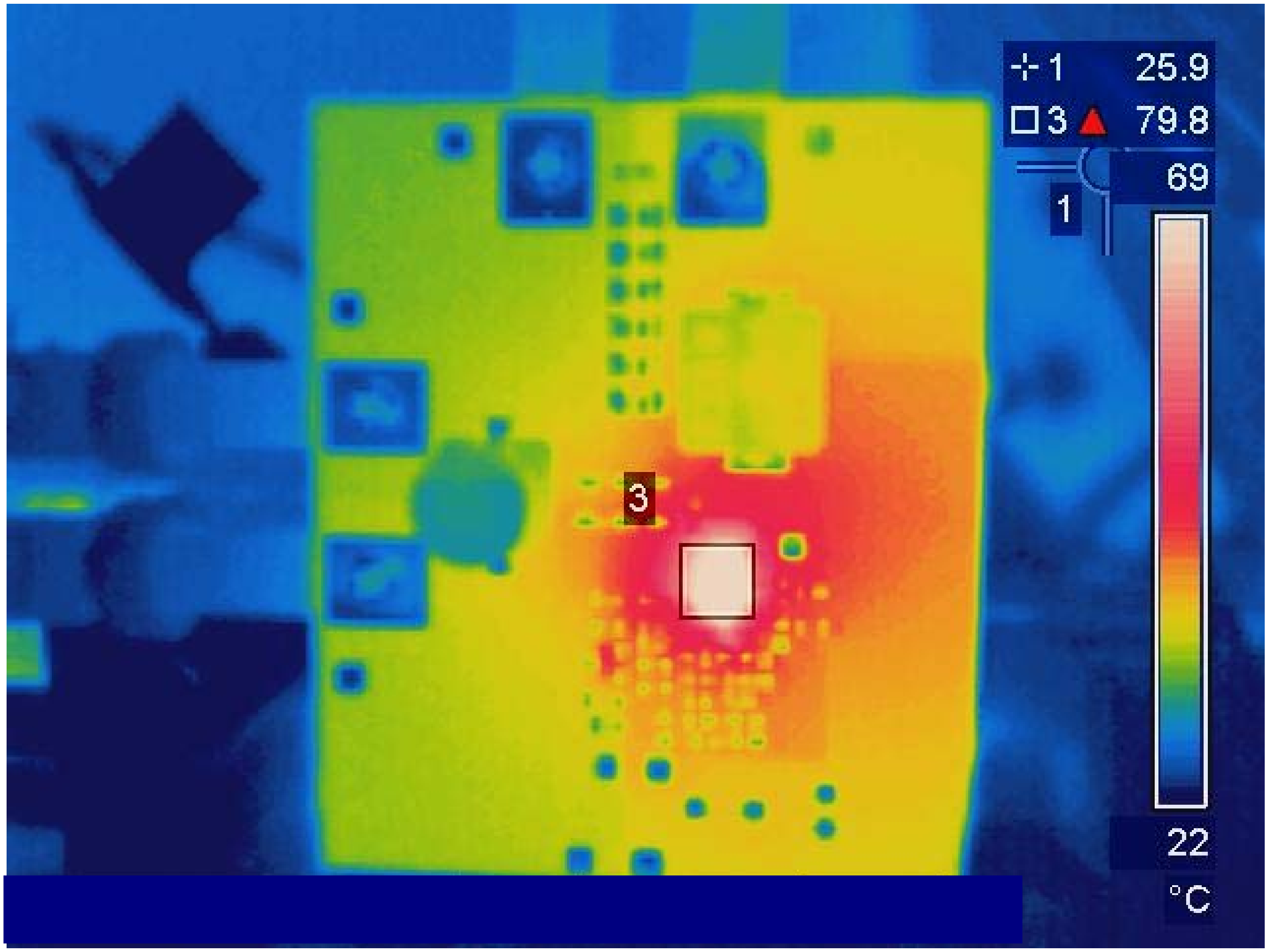


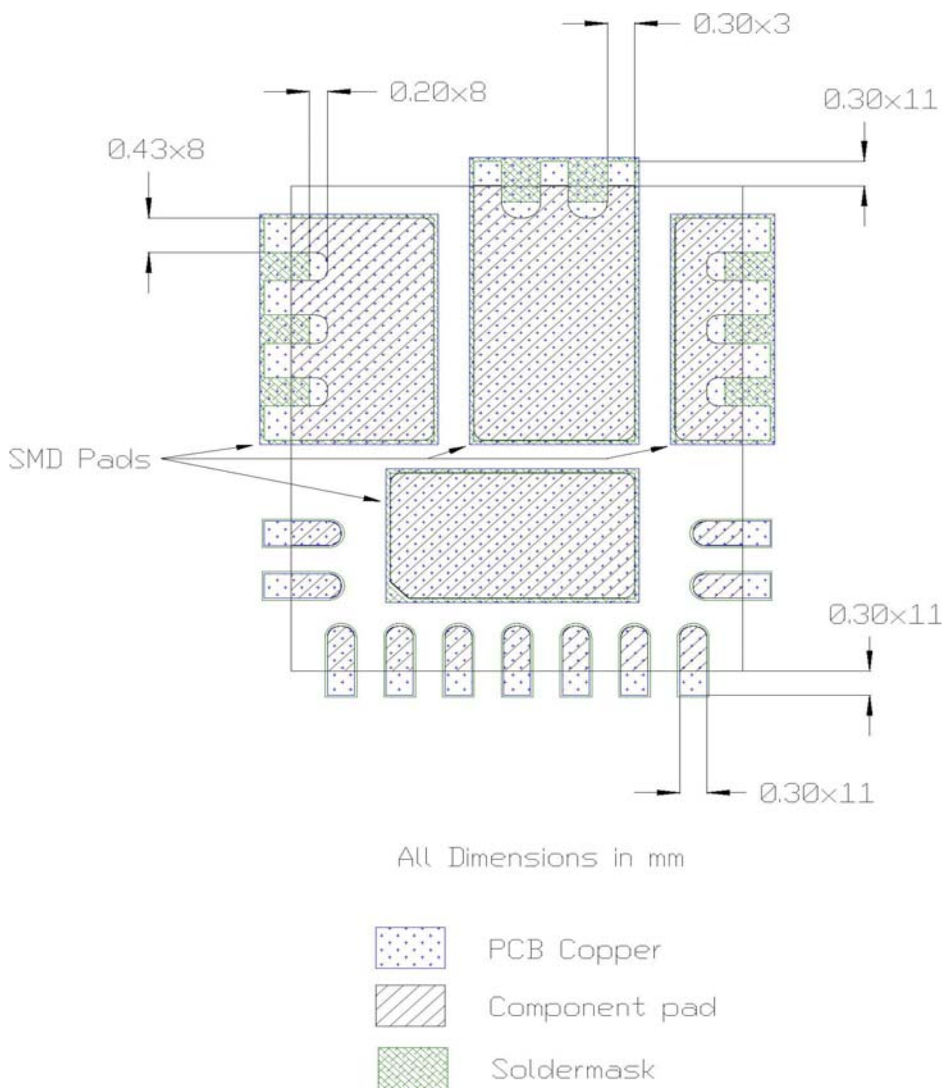
Fig. 17: Thermal Image at 12A load
Test point 1 is the IR3810

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

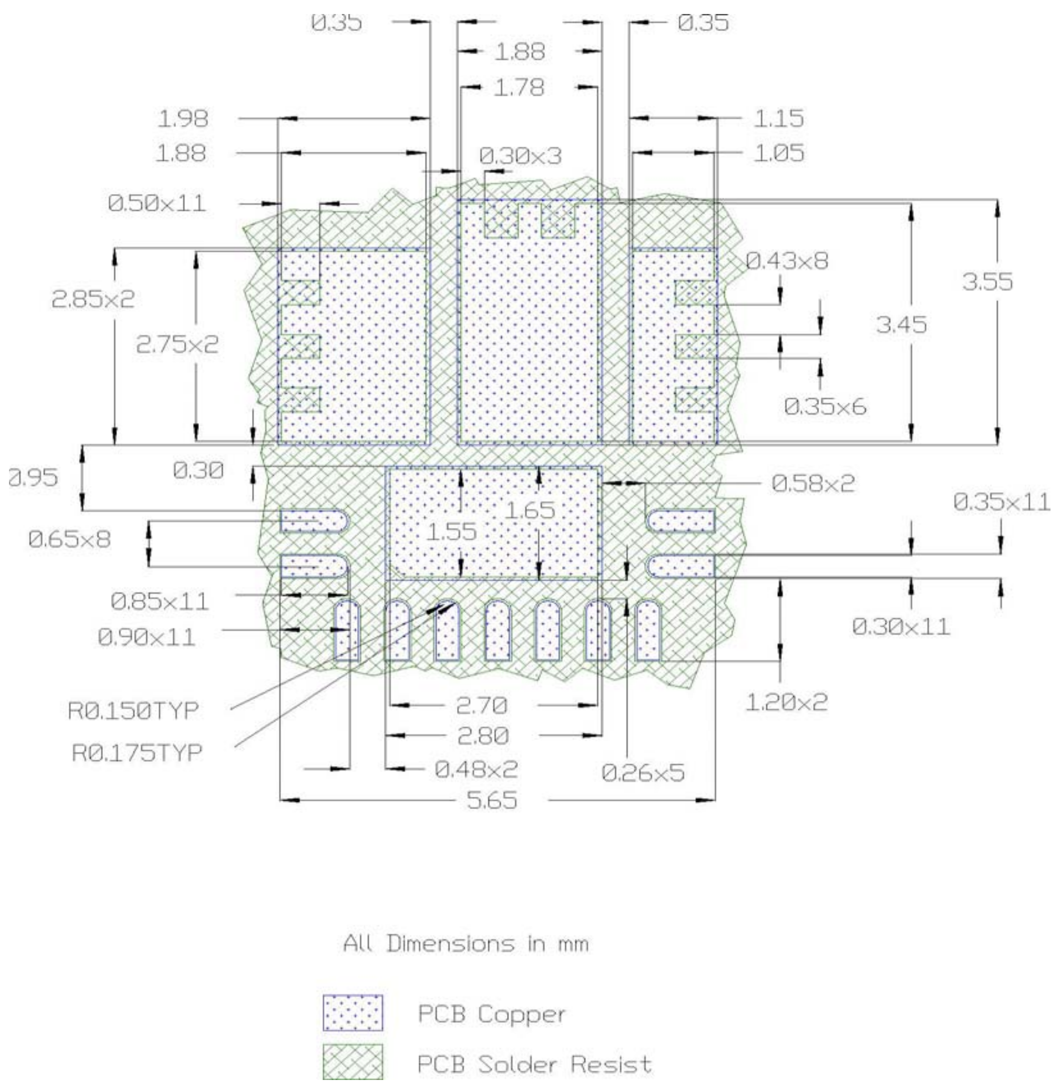


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

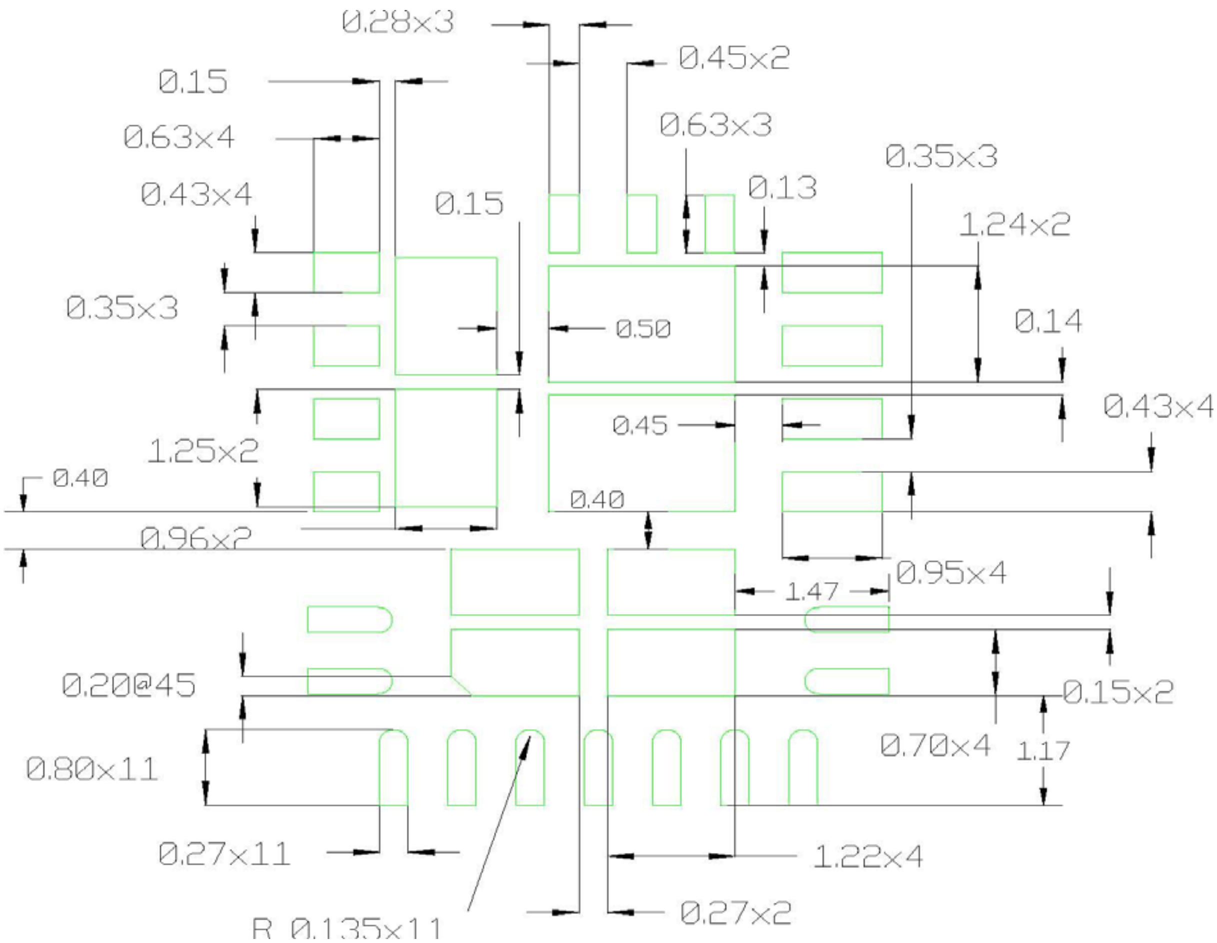
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ⩾ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

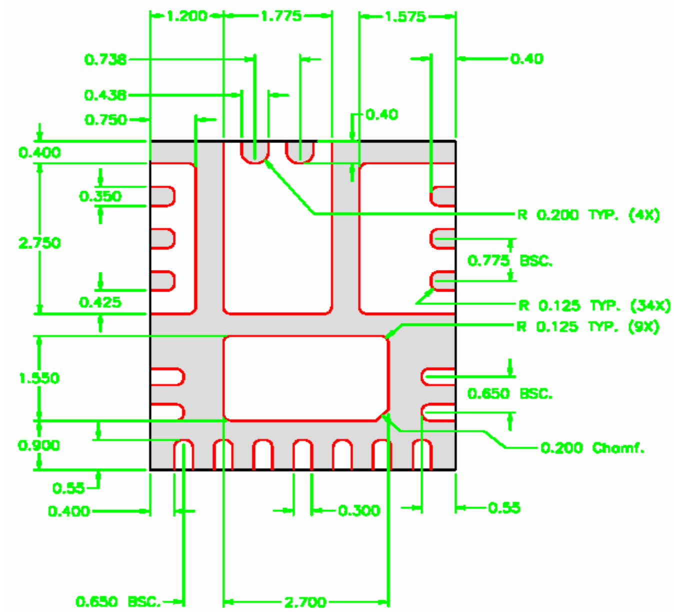


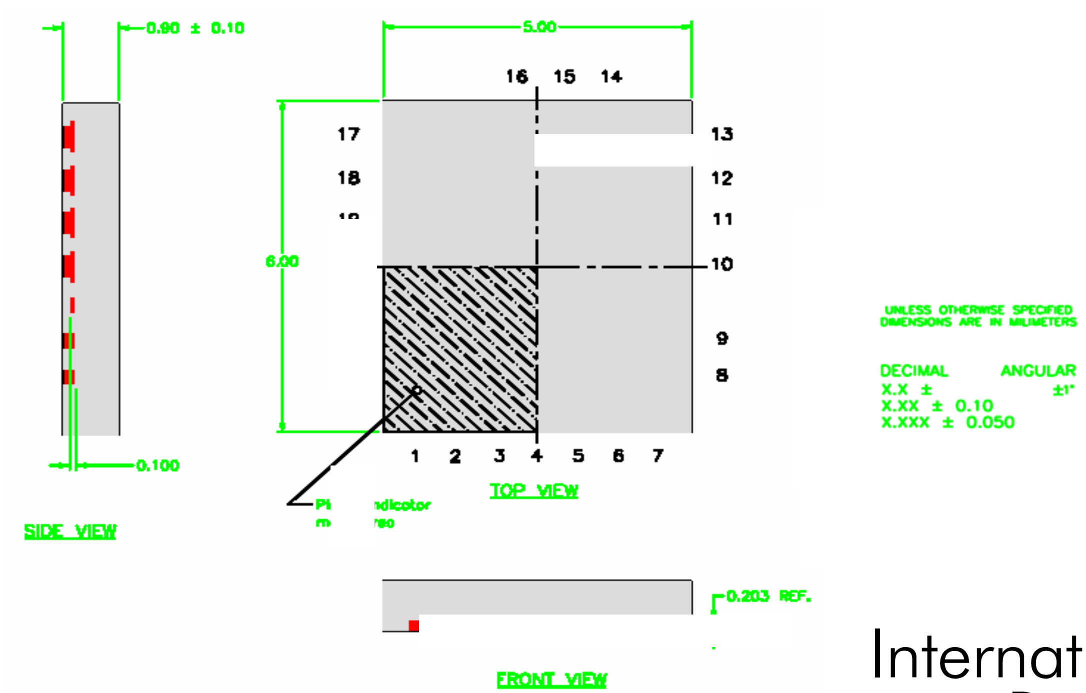
Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm





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