PD-94526A

International
IOR Rectifier

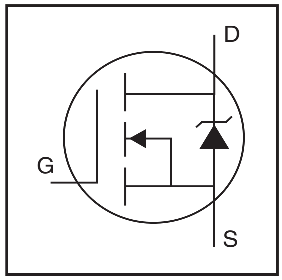
AUTOMOTIVE MOSFET

IRF1503

Typical Applications
- 14V Automotive Electrical Systems
- 14V Electronic Power Steering

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

HEXFET® Power MOSFET

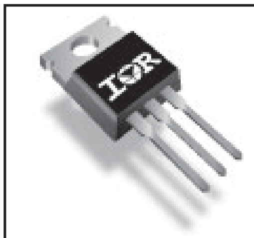


V_{DSS} = 30V

$R_{DS(on)}$ = 3.3mΩ

I_D = 75A

Description
Specifically designed for Automotive applications, this design of HEXFET® Power MOSFETs utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



TO-220AB

Absolute Maximum Ratings

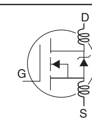
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon limited)	240	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (See Fig.9)	170	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package limited)	75	
I_{DM}	Pulsed Drain Current ①	960	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	510	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value⑥	980	
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

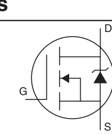
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

12/11/02

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.028	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	2.6	3.3	mΩ	V_{GS} = 10V, I_D = 140A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	75	–––	–––	S	V_{DS} = 25V, I_D = 140A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	μA	V_{DS} = 30V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 30V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-200		V_{GS} = -20V
Q_g	Total Gate Charge	–––	130	200	nC	I_D = 140A
Q_{gs}	Gate-to-Source Charge	–––	36	54		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	41	62		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	–––	17	–––	ns	V_{DD} = 15V
t_r	Rise Time	–––	130	–––		I_D = 140A
$t_{d(off)}$	Turn-Off Delay Time	–––	59	–––		R_G = 2.5Ω
t_f	Fall Time	–––	48	–––		V_{GS} = 10V ③
L_D	Internal Drain Inductance	–––	5.0	–––	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	–––	13	–––		
C_{iss}	Input Capacitance	–––	5730	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	2250	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	290	–––		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	7580	–––		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	2290	–––		V_{GS} = 0V, V_{DS} = 24V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ④	–––	3420	–––		V_{GS} = 0V, V_{DS} = 0V to 24V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	240	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	960		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 140A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	71	110	ns	T_J = 25°C, I_F = 140A, V_{DD} = 15V
Q_{rr}	Reverse RecoveryCharge	–––	110	170	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.049mH R_G = 25Ω, I_{AS} = 140A. (See Figure 12).

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

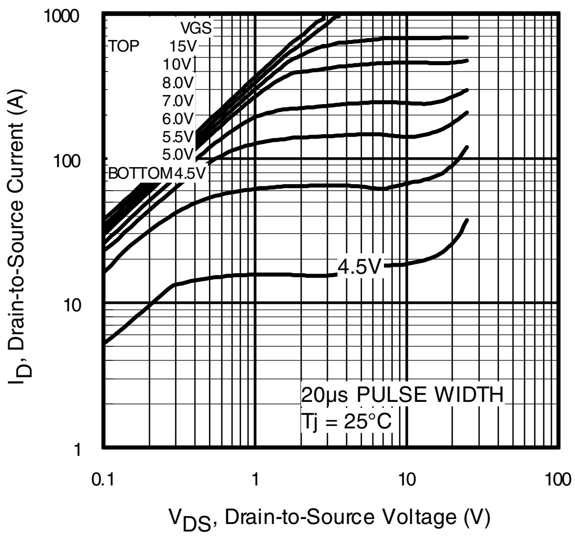


Fig 1. Typical Output Characteristics

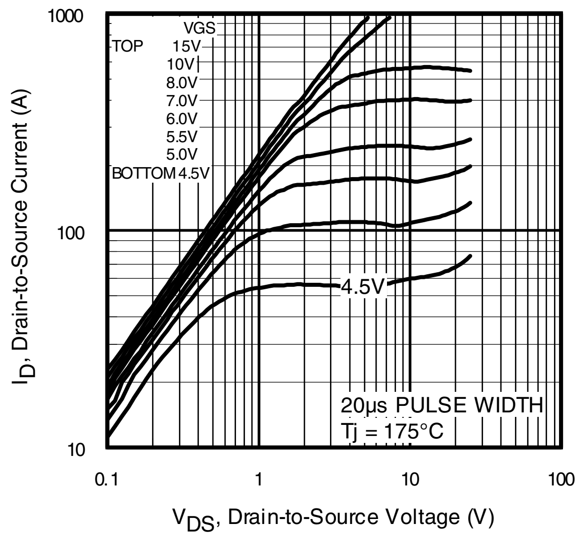


Fig 2. Typical Output Characteristics

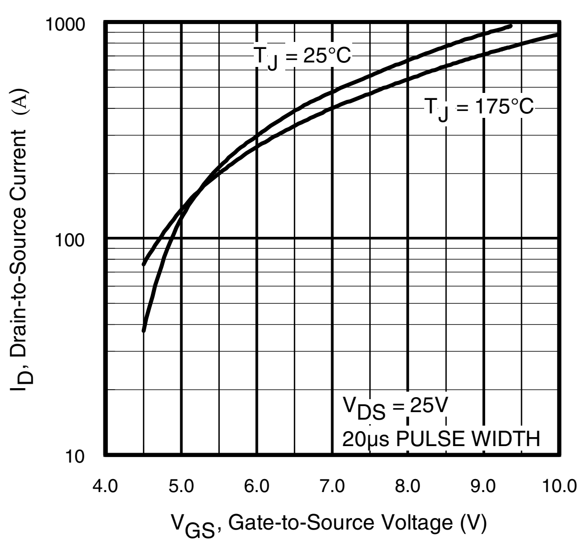


Fig 3. Typical Transfer Characteristics

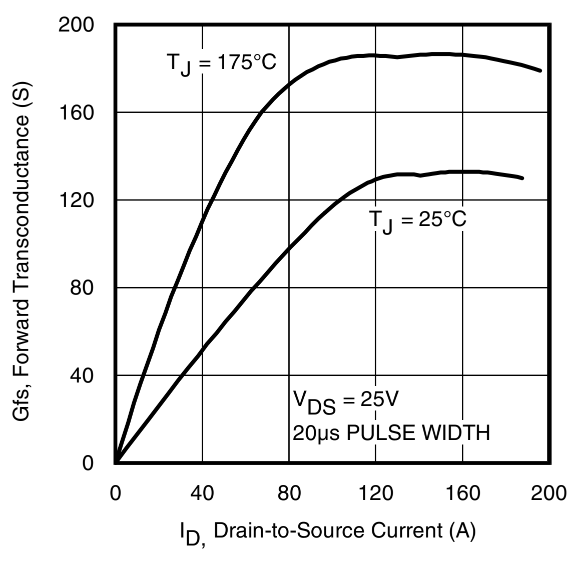


Fig 4. Typical Forward Transconductance Vs. Drain Current

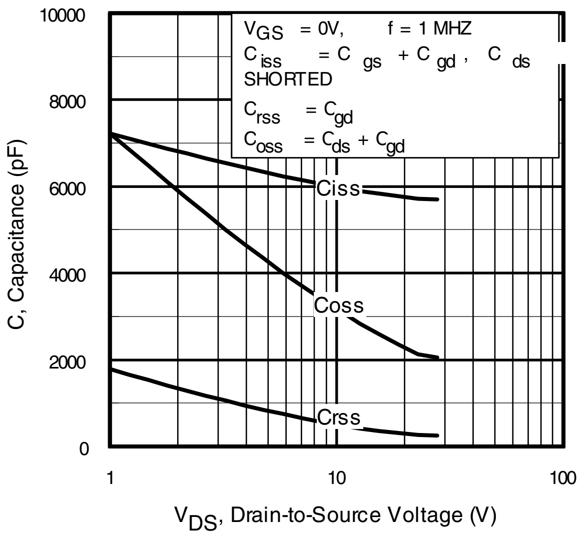


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

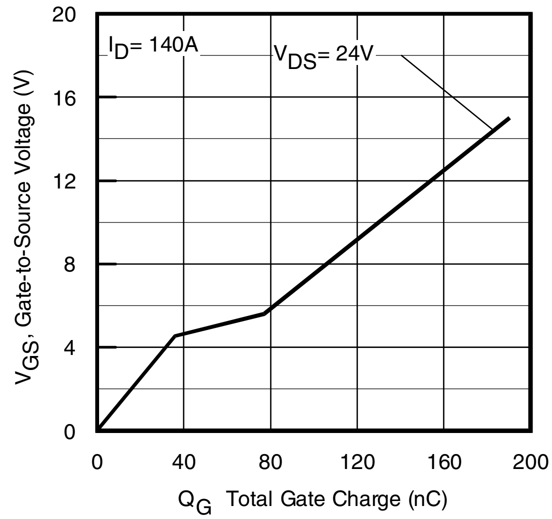


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

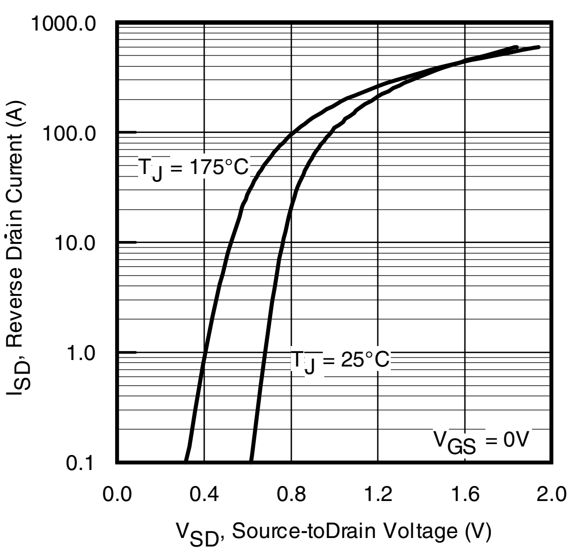


Fig 7. Typical Source-Drain Diode Forward Voltage

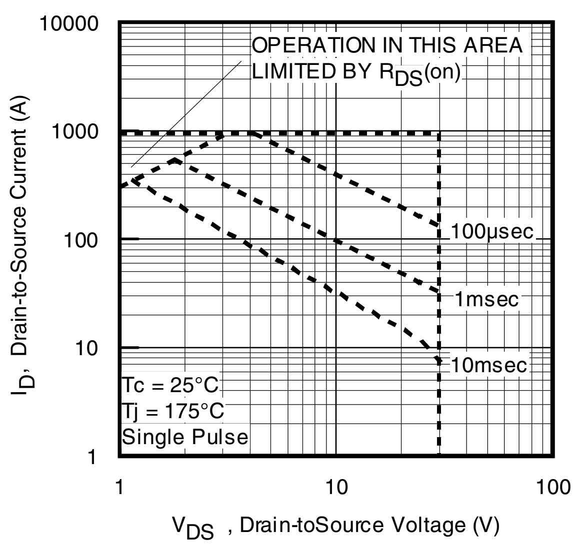


Fig 8. Maximum Safe Operating Area

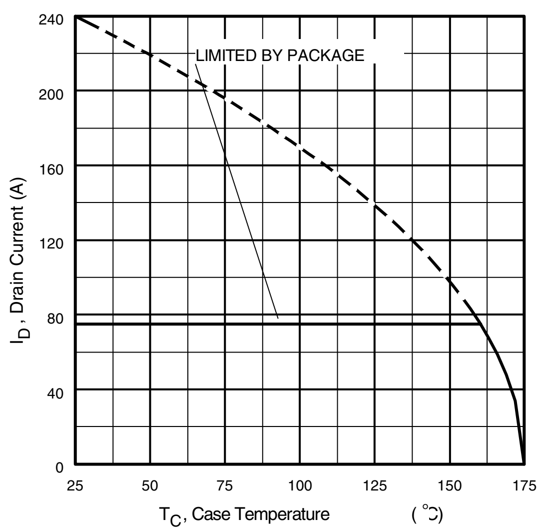


Fig 9. Maximum Drain Current Vs. Case Temperature

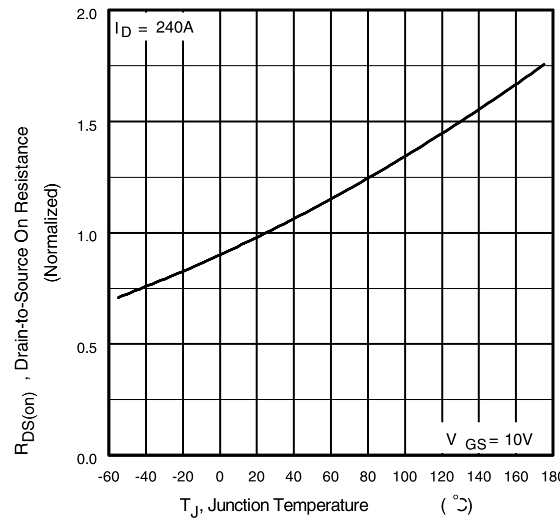


Fig 10. Normalized On-Resistance Vs. Temperature

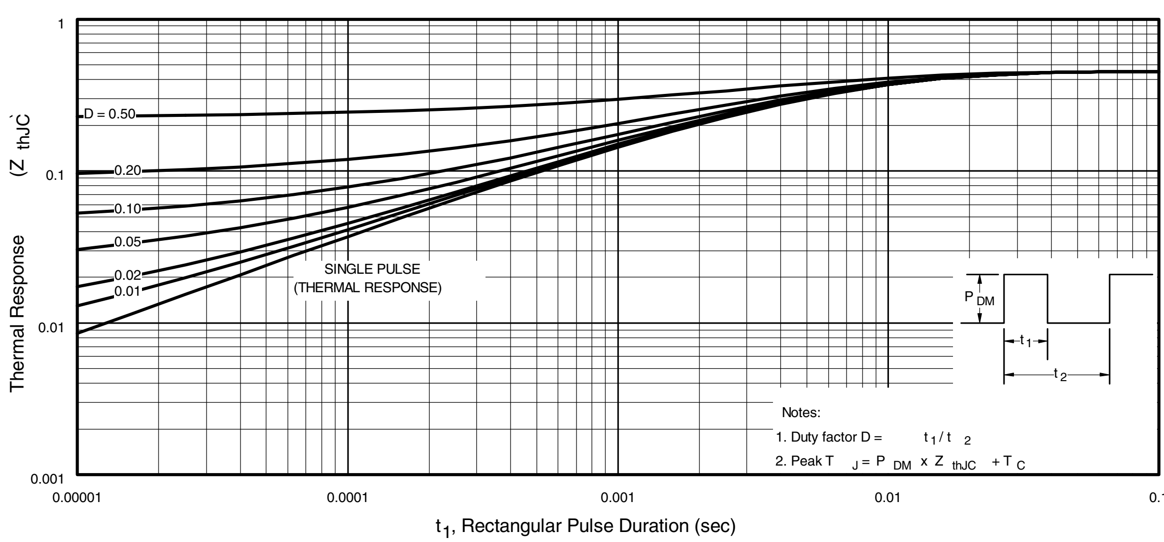


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

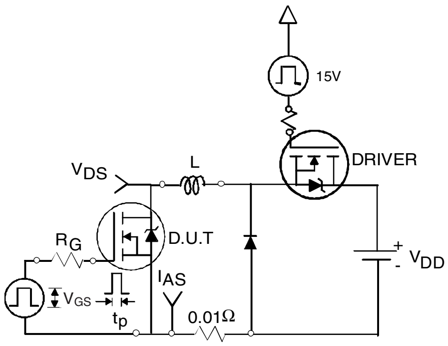


Fig 12a. Unclamped Inductive Test Circuit

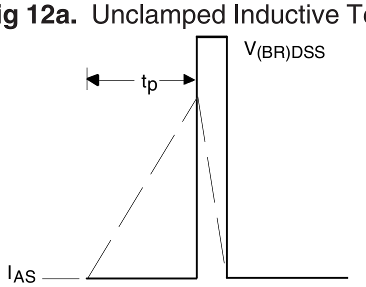


Fig 12b. Unclamped Inductive Waveforms

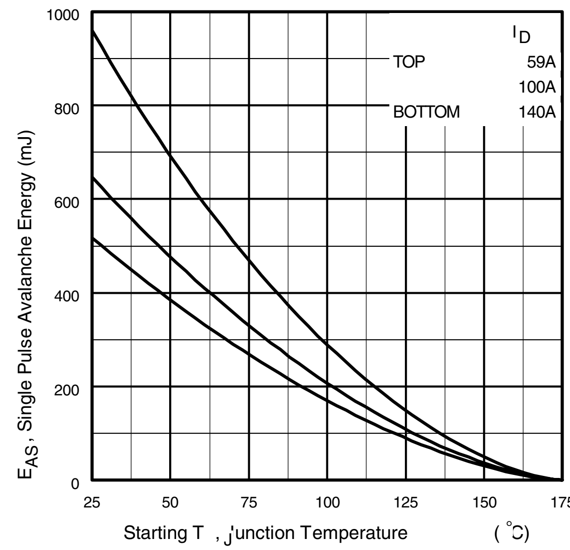


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

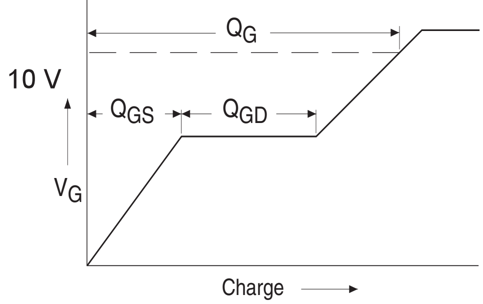


Fig 13a. Basic Gate Charge Waveform

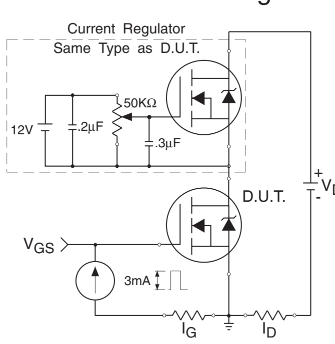


Fig 13b. Gate Charge Test Circuit

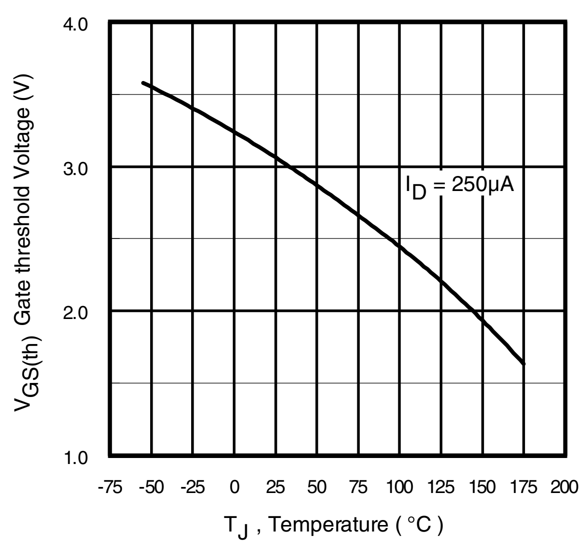


Fig 14. Threshold Voltage Vs. Temperature

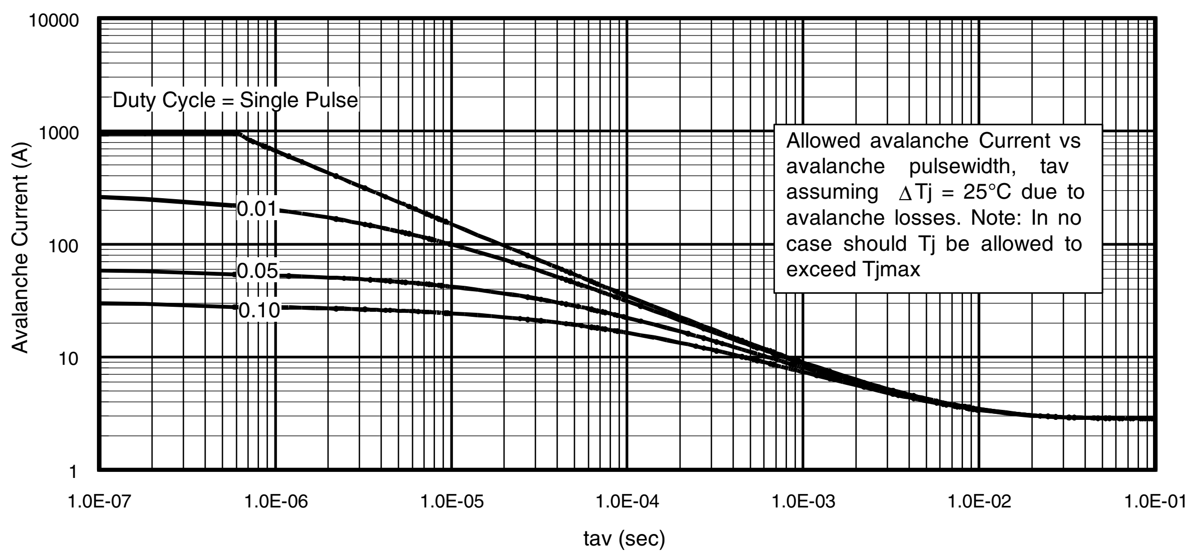


Fig 15. Typical Avalanche Current Vs.Pulsewidth

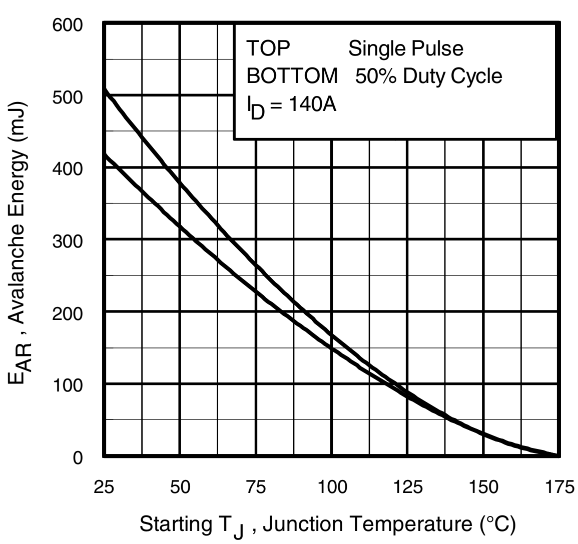


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

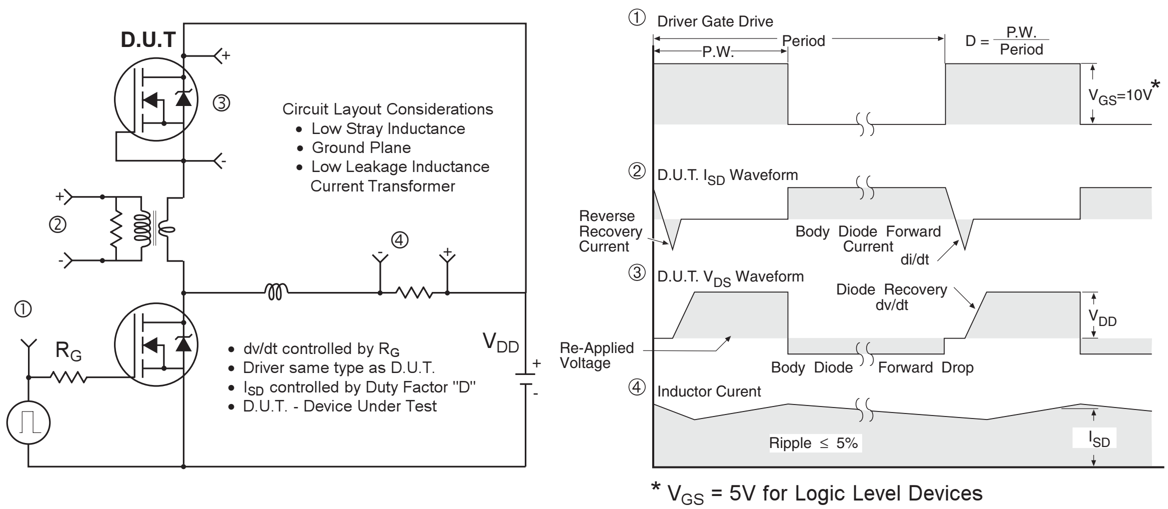


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

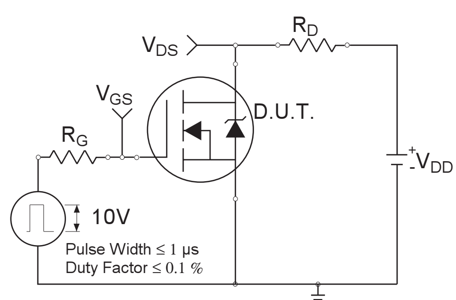


Fig 18a. Switching Time Test Circuit

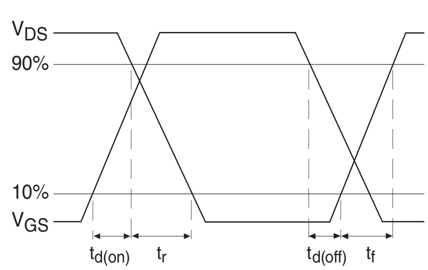
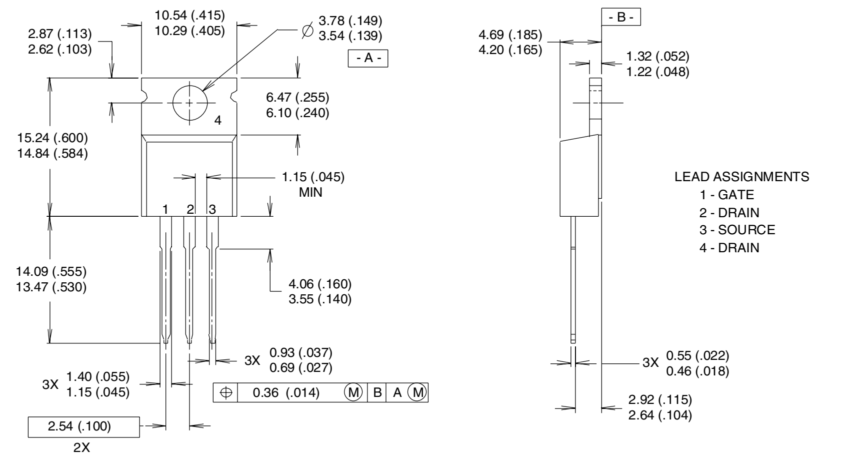


Fig 18b. Switching Time Waveforms

Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)

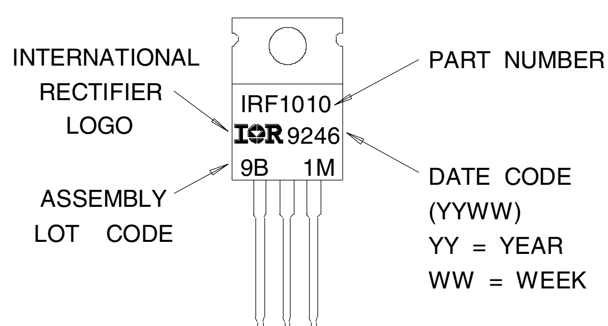


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/