ISL71830SEH

Radiation Tolerant 5V 16-Channel Analog Multiplexer

FN8758
Rev 4.00
February 6, 2017

The ISL71830SEH is a radiation tolerant, 16-channel multiplexer that is fabricated using Intersil's proprietary P6-SOI process technology to provide excellent latch-up performance. It operates with a single supply range from 3V to 5.5V and has a 4-bit address line plus an enable that can be driven with adjustable logic thresholds to conveniently select one of 16 available channels. An inactive channel is separated from the active channel by a high impedance, which inhibits any interaction between them.

The ISL71830SEH's low $r_{DS(ON)}$ allows for improved signal integrity and reduced power losses. The ISL71830SEH is also designed for cold sparing, making it excellent for redundancy in high reliability applications. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71830SEH also has analog overvoltage protection on the input that disables the switch during an overvoltage event to protect upstream and downstream devices.

The ISL71830SEH is available in a 28 Ld CDFP and operates across the extended temperature range of -55°C to +125°C.

A 32-channel version is also available offered in a 48 Ld CQFP. Refer to the ISL71831SEH datasheet for more information. For a list of differences, refer to Table 1 on page 2.

Related Literature

- For a full list of related documents, visit our website
  - ISL71830SEH product page

Features

- **DLA SMD# 5962-15247**
- **Fabricated using P6 SOI process technology**
- **Rail-to-rail operation**
- **No latch-up**
- **Low $r_{DS(ON)}$ . . . . . <120Ω (maximum)**
- **Single supply operation . . . . . 3V to 5.5V**
  - Adjustable logic threshold control
- **Cold sparing capable . . . . . -0.4V to 7V**
- **Analog overvoltage range . . . . . -0.4V to 7V**
- Switch input off leakage 120nA
- Transition times (t_{AHL}) 70ns
- Internally grounded metal lid
- Break-before-make switching
- ESD protection ≥5kV (HBM)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - Low dose rate (0.01rad(Si)/s) . . . . . 75krad(Si)
  - SEL/SEB LET_{TH} (V^+ = 6.5V). . . . . 60MeV•cm^2/mg
- All lots are assurance tested to 75krad (0.01rad(Si)/s) wafer-by-wafer.

Applications

- Telemetry signal processing
- Harsh environments
- Down-hole drilling

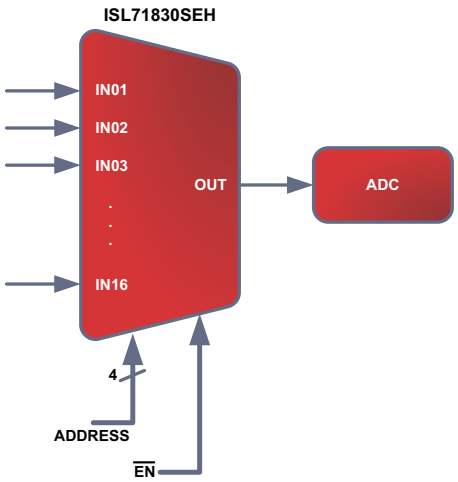


FIGURE 1. TYPICAL APPLICATION

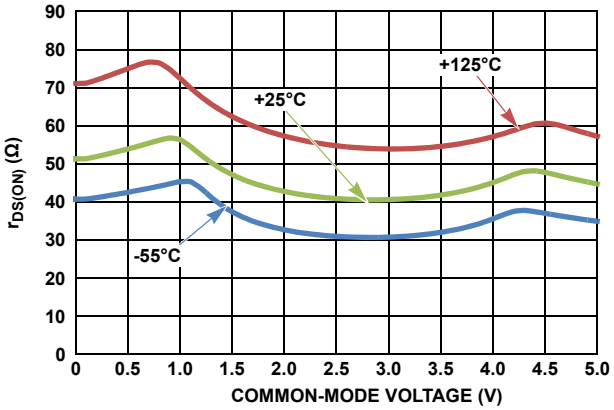


FIGURE 2. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE (V^+ = 5V)

Ordering Information

SMD ORDERING NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962L1524701VXC	ISL71830SEHVF	-55 to +125	28 Ld CDFP	K28.A
N/A	ISL71830SEHF/PROTO	-55 to +125	28 Ld CDFP	K28.A
5962L1524701V9A	ISL71830SEHVX	-55 to +125	DIE	
N/A	ISL71830SEHX/SAMPLE	-55 to +125	DIE	
N/A	ISL71830SEHEV1Z	Evaluation Board		

NOTES:

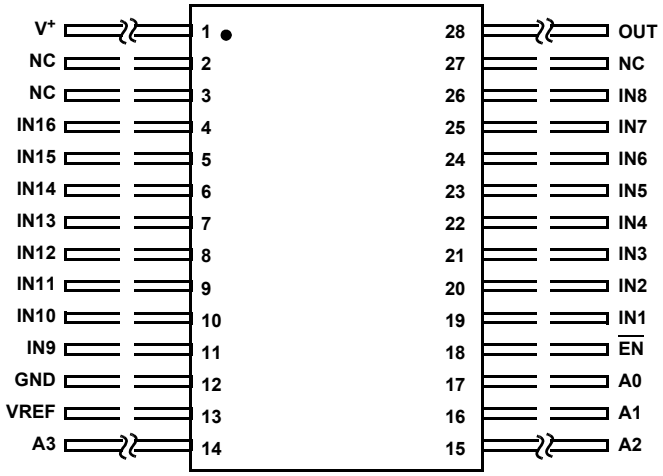
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	NUMBER OF CHANNELS	OUTPUT LEAKAGE	PACKAGE
ISL71830SEH	16	60nA	28 Ld CDFP
ISL71831SEH	32	120nA	48 Ld CQFP

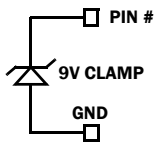
Pin Configuration

ISL71830SEH
(28 LD CDFP)
TOP VIEW

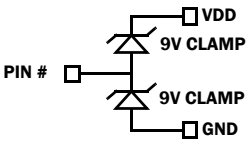


Pin Descriptions

PIN NAME	ESD CIRCUIT	PIN NUMBER	DESCRIPTION
OUT	2	28	Output for multiplexer.
V^+	1	1	Positive power supply.
NC	-	2, 3, 27	Not electrically connected.
INx	1	4, 5, 6, 7, 8, 9, 10, 11, 19, 20, 21, 22, 23, 24, 25, 26	Input for multiplexer.
Ax	1	14, 15, 16, 17	Address lines for multiplexer.
$\overline{EN}$	1	18	Enable control for multiplexer (active low).
VREF	1	13	Reference voltage used to set logic thresholds.
GND	-	12	Ground
LID	-	-	Package lid is internally connected to GND (Pin 12).



CIRCUIT 1



CIRCUIT 2

Absolute Maximum Ratings

Maximum Supply Voltage (V^+ to GND) 7V
Maximum Supply Voltage (V+ to GND) (Note 5) 6.5V
Analog Input Voltage Range (INx) . . . . . -0.4V to 7V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . . (GND - 0.4V) to V_{REF}
VREF to GND 7V
ESD Tolerance
Human Device Model (Tested per MIL-STD-883 TM 3015) 5kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A) 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld CDFP (Notes 3, 4)	55	8.5

Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Supply Voltage . . . . . 3V to 5.5V
V_{REF} to GND . . . . . 3V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.
5. Tested in a heavy ion environment at LET = 60MeV • cm^2/mg at +125°C.

Electrical Specifications, V^+ = 5V

GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Analog Input Signal Range	V_{IN}		0		V^+	V
Channel On-Resistance	$r_{DS(ON)}$	V^+ = 4.5V, V_{IN} = 0V to V^+ I_{OUT} = 1mA	-	40	**120**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V^+ = 4.5V, V_{IN} = 0V, 2.25V, 4.5V I_{OUT} = 1mA	-	-	**5**	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V^+ = 4.5V, V_{IN} = 0V to V^+	-	-	**40**	Ω
Switch Input Off Leakage	$I_{IN(OFF)}$	V^+ = 5.5V, V_{IN} = 5V, Unused inputs and V_{OUT} = 0.5V	**-30**	-	**30**	nA
		V^+ = 5.5V, V_{IN} = 0.5V, Unused inputs and V_{OUT} = 5V	**-30**	-	**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-OV)}$	V^+ = 5.5V, V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-30	-	120	nA
		Post radiation, +25°C	-30	-	30	nA
Switch Input Off Leakage with Supply Voltage Grounded	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V $V^+ = V_{EN} = V_{REF}$ = 0V, T_A = +25°C, -55°C	-20	-	20	nA
		T_A = +125°C	-20	-	50	nA
		Post radiation, +25°C	-20	-	20	nA
Switch Input Off Leakage with Supply Voltage Open	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V $V^+ = V_{EN} = V_{REF}$ = Open, T_A = +25°C, -55°C	-20	-	20	nA
		T_A = +125°C	-20	-	50	nA
		Post radiation, +25°C	-20	-	20	nA
Switch On Input Leakage with Overvoltage Applied to the Input	$I_{IN(ON-OV)}$	V^+ = 5.5V, V_{IN} = 7V, V_{OUT} = OPEN	**2.75**	-	**5.50**	µA

Electrical Specifications, V^+ = 5V GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Switch Output Off Leakage	$I_{OUT(OFF)}$	V^+ = 5.5V, V_{OUT} = 5V, All inputs = 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	150	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 5.5V, V_{OUT} = 0.5V, All inputs = 5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-60		0	nA
		Post radiation, +25°C	-30	-	30	nA
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V^+ = 5.5V, V_{IN} = V_{OUT} = 5V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	150	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 5.5V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-60	-	0	nA
		Post radiation, +25°C	-30	-	30	nA
Logic Input Voltage High/Low	$V_{IH/L}$	V^+ = 5.5V, V_{REF} = 3.3V	**1.3**	-	**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V^+ = 5.5V, V_{EN} = V_A = V_{REF}	**-0.1**	-	**0.1**	µA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V^+ = 5.5V, V_{EN} = V_A = 0V	**-0.1**	-	**0.1**	µA
Quiescent Supply Current	I_{SUPPLY}	V^+ = V_{REF} = V_{EN} = 5.5V V_A = 0V, T_A = +25°C, -55°C	-	-	100	nA
		T_A = +125°C	-	-	300	nA
		Post radiation, +25°C	-	-	300	nA
Reference Quiescent Supply Current	I_{REF}	V^+ = V_{REF} = V_{EN} = 5.5V V_A = 0V	-	-	**200**	nA
DYNAMIC						
Addressing Transition Time	t_{AHL}	V^+ = 4.5V; Figure 3	**10**	-	**70**	ns
Break-Before-Make Delay	t_{BBM}	V^+ = 4.5V; Figure 5	**5**	18	**40**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V^+ = 4.5V; Figure 4	-	-	**40**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V^+ = 4.5V; Figure 4	-	-	**40**	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, Figure 6	-	1.4	5	pC
Off Isolation	V_{ISO}	V_{EN} = V_{REF}, R_L = OPEN, f = 1kHz	**60**	-	-	dB
Crosstalk	V_{CT}	V_{EN} = 0V, f = 1kHz, V_{P-P} = 1V, R_L = OPEN	**73**	-	-	dB
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz	-	-	**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz	-	-	**25**	pF

Electrical Specifications, $V^+ = 3.3V$

V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Analog Input Signal Range	V_{IN}		0	-	V^+	V
Channel On-Resistance	$r_{DS(ON)}$	V^+ = 3V, V_{IN} = 0V to V^+ I_{OUT} = 1mA	**25**	70	**200**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V^+ = 3V, V_{IN} = 0.5V, 2.5V I_{OUT} = 1mA	-	-	**5**	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V^+ = 3V V_{IN} = 0V to V^+	-	-	**50**	Ω
Switch Input Off Leakage	$I_{IN(OFF)}$	V^+ = 3.6V V_{IN} = 3.1V, Unused inputs and V_{OUT} = 0.5V	**-30**	-	**30**	nA
		V^+ = 3.6V V_{IN} = 0.5V, Unused inputs and V_{OUT} = 3.1V	**-30**	-	**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-OV)}$	V^+ = 3.6V V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-30	-	100	nA
		Post radiation, +25°C	-30	-	30	
Switch On Input Leakage with Overvoltage Applied to the Input	$I_{IN(ON-OV)}$	V^+ = 3.6V, V_{IN} = 7V, V_{OUT} = OPEN	**1.8**	-	**3.6**	µA
Switch Output Off Leakage	$I_{OUT(OFF)}$	V^+ = 3.6V, V_{OUT} = 3.1V, All inputs = 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	60	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 3.6V, V_{OUT} = 0.5V, All inputs = 3.1V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V^+ = 3.6V, V_{IN} = V_{OUT} = 3.1V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 3.6V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 3.1V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
Quiescent Supply Current	I_{SUPPLY}	V^+ = V_{REF} = V_{EN} = 3.6V V_A = 0V, T_A = +25°C, -55°C	-	-	100	nA
		T_A = +125°C	-	-	300	nA
		Post radiation, +25°C	-	-	300	nA
Reference Quiescent Supply Current	I_{REF}	V^+ = V_{REF} = V_{EN} = 3.6V, V_A = 0V	-	-	**200**	nA

Electrical Specifications, V^+ = 3.3V V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DYNAMIC						
Addressing Transition Time	t_{AHL}	V^+ = 3V; Figure 3	**10**	-	**100**	ns
Break-Before-Make Delay	t_{BBM}	V^+ = 3V; Figure 5	**5**	25	**50**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V^+ = 3V; Figure 4	-	-	**50**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V^+ = 3V; Figure 4	-	-	**50**	ns

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

TABLE 2. TRUTH

A3	A2	A1	A0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	1	None
0	0	0	0	0	1
0	0	0	1	0	2
0	0	1	0	0	3
0	0	1	1	0	4
0	1	0	0	0	5
0	1	0	1	0	6
0	1	1	0	0	7
0	1	1	1	0	8
1	0	0	0	0	9
1	0	0	1	0	10
1	0	1	0	0	11
1	0	1	1	0	12
1	1	0	0	0	13
1	1	0	1	0	14
1	1	1	0	0	15
1	1	1	1	0	16

NOTE:

7. X = Don't care, "1" = Logic High, "0" = Logic Low.

Timing Diagrams

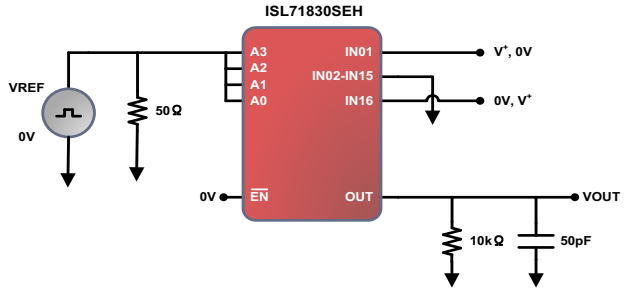


FIGURE 3. ADDRESS TIME TO OUTPUT TEST CIRCUIT

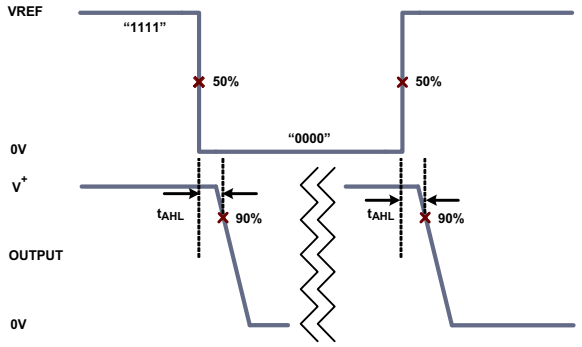


FIGURE 4. ADDRESS TIME TO OUTPUT DIAGRAM

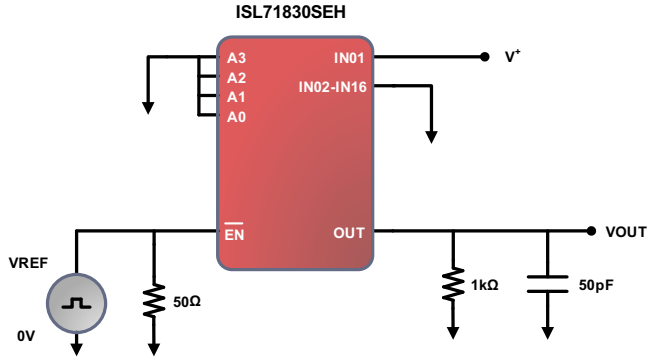


FIGURE 5. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

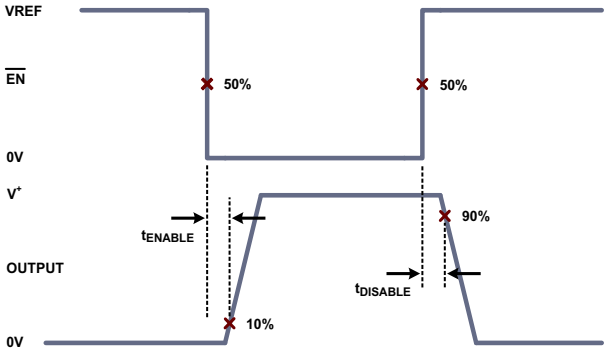


FIGURE 6. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

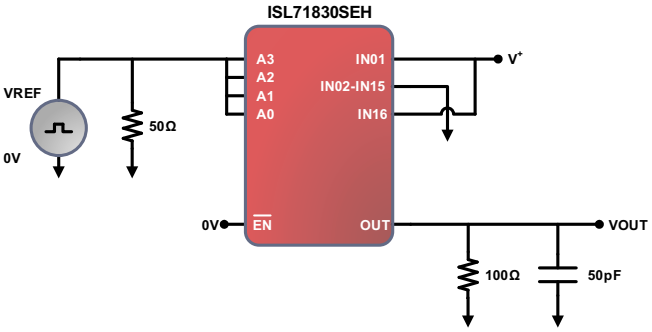


FIGURE 7. BREAK-BEFORE-MAKE TEST CIRCUIT

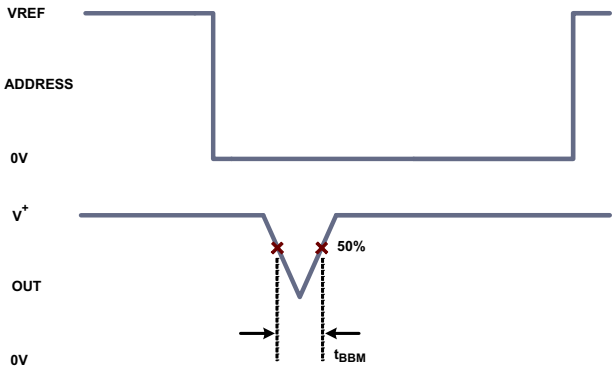


FIGURE 8. BREAK-BEFORE-MAKE DIAGRAM

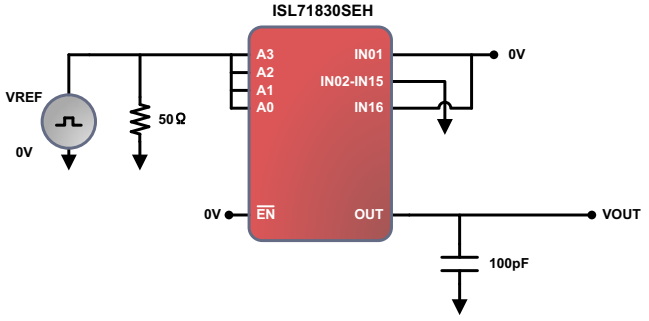


FIGURE 9. CHARGE INJECTION TEST CIRCUIT

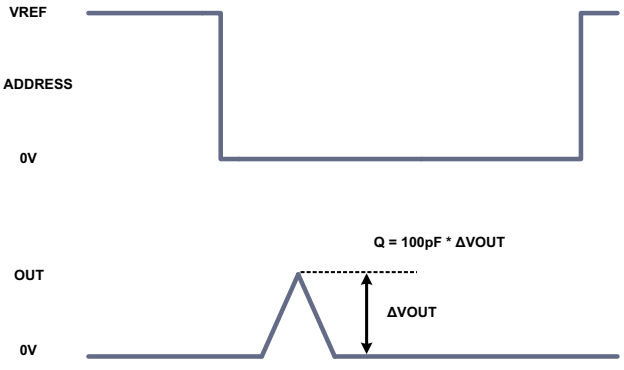


FIGURE 10. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V^+ = 5V$, $V_{REF} = 3.3V$, $V_{IN} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified.

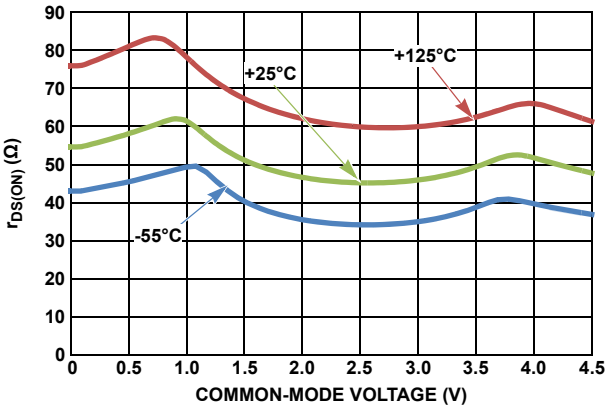


FIGURE 11. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 4.5V$)

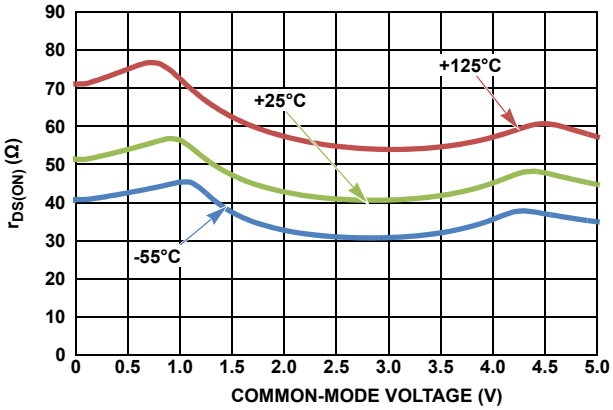


FIGURE 12. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 5V$)

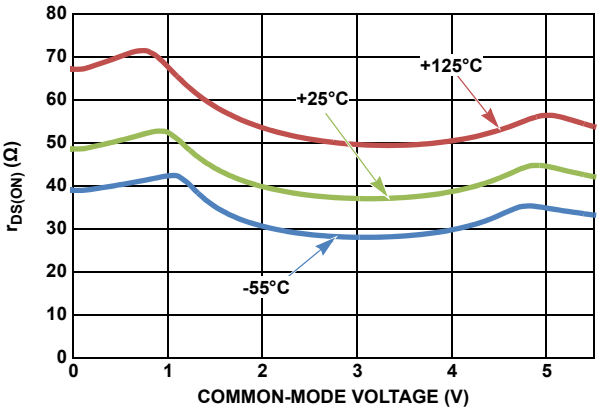


FIGURE 13. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 5.5V$)

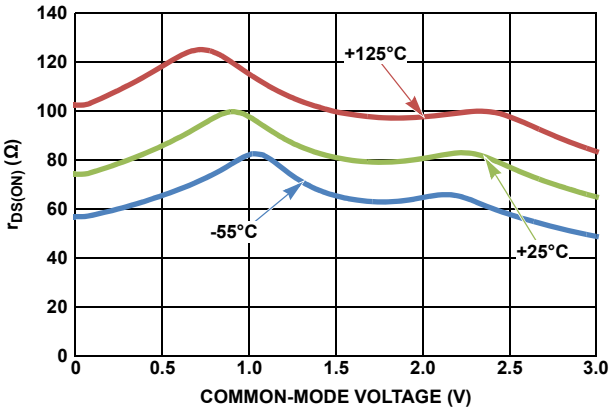


FIGURE 14. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3V$)

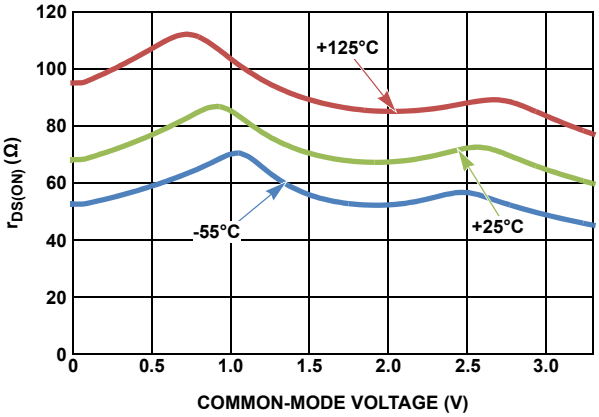


FIGURE 15. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3.3V$)

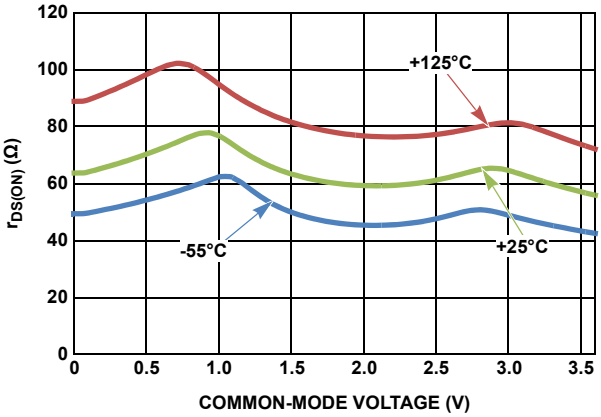


FIGURE 16. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3.6V$)

Typical Performance Curves

$V^+ = 5V$, $V_{REF} = 3.3V$, $V_{IN} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

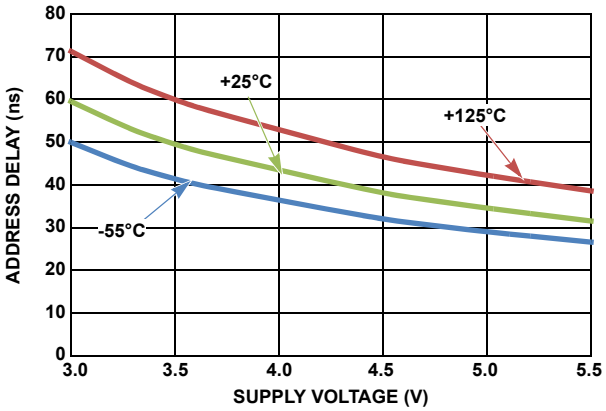


FIGURE 17. ADDRESS PROPAGATION DELAY (HIGH TO LOW)

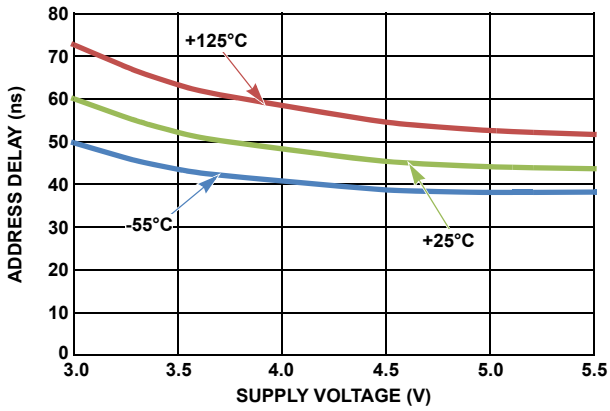


FIGURE 18. ADDRESS PROPAGATION DELAY (LOW TO HIGH)

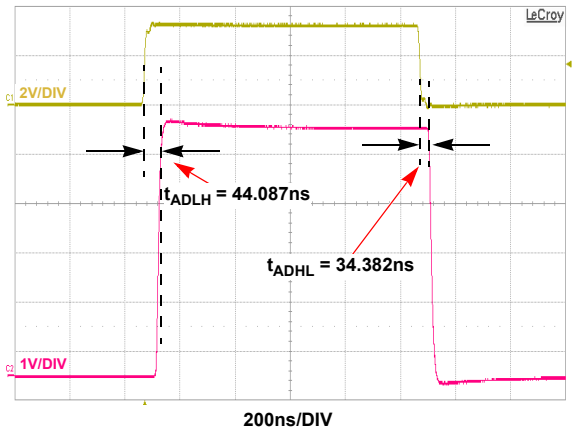


FIGURE 19. ADDRESS PROPAGATION DELAY

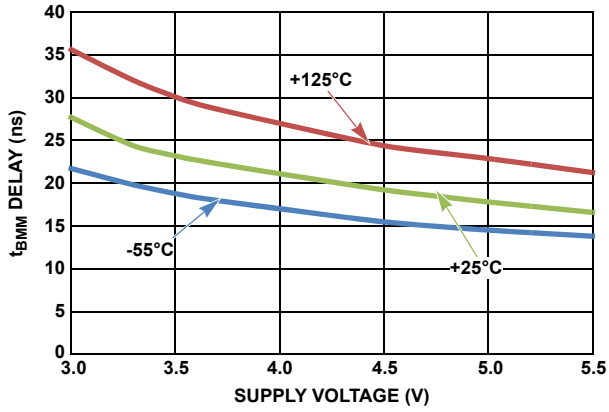


FIGURE 20. BREAK-BEFORE-MAKE DELAY

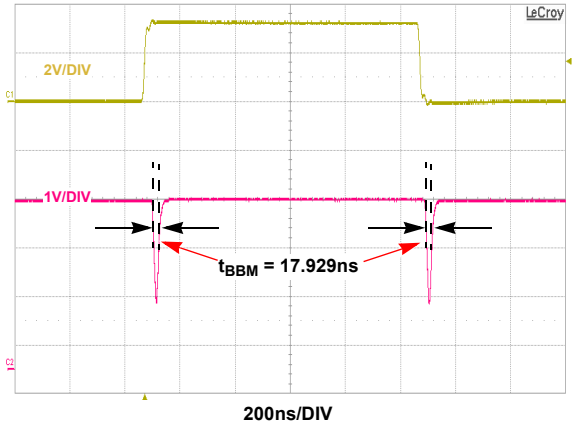


FIGURE 21. BREAK-BEFORE-MAKE DELAY

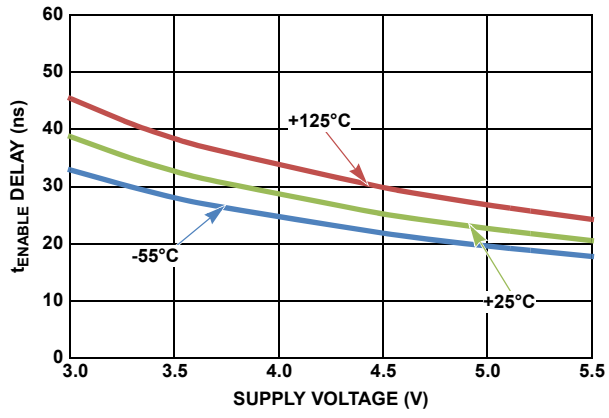


FIGURE 22. ENABLE TO OUTPUT PROPAGATION DELAY

Typical Performance Curves

$V^+ = 5V$, $V_{REF} = 3.3V$, $V_{IN} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

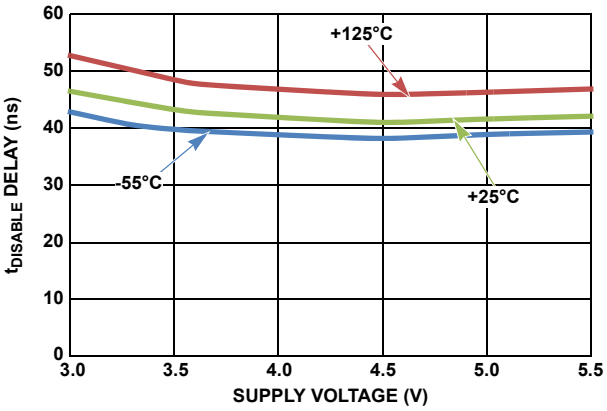


FIGURE 23. DISABLE TO OUTPUT PROPAGATION DELAY

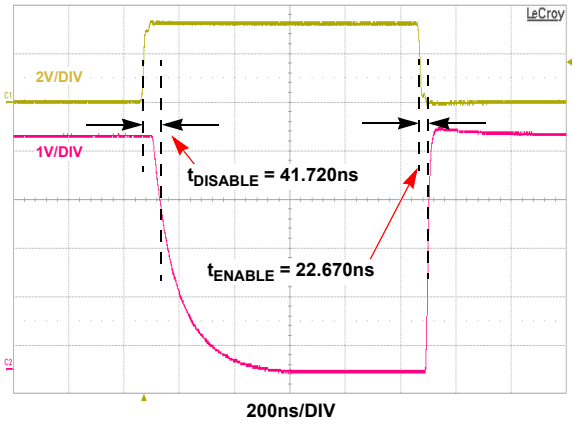


FIGURE 24. ENABLE/DISABLE PROPAGATION DELAY

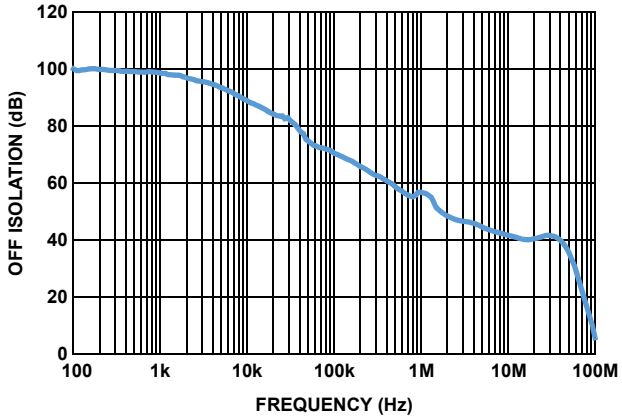


FIGURE 25. OFF ISOLATION ($V^+ = 5V$, +25°C, $R_L = 511\Omega$)

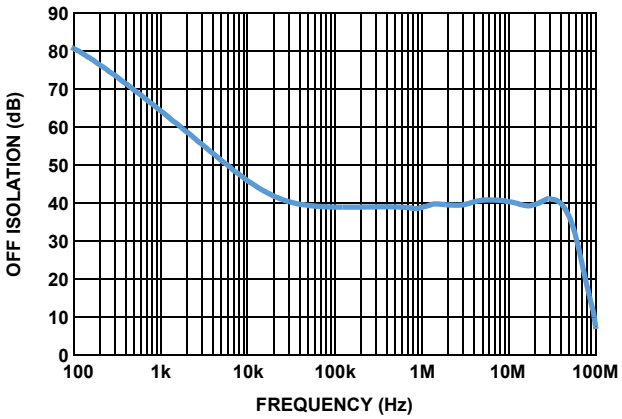


FIGURE 26. OFF ISOLATION ($V^+ = 5V$, +25°C, R_L= OPEN)

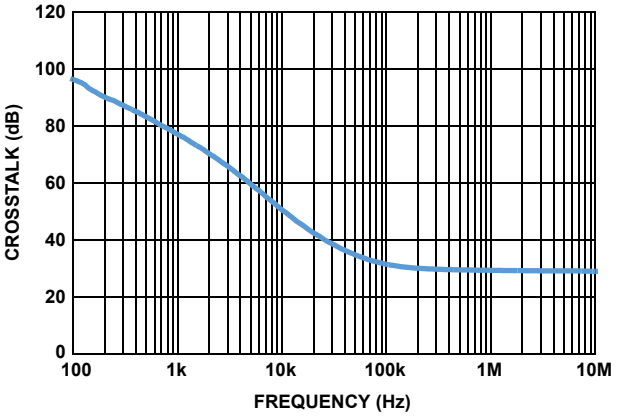


FIGURE 27. CROSSTALK ($V^+ = 5V$, +25°C, R_L = OPEN)

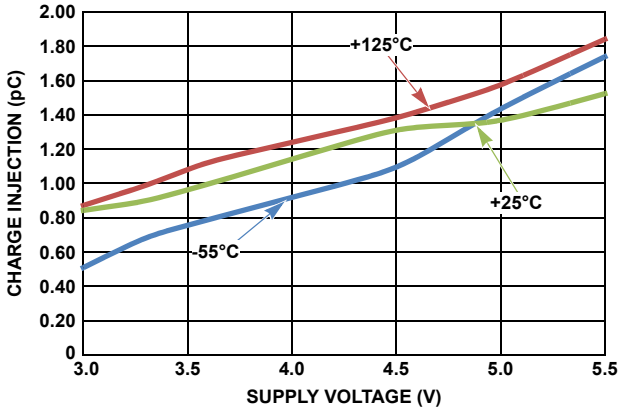


FIGURE 28. CHARGE INJECTION

Post Low Dose Rate Radiation Characteristics (V^+ = 5V)

Unless otherwise specified, V^+ = 5V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

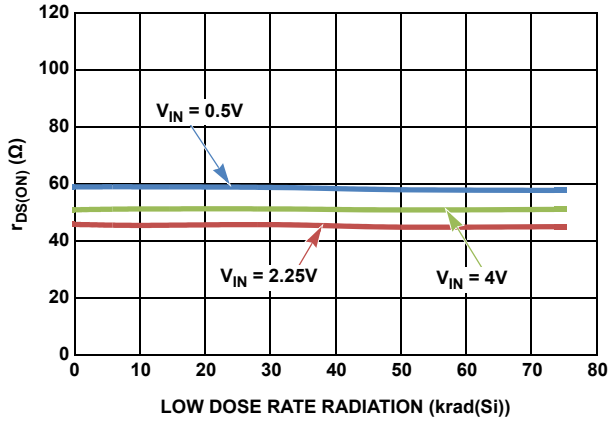


FIGURE 29. $r_{DS(ON)}$ (V^+ = 4.5V), BIASED

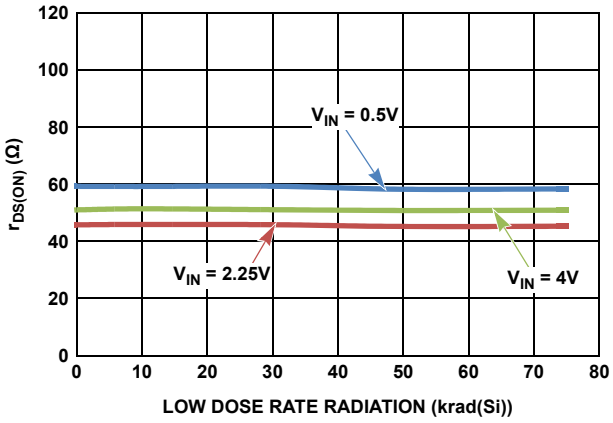


FIGURE 30. $r_{DS(ON)}$ (V^+ = 4.5V), GROUNDED

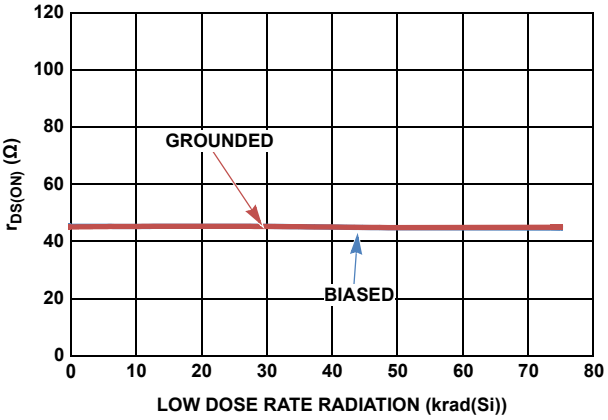


FIGURE 31. $r_{DS(ON)}$ MINIMUM (V^+ = 4.5V)

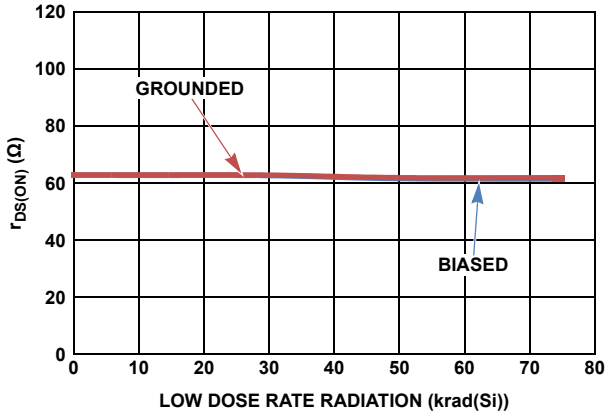


FIGURE 32. $r_{DS(ON)}$ MAXIMUM (V^+ = 4.5V)

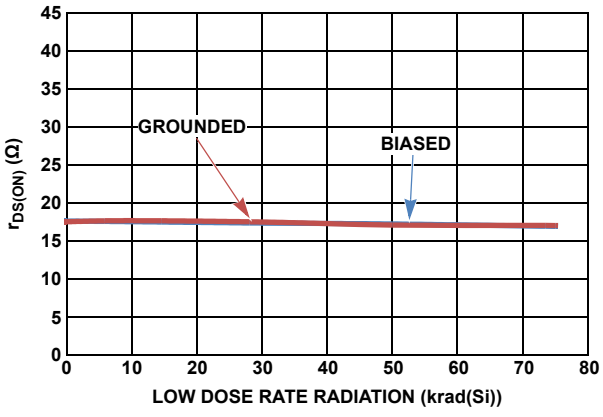


FIGURE 33. $r_{DS(ON)}$ FLATNESS (V^+ = 4.5V)

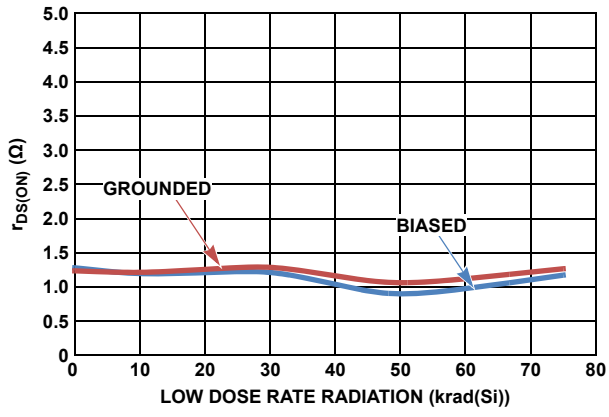


FIGURE 34. $r_{DS(ON)}$ MATCH (V^+ = 4.5V, V_{IN} = 0.5V)

Post Low Dose Rate Radiation Characteristics (V^+ = 5V)

Unless otherwise specified, V^+ = 5V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

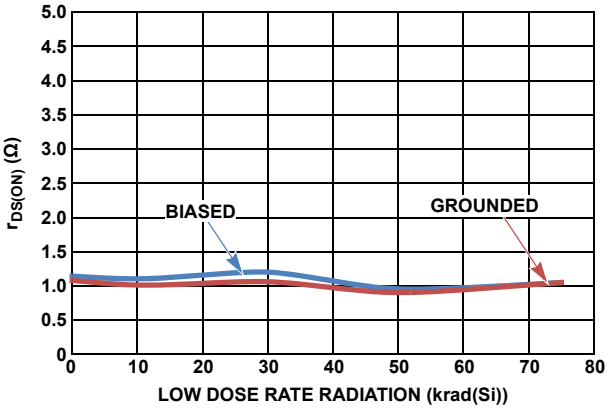


FIGURE 35. $r_{DS(ON)}$ MATCH (V^+ = 4.5V, V_{IN} = 4V)

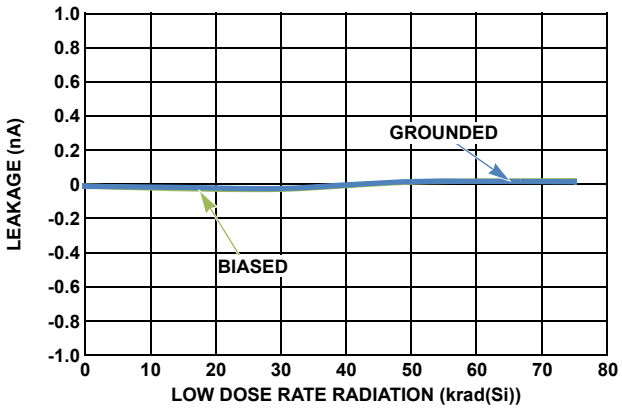


FIGURE 36. $I_{S(OFF)}$ (V^+ = 5.5V, V_{IN} = 5V)

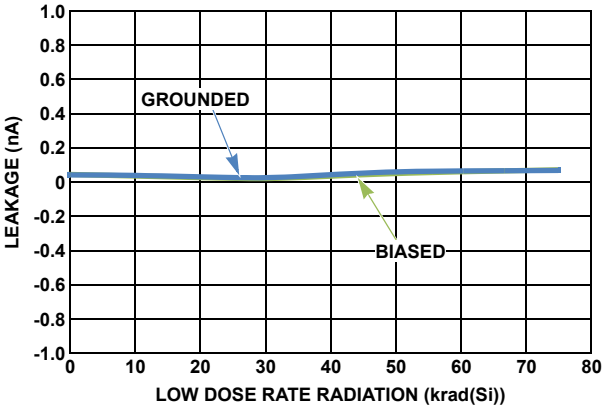


FIGURE 37. $I_{S(OFF)}$ (V^+ = 5.5V, V_S = 7V)

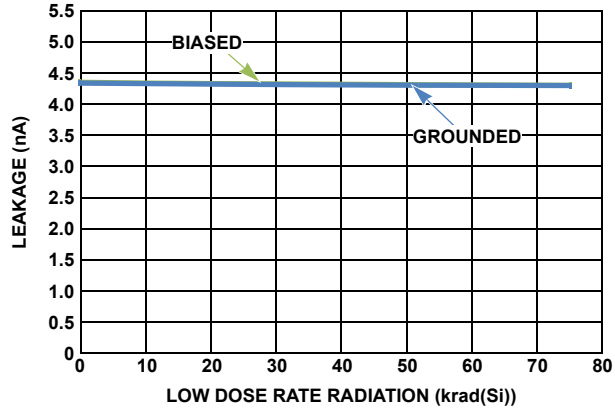


FIGURE 38. $I_{S(ON)}$ (V^+ = 5.5V, V_{IN} = 5V)

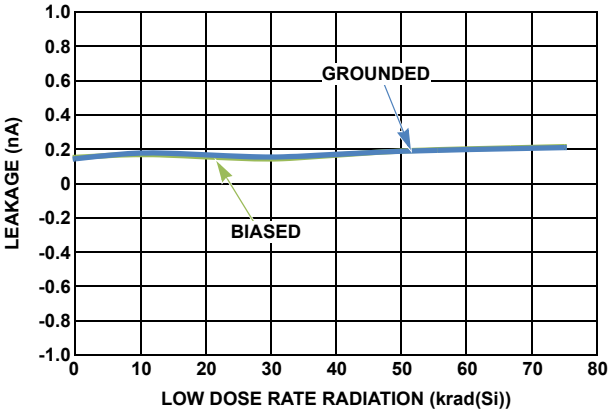


FIGURE 39. $I_{D(ON)}$ (V^+ = 5.5V, V_{IN} = 5V)

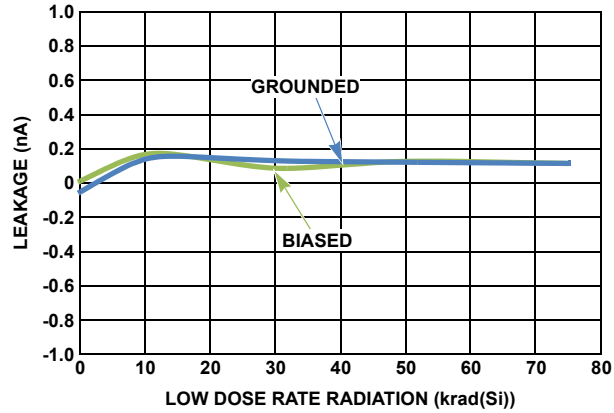


FIGURE 40. $I_{D(OFF)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

Post Low Dose Rate Radiation Characteristics (V^+ = 3.3V)

Unless otherwise specified, V^+ = 3.3V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

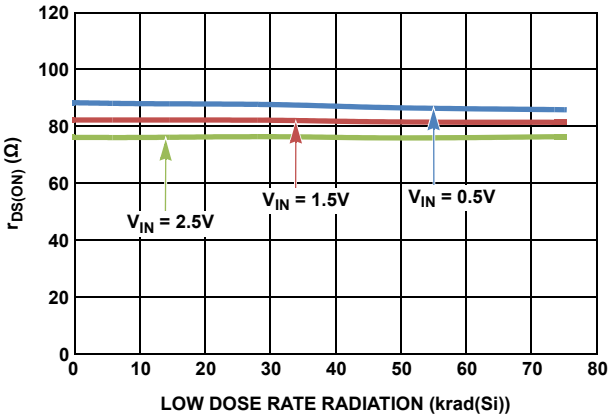


FIGURE 41. $r_{DS(ON)}$ (V^+ = 3V), BIASED

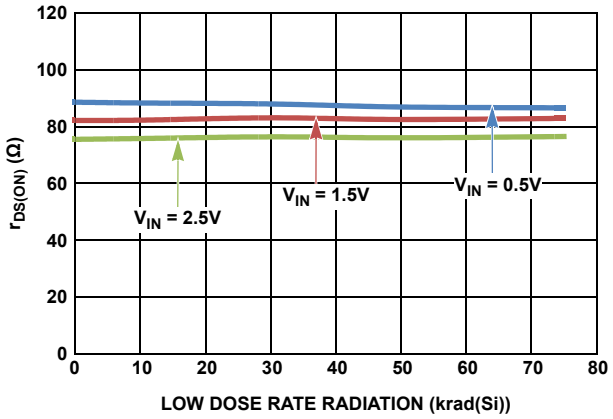


FIGURE 42. $r_{DS(ON)}$ (V^+ = 3V), GROUNDED

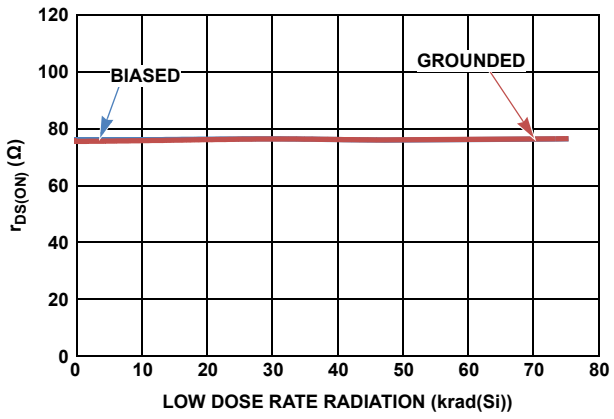


FIGURE 43. $r_{DS(ON)}$ MINIMUM (V^+ = 3V)

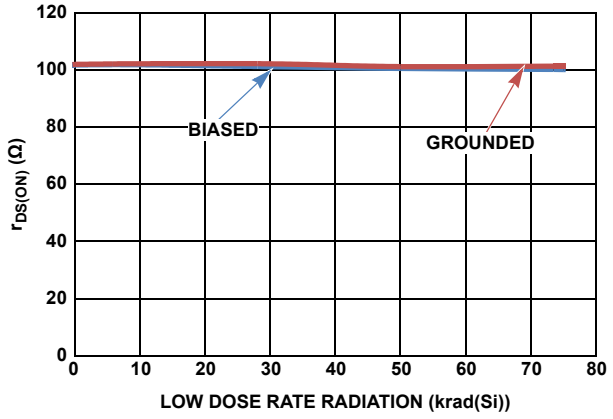


FIGURE 44. $r_{DS(ON)}$ MAXIMUM (V^+ = 3V)

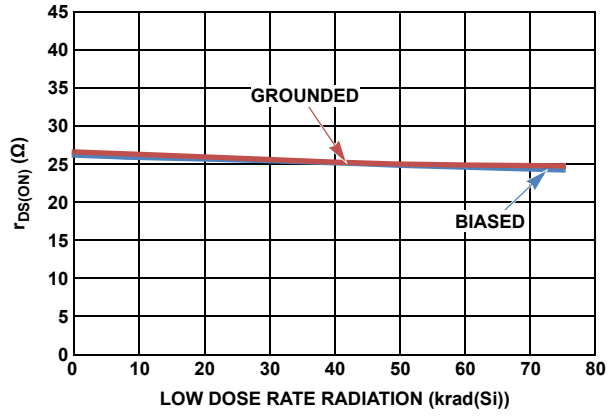


FIGURE 45. $r_{DS(ON)}$ FLATNESS (V^+ = 3V)

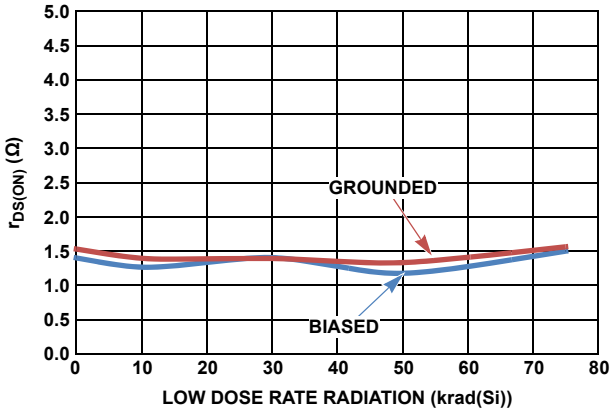


FIGURE 46. $r_{DS(ON)}$ MATCH (V^+ = 3V, V_{IN} = 0.5V)

Post Low Dose Rate Radiation Characteristics (V^+ = 3.3V)

Unless otherwise specified, V^+ = 3.3V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

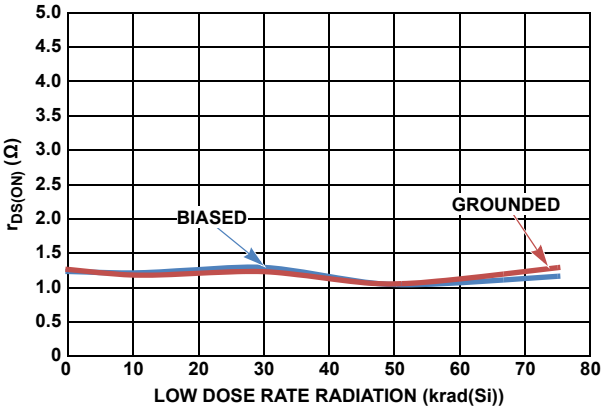


FIGURE 47. $r_{DS(ON)}$ MATCH (V^+ = 3V, V_{IN} = 2.5V)

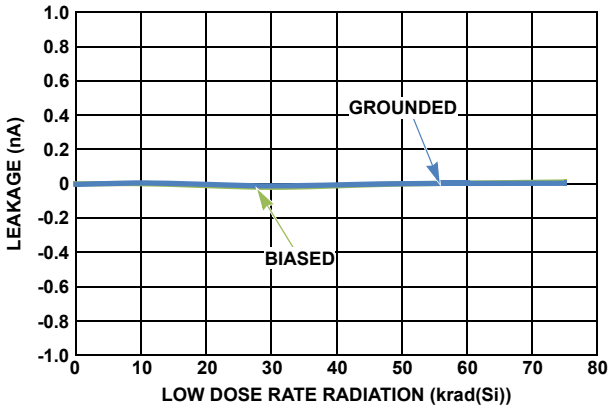


FIGURE 48. $I_{S(OFF)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

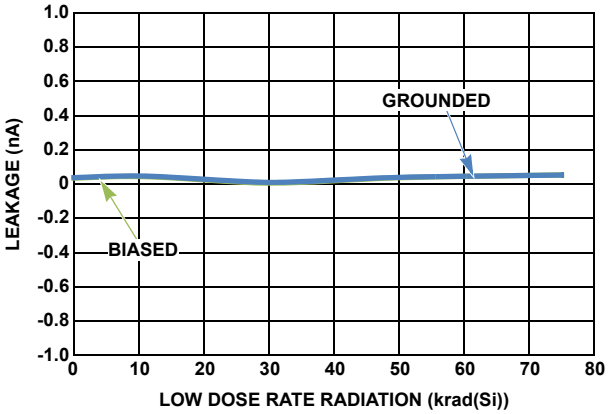


FIGURE 49. $I_{S(OFF)}$ (V^+ = 3.6V, V_{IN} = 7V)

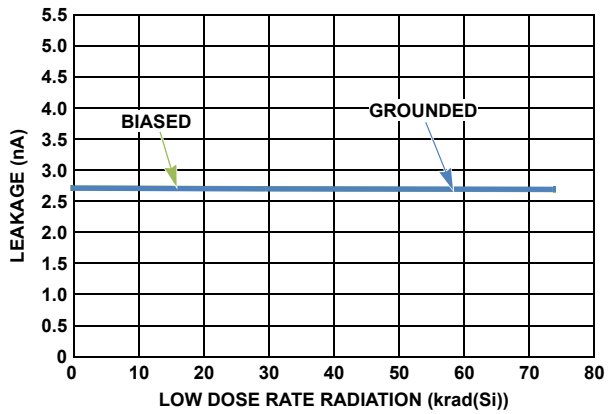


FIGURE 50. $I_{S(ON)}$ (V^+ = 3.6V, V_{IN} = 7V)

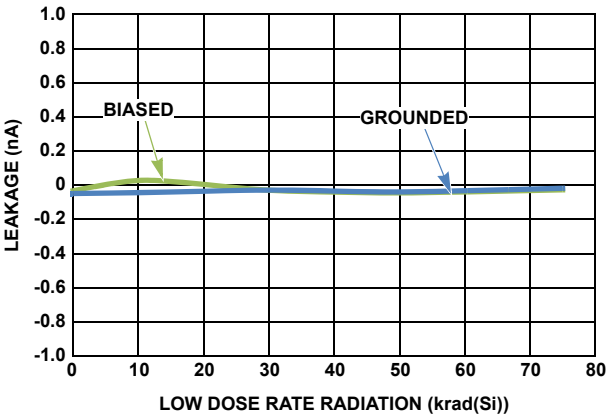


FIGURE 51. $I_{D(ON)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

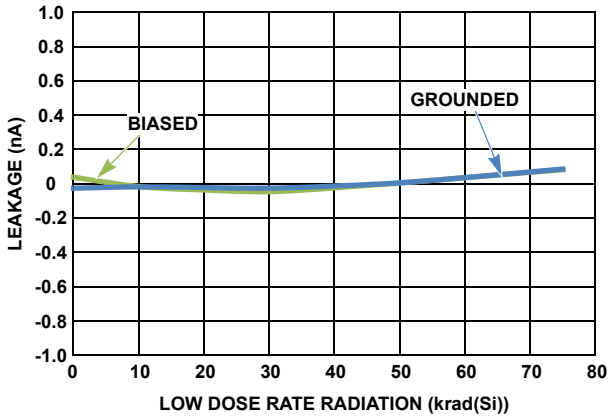


FIGURE 52. $I_{D(OFF)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+ and VREF, however, it is recommended that all supplies power-up relatively close to each other.

Overvoltage Protection

The ISL71830SEH has overvoltage protection on both the input as well as the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition, the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71830SEH. The range for VREF is between 3V and 5.5V. The switching point is set to around 50% of the voltage presented to VREF. This switching point allows for both 5V and 3.3V logic control.

ISL71830SEH vs ISL71831SEH

A 32-channel version of the ISL71830SEH is available in a 48 Ld CQFP. In terms of performance specs, the parts are very similar in behavior. Apart from the apparent increase in channel density, the ISL71831SEH does have slightly higher output leakage compared to the ISL71830SEH due to having more channels connected to the output. The supply current for the ISL71831SEH is also a bit higher compared to the ISL71830SEH.

Die Characteristics

Die Dimensions

2026µm x 2240µm (79.7638 mils x 88.1890 mils)
Thickness: 483µm ± 25µm (19 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6×10^5 A/cm^2

TRANSISTOR COUNT

3875

Weight of Packaged Device

2.091 grams

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package pin 12

Metalization Mask Layout

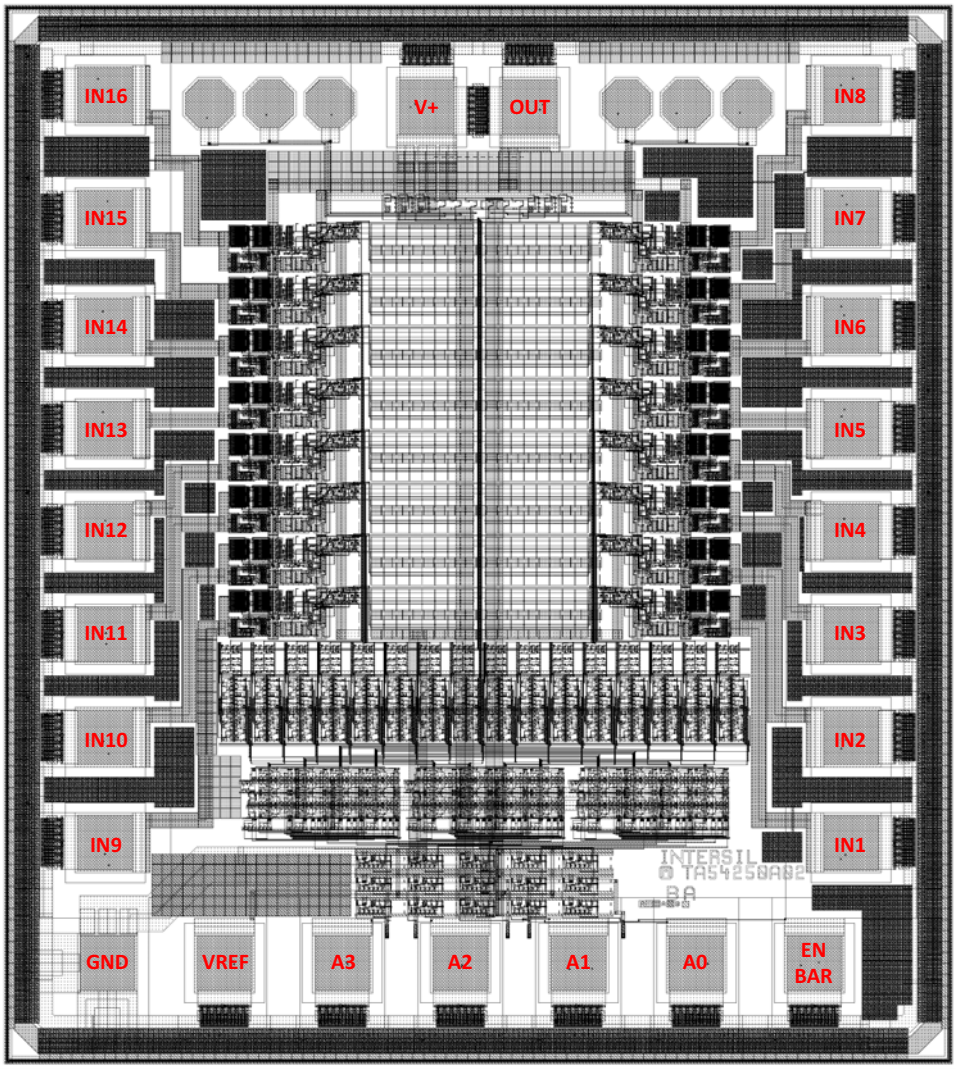


TABLE 3. ISL71830SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN8	P26	110	110	1693.925	1939.8
5	OUT	P28	110	110	1050.875	1915.8
6	V+	P1	110	110	844.875	1915.8
10	IN16	P4	110	110	201.8	1939.8
11	IN15	P5	110	110	201.8	1693.8
12	IN14	P6	110	110	201.8	1477.8
13	IN13	P7	110	110	201.8	1271.8
14	IN12	P8	110	110	201.8	1065.8
15	IN11	P9	110	110	201.8	859.8
16	IN10	P10	110	110	201.8	653.8
17	IN9	P11	110	110	201.8	442.8
18	GND	P12	110	110	206.225	201.8
19	VREF	P13	110	110	440.35	201.8
20	A3	P14	110	110	676.35	201.8
21	A2	P15	110	110	912.35	201.8
22	A1	P16	110	110	1148.35	201.8
23	A0	P17	110	110	1384.35	201.8
24	$\overline{EN}$	P18	110	110	1620.35	201.8
25	IN1	P19	110	110	1693.925	442.8
26	IN2	P20	110	110	1693.925	653.8
27	IN3	P21	110	110	1693.925	859.8
28	IN4	P22	110	110	1693.925	1065.8
29	IN5	P23	110	110	1693.925	1271.8
30	IN6	P24	110	110	1693.925	1477.8
31	IN7	P25	110	110	1693.925	1693.8

NOTE: Origin of coordinates is the bottom left of the die, near Pad 18.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
February 6, 2017	FN8758.4	Updated the note on Table 3 on page 18.
November 18, 2016	FN8758.3	Added ESD diagrams to the “Pin Descriptions” on page 3. Updated Related Literature section.
March 4, 2016	FN8758.2	Page 1 Features, changed the following: From: SEL/B immune to LET 60MeV • mg/cm^2 To: SEL/B immune to LET 60MeV • cm^2/mg
December 10, 2015	FN8758.1	Changed r_{ON} to $r_{DS(ON)}$ throughout datasheet Changed in Features on page 1 last item under “Radiation tolerance” “V^+ = 5V” to “V^+ = 6.5V” Changed in Description and Features on page 1 supply voltage from “3.3V to 5V” to “3V to 5.5V”. Removed ADDR throughout datasheet from: Pin Configuration from pins 14 through 17 on page 3 “Pin Descriptions” on page 3, “Absolute Maximum Ratings” on page 4 and Table 3 on page 18. Abs Max Section, page 4, changed: Maximum Supply Voltage (V+ to GND) (Note 5) . . . . . 7V TO: Maximum Supply Voltage (V+ to GND) (Note 5) . . . . . 6.5V Electrical Spec table: page 4 Changed TYP from 60 to 40 page 5 t_{BBM} changed TYP from 15 to 18 V_{CTE} changed TYP from 2 to 1.4 Swapped the "VEN = " statements between Off Isolation and Crosstalk. Off Isolation changed: From: 60dB (TYP) To: 60dB (MIN) and Crosstalk changed: From: 73dB (TYP) To: 73dB (MIN) page 6 Changed TYP from 60 to 70 page 7 tBBM changed TYP from 15 to 25 “Timing Diagrams” on page 8 Figures 5 and 7 changed 500 to 50Ω On page 7 added Truth table. Replaced die plot on page 17, changed VDD to V+. Page 18 X-Y Coordinates table, changed VDD to V+ Figure 7 changed 1000 on bottom right resistor to 100Ω. Y-Axis Changes: Figure 20: from ADDRESS DELAY (ns) to: t_{BMM} DELAY (ns) Figure 22: from ADDRESS DELAY (ns) to: t_{ENABLE} DELAY (ns) Figure 23: from ADDRESS DELAY (ns) to: $t_{DISABLE}$ DELAY (ns)
September 24, 2015	FN8758.0	Initial Release

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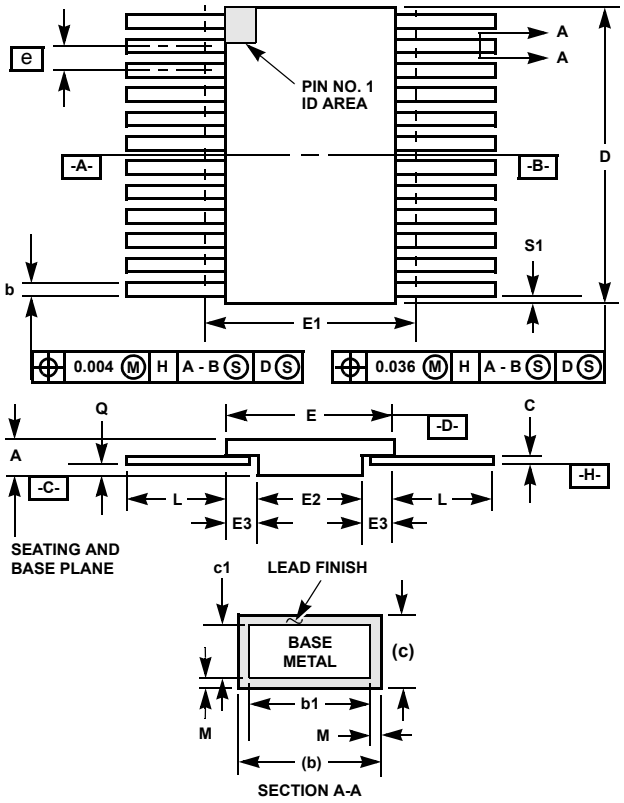
Ceramic Metal Seal Flatpack Packages (Flatpack)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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