

The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 June 2013.

INCH-POUND

MIL-PRF-19500/596K  
 17 April 2013  
 SUPERSEDING  
 MIL-PRF-19500/596J  
 14 April 2009

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT,  
 TRANSISTOR, N-CHANNEL, SILICON,  
 TYPES 2N7218, 2N7219, 2N7221, 2N7222, 2N7218U, 2N7219U,  
 2N7221U, AND 2N7222U, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum ratings ( $E_{AR}$  and  $E_{AS}$ ) and maximum avalanche current  $I_{AR}$ . Two levels of product assurance are provided for die (element evaluation).

1.2 Physical dimensions. See figure 1 (TO-254AA), figure 2 for JANHC and JANKC (die) dimensions, and figure 3 for surface mount (TO-267AB).

1.3 Maximum ratings. Unless otherwise specified,  $T_C = +25^\circ\text{C}$ .

Type	$P_T$ (1) $T_C = +25^\circ\text{C}$	$P_T$ $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	$V_{(BR)DSS}$ min $V_{GS} = 0$ $I_D = 1.0 \text{ mA dc}$	$I_{D1}$ (3) (4) $T_C = +25^\circ\text{C}$	$I_{D2}$ (3) (4) $T_C = +100^\circ\text{C}$	$I_S$	$I_{DM}$ (5)	$T_J$ and $T_{STG}$
	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u><math>^\circ\text{C}</math></u>
2N7218, 2N7218U	125	4	1.0	100	28	20	28	112	-55 to +150
2N7219, 2N7219U	125	4	1.0	200	18	11	18	72	-55 to +150
2N7221, 2N7221U	125	4	1.0	400	10	6	10	40	-55 to +150
2N7222, 2N7222U	125	4	1.0	500	8	5	8	32	-55 to +150

See notes next page.

\* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

1.3 Maximum ratings - continued.

Type	I <sub>AR</sub>	E <sub>AS</sub>	E <sub>AR</sub>	V <sub>(ISO)</sub> at 70,000 feet	V <sub>GS</sub>	r <sub>DS(on)</sub> max (6) V <sub>GS</sub> = 10 V dc I <sub>D</sub> = I <sub>D2</sub>	
						T <sub>J</sub> = +25°C	T <sub>J</sub> = +150°C
	<u>A</u>	<u>mj</u>	<u>mj</u>		<u>V dc</u>	<u>Ω</u>	<u>Ω</u>
2N7218, 2N7218U	28	250	12.5		±20	0.077	0.154
2N7219, 2N7219U	18	450	12.5		±20	0.18	0.387
2N7221, 2N7221U	10	650	12.5	400	±20	0.55	1.32
2N7222, 2N7222U	8	700	12.5	500	±20	0.85	2.04

- (1) Derate linearly 1.0 W/°C for T<sub>C</sub> > +25°C.
- (2) See figure 4, thermal impedance curves.
- (3) The following formula derives the maximum theoretical I<sub>D</sub> limit. I<sub>D</sub> is limited by package and internal wires and may be limited by pin diameter:

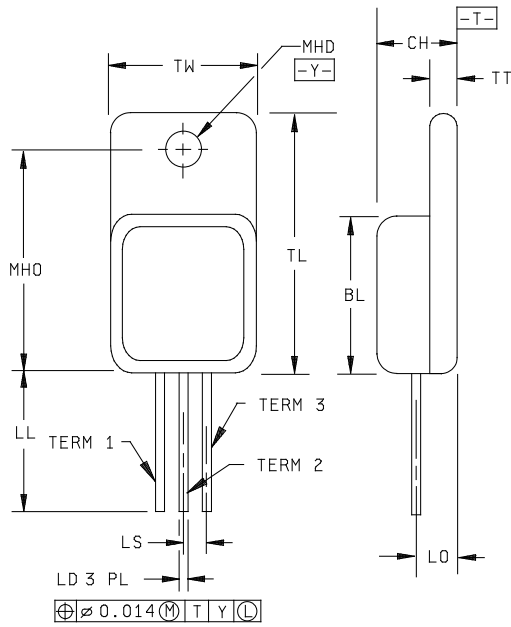
$$I_D = \sqrt{\frac{T_J \text{ max} - T_C}{(R_{\theta JC}) \times (R_{DS(ON)} \text{ at } T_{J \text{ max}})}}$$

- (4) See figure 5, maximum drain current graph.
- (5) I<sub>DM</sub> = 4 x I<sub>D1</sub> as calculated in note 3.
- (6) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. T<sub>C</sub> = +25°C (unless otherwise specified).

Type	Min V <sub>(BR)DSS</sub> V <sub>GS</sub> = 0 I <sub>D</sub> = 1.0 mA dc	V <sub>GS(th)1</sub> V <sub>DS</sub> ≥ V <sub>GS</sub> I <sub>D</sub> = 0.25 mA dc	Max I <sub>DSS1</sub> V <sub>GS</sub> = 0 V <sub>DS</sub> = 80 percent of rated V <sub>DS</sub>	Max r <sub>DS(on)1</sub> (1) I <sub>D</sub> = I <sub>D2</sub> V <sub>GS</sub> = 10 V
	<u>V dc</u>	<u>V dc</u>	<u>μA dc</u>	<u>Ohms</u>
		<u>Min</u> <u>Max</u>		
2N7218, 2N7218U	100	2.0      4.0	25	0.077
2N7219, 2N7219U	200	2.0      4.0	25	0.18
2N7221, 2N7221U	400	2.0      4.0	25	0.55
2N7222, 2N7222U	500	2.0      4.0	25	0.85

- (1) Pulsed (see 4.5.1).

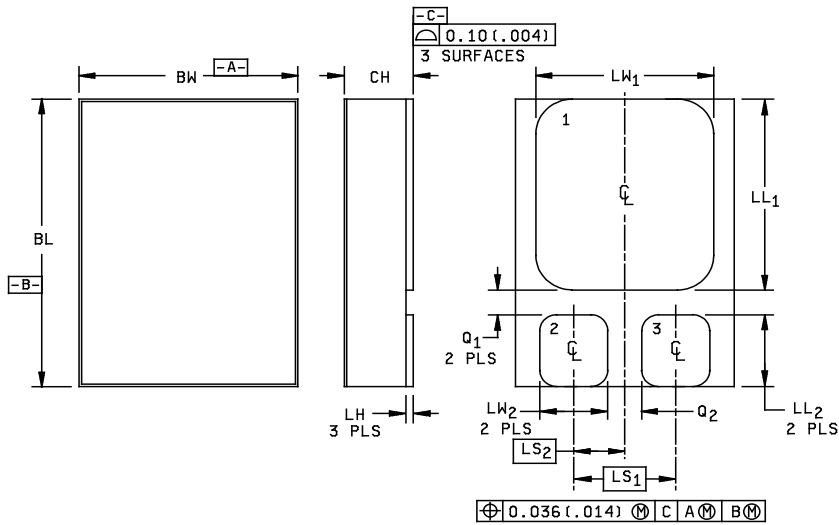


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	3, 4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	3, 4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7218, 2N7219, 2N7221, and 2N7222).

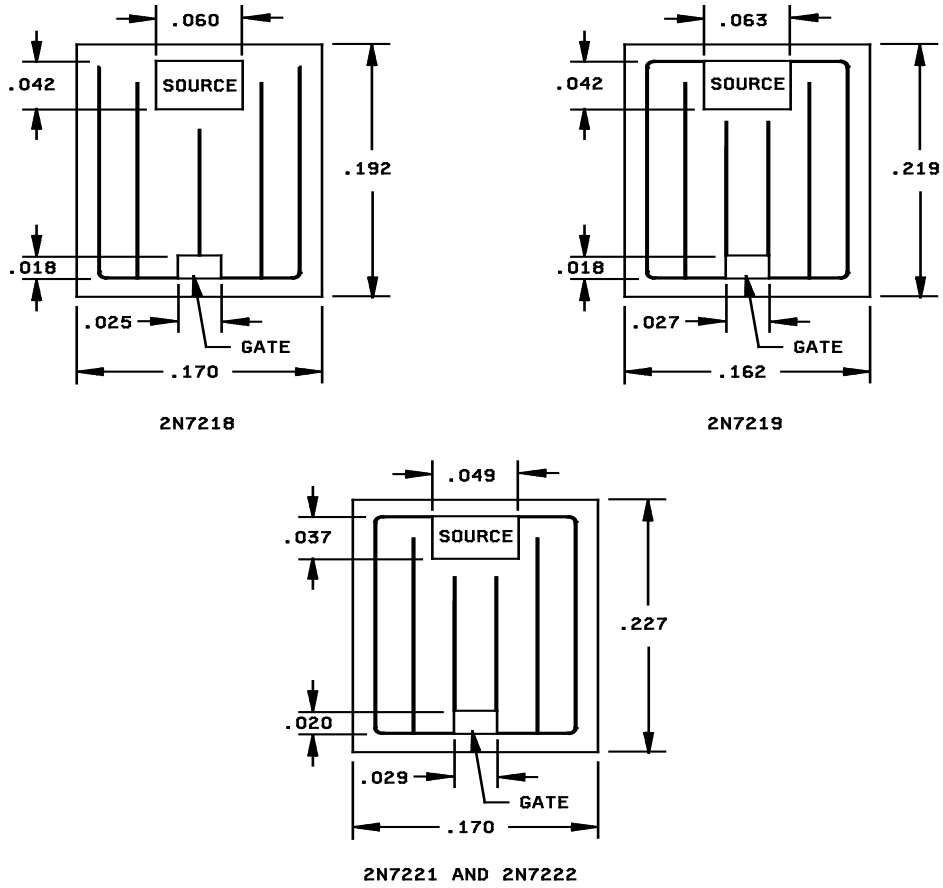


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL <sub>1</sub>	.410	.420	10.41	10.67
LL <sub>2</sub>	.152	.162	3.86	4.11
LS <sub>1</sub>	.210 BSC		5.33 BSC	
LS <sub>2</sub>	.105 BSC		2.67 BSC	
LW <sub>1</sub>	.370	.380	9.40	9.65
LW <sub>2</sub>	.135	.145	3.43	3.68
Q <sub>1</sub>	.030		0.76	
Q <sub>2</sub>	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 2. Dimensions and configuration of surface mount package outline (TO-267AB), 2N7218U, 2N7219U, 2N7221U, and 2N7222U.



Inches	mm	Inches	mm	Inches	mm
.018	0.46	.037	0.94	.162	4.11
.020	0.51	.042	1.07	.170	4.32
.025	0.64	.049	1.24	.192	4.88
.027	0.69	.060	1.52	.219	5.56
.029	0.74	.063	1.60	.227	5.77

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is  $\pm 0.005$  inch (0.13 mm).
4. The physical characteristics of the die thickness are .0187 inch (0.475 mm). The back metals are chromium, nickel, and silver. The top metal is aluminum and the back contact is the drain.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.
6. See 6.4 for ordering information.

FIGURE 3. JANHC and JANKC (A-version) die dimensions.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or <https://assist.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 (TO-254AA), 2 (TO-267AB, surface mount), and 3 (die) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent  $AL_2O_3$  (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation or finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling procedures shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source.  $R \leq 100 \text{ k}\Omega$ , whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500, except at the option of the manufacturer, the country of origin and/or the manufacturers identification may be omitted from the body of the transistor.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV level
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2)
(3)	Method 3470 of MIL-STD-750. (see 4.3.3)	Method 3470 of MIL-STD-750. (see 4.3.3)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
9	$I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , subgroup 2 of table I herein;	Subgroup 2 of table I herein
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	$I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , $r_{DS(on)1}$ , $V_{GS(th)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater.	$I_{GSSF1}$ , $I_{GSSR1}$ , $I_{DSS1}$ , $r_{DS(on)1}$ , $V_{GS(th)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A or $T_A = +175^\circ\text{C}$ and $t = 48$ hours
13	Subgroup 2 and 3 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ $\mu$ A dc or $\pm 100$ percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.
* 17	Method 1081 of MIL-STD-750 (see 4.3.5) Endpoints: Subgroup 2 of table I herein	Method 1081 of MIL-STD-750 (see 4.3.5) Endpoints: Subgroup 2 of table I herein

(1) At the end of the test program,  $I_{GSSF1}$ ,  $I_{GSSR1}$ , and  $I_{DSS1}$  are measured.

(2) An out-of-family program to characterize  $I_{GSSF1}$ ,  $I_{GSSR1}$ ,  $I_{DSS1}$ , and  $V_{GS(th)1}$  shall be invoked.

(3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.



4.3.1 Screening (JANHC and JANKC). Screening of die shall be in accordance with MIL-PRF-19500. As a minimum die, shall be 100 percent probed in accordance with table I, subgroup 2 except test current shall not exceed 20 amperes.

4.3.2 Gate stress test. Apply  $V_{GS} = 30$  V minimum for  $t = 250$   $\mu$ s minimum.

4.3.3 Single pulse avalanche energy ( $E_{AS}$ ).

- a. Peak current ( $I_{AS}$ )..... $I_{D1}$ .
- b. Peak gate voltage ( $V_{GS}$ )..... 10 V.
- c. Gate to source resistor ( $R_{GS}$ ) ..... $25 \leq R_{GS} \leq 200 \Omega$ .
- d. Initial case temperature ..... $+25^{\circ}\text{C} +10^{\circ}\text{C}, -5^{\circ}\text{C}$ .
- e. Inductance:..... $\left[ \frac{2E_{AS}}{(I_{D1})^2} \right] \left[ \frac{V_{BR} - V_{DD}}{V_{BR}} \right]$  mH minimum.
- f. Number of pulses to be applied ..... 1 pulse minimum.
- g. Supply voltage ( $V_{DD}$ ).....50 V, 25 V for 100 V devices.

4.3.4 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$ , (and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 30 - 60  $\mu$ s max. See table II, group E, subgroup 4 herein.

\* 4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage.....900V DC
- b. Duration of application of test voltage.....15 seconds (min)
- c. Points of application of test voltage.....All leads to case (bunch connection)
- d. Method of connection.....Mechanical
- e. Kilovolt-ampere rating of high voltage source.....1200V/1.0 mA (min)
- f. Maximum leakage current.....1.0 mA
- g. Voltage ramp up time.....500V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein.

\* 4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
* B4	1042	Test condition D; the heating cycle shall be 1 minute minimum. No heat sink or forced air cooling on the device shall be permitted during the cycle.
B5	1042	A separate sample may be pulled for each test. Accelerated steady-state reverse bias, test condition A, $V_{DS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 120$ hours, read and record $V_{(BR)DSS}$ (pre and post at $1 \text{ mA} = I_D$ . Read and record $I_{DSS}$ (pre and post). Deltas for $V_{(BR)DSS}$ shall not exceed 10 percent and $I_{DSS}$ shall not exceed $25 \mu\text{A}$ .  Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 24$ hours.
B5	2037	Bond strength; test condition D.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G.
B3	1042	Test condition D, 2,000 cycles minimum. The heating cycle shall be 1 minute minimum.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Tension: Test condition A; weight = 10 lbs, $t = 10$ s (not applicable to "U" suffix version).
C5	3161	See 4.3.4, $R_{\theta JC(max)}$ shall be $1.0^\circ\text{C/W}$ .
* C6	1042	Test condition D. The heating cycle shall be 1 minute minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.4	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3407	Bias condition C, $V_{GS} = 0$ V, $I_D = 1$ mA dc	$V_{(BR)DSS}$	100 200 400 500		V dc V dc V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = .25$ mA	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	Bias condition C, $V_{GS} = 20$ V dc, $V_{DS} = 0$	$I_{GSSF1}$		100	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20$ V dc, $V_{DS} = 0$	$I_{GSSR1}$		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ , $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS1}$		25	μA dc
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = 10$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)1}$		0.077 0.18 0.55 0.85	Ω Ω Ω Ω
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = 10$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D1}$ (see 1.3)	$r_{DS(on)2}$		0.125 0.25 0.70 0.95	Ω Ω Ω Ω

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward voltage (source drain diode)	4011	$V_{GS} = 0$ , $I_D = \text{rated } I_{D1}$ , pulsed (see 4.5.1)	$V_{SD}$		1.5	V
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	Bias condition C, $V_{GS} = 20$ V dc, $V_{DS} = 0$	$I_{GSSF2}$		200	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20$ V dc, $V_{DS} = 0$	$I_{GSSR2}$		-200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ , $V_{DS} = 100$ percent of rated $V_{DS}$	$I_{DSS2}$		1.0	mA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ , $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS3}$		0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 0.25$ mA	$V_{GS(th)2}$	1.0		V dc
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = 10$ V dc, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)3}$		0.24 0.48 1.44 2.04	$\Omega$ $\Omega$ $\Omega$ $\Omega$
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 0.25$ mA	$V_{GS(th)3}$		5.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$ (see 1.3), $V_{GS} = 10 \text{ V}$ dc, gate drive impedance = $9.1 \Omega$ , $V_{DD} = 50$ percent of $V_{BR(DSS)}$				
Turn-on delay time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_{d(on)}$		21 20 25 21	ns ns ns ns
Rise time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_r$		105 105 92 73	ns ns ns ns
Turn-off delay time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_{d(off)}$		64 58 79 72	ns ns ns ns
Fall time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_f$		65 67 58 51	ns ns ns ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 6; $t_p = 10 \text{ ms}$ , $V_{DS} = 80$ percent of rated $V_{BR(DSS)}$ , $V_{DS} = 200 \text{ V}$ maximum				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 6</u>						
Not applicable						

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7218, 2N7218U					59	nC
2N7219, 2N7219U					60	nC
2N7221, 2N7221U					65	nC
2N7222, 2N7222U					68.5	nC
Gate to source charge			$Q_{gs}$			
2N7218, 2N7218U					16	nC
2N7219, 2N7219U					14.6	nC
2N7221, 2N7221U					14.0	nC
2N7222, 2N7222U					12.5	nC
Gate to drain charge			$Q_{gd}$			
2N7218, 2N7218U					30.7	nC
2N7219, 2N7219U					37.6	nC
2N7221, 2N7221U					40.5	nC
2N7222, 2N7222U					42.4	nC
Reverse recovery time	3473	$d_i/d_t \leq 100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq 30 \text{ V}$ , $I_D = I_{D1}$ , (see 1.3)	$t_{rr}$			
2N7218, 2N7218U					400	ns
2N7219, 2N7219U					500	ns
2N7221, 2N7221U					600	ns
2N7222, 2N7222U					700	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroups 2 and 6.
- Group E, subgroup 1.

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\* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	-55 to 150°C, 500 cycles	
Hermetic seal	1071	As applicable.	
Fine leak			
Gross leak			
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
<u>Subgroup 5 2/</u>			3 devices c = 0
Barometric pressure test	1001	Condition C, $V_{(ISO)} = V_{DS}$	
2N7221, 2N7221U		$V_{DS} = 400$ V dc	
2N7222, 2N7222U		$V_{DS} = 500$ V dc	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

See footnotes at end of table.

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 11</u> Repetitive avalanche energy  Electrical measurements	3469	Peak current $I_{AR} = I_D$ ; peak gate voltage $V_{GS} = 10$ V; gate to source resistor, $R_{GS} 25 \leq R_{GS} \leq 200$ ohms Temperature = $T_J = +150^\circ\text{C} +0, -10^\circ\text{C}$ Inductance = $\left[ \frac{2E_{AR}}{(I_{D1})^2} \right] \left[ \frac{V_{BR} - V_{DD}}{V_{BR}} \right] \text{ mH minimum}$ Number of pulses to be applied = $3.6 \times 10^8$ ; supply voltage ( $V_{DD}$ ) = 50 V, time in avalanche = 2 $\mu\text{s}$ min., 20 $\mu\text{s}$ max. frequency = 500 Hz minimum.  See table I, subgroup 2	5 devices c = 0

1/ A separate sample for each test may be pulled.

2/ Not required for 2N7218, 2N7218U, 2N7219, and 2N7219U.



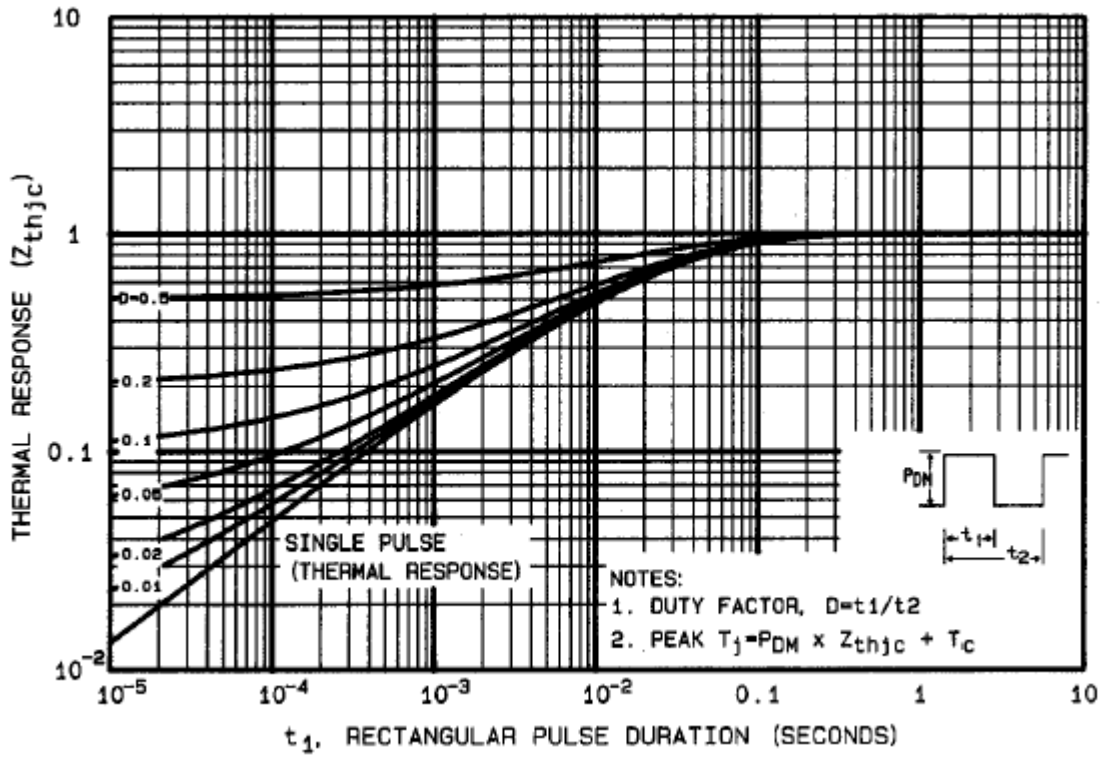


FIGURE 4. Thermal impedance.

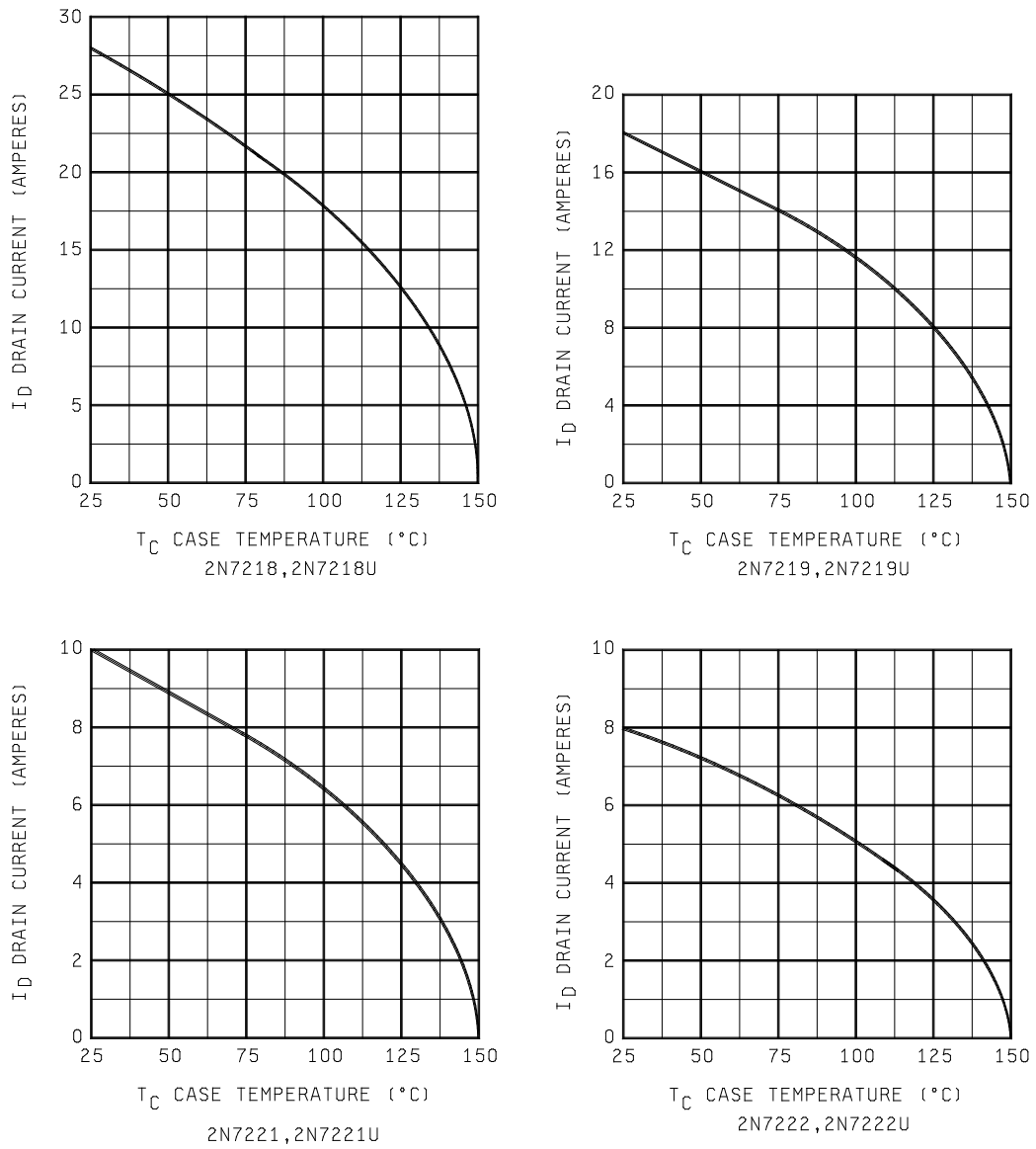


FIGURE 5. Maximum drain current versus case temperature graphs.

2N7218, 2N7218U

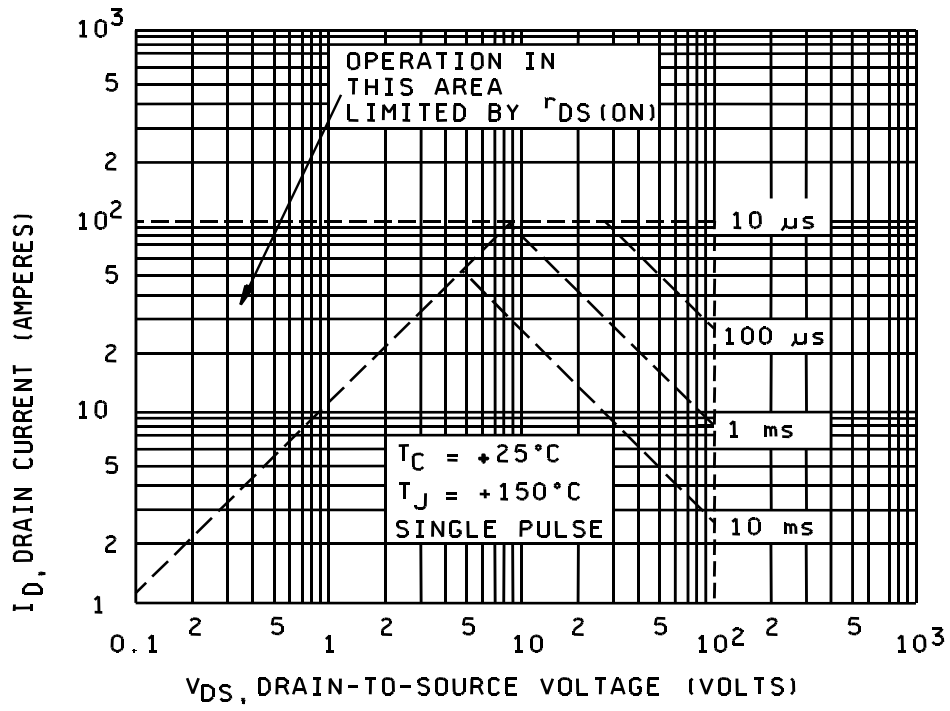


FIGURE 6. Safe operating area.

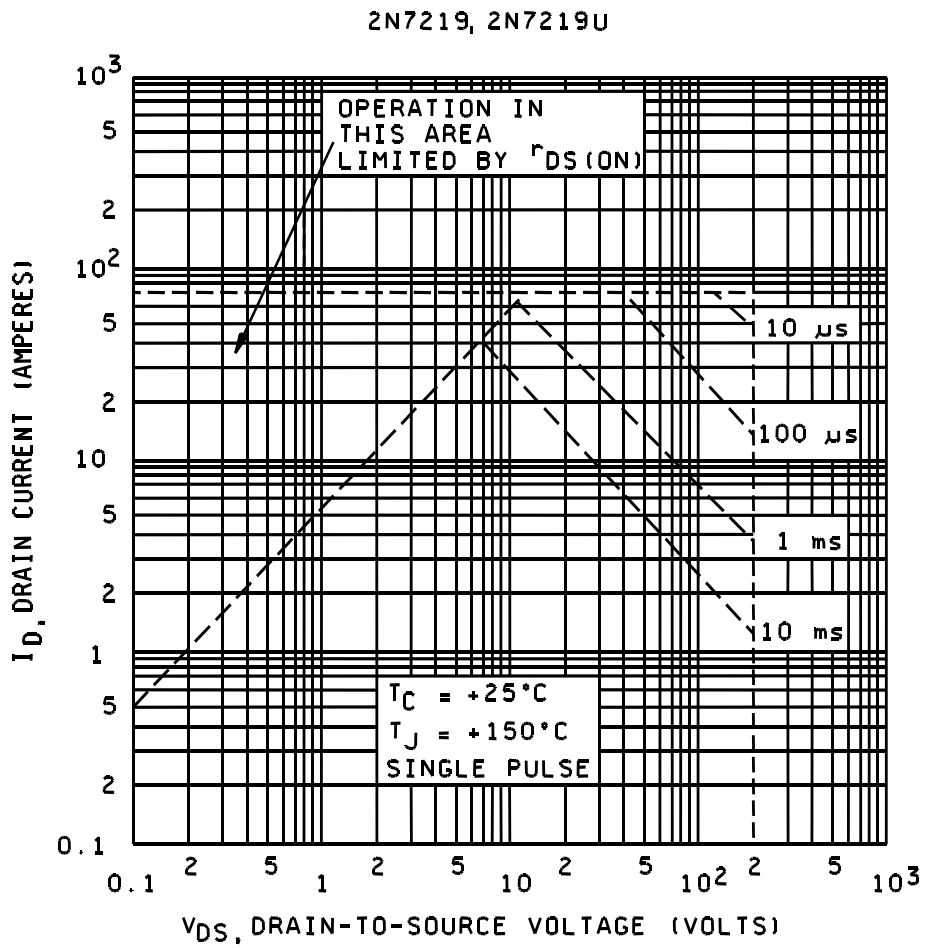


FIGURE 6. Safe operating area - Continued.

2N7221, 2N7221U

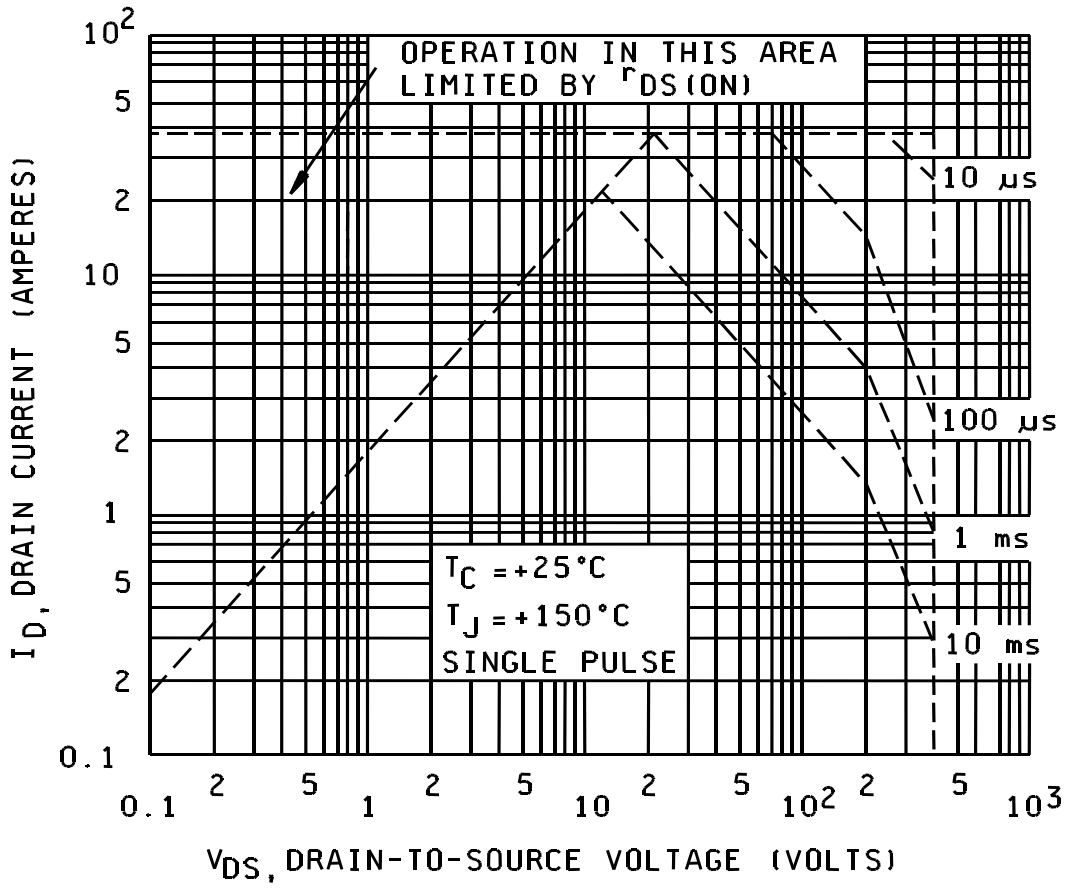


FIGURE 6. Safe operating area - Continued.

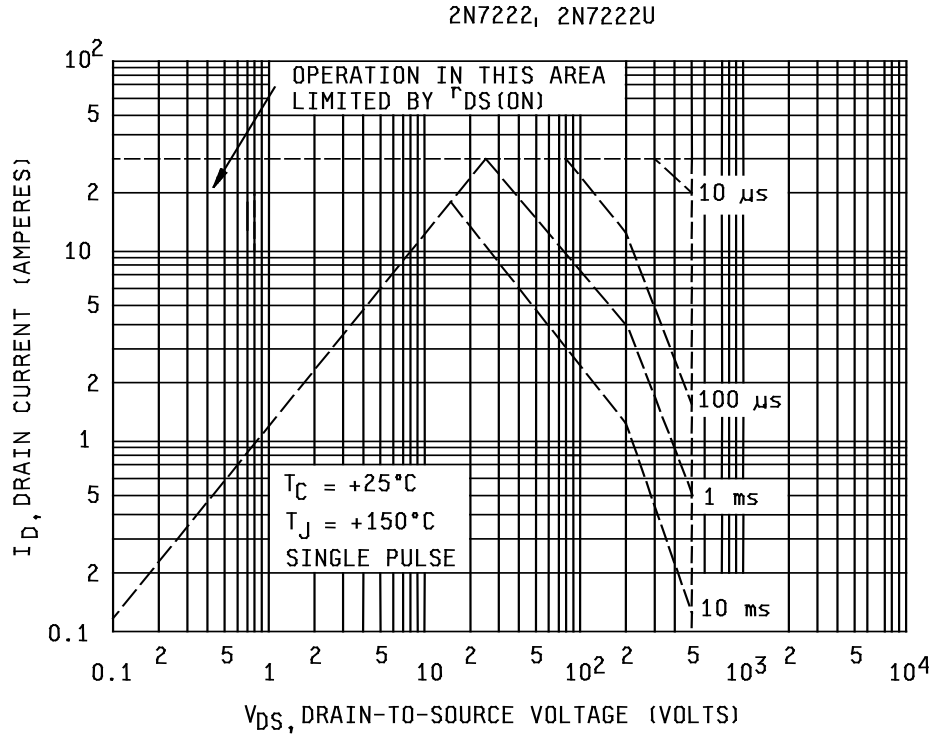


FIGURE 6. Safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead formation and finish (see 3.4.1).
- d. Product assurance level and type designator.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <http://assist.dla.mil>.

6.4 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example JANHCA2N7218) will be identified on the QML.

JANC ordering information		
Military PIN	Manufacturer	
	59993	59993
2N7218	JANHCA2N7218	JANKCA2N7218
2N7219	JANHCA2N7219	JANKCA2N7219
2N7221	JANHCA2N7221	JANKCA2N7221
2N7222	JANHCA2N7222	JANKCA2N7222

6.5 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable as a substitute for the military PIN.

Military PIN	Manufacturer's CAGE	Manufacturer's and user's PIN
2N7218	59993	IRFM 140
2N7219	59993	IRFM 240
2N7221	59993	IRFM 340
2N7222	59993	IRFM 440
2N7218U	59993	IRFN 140
2N7219U	59993	IRFN 240
2N7221U	59993	IRFN 340
2N7222U	59993	IRFN 440

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

## Custodians:

Army - CR  
Navy - EC  
Air Force - 85  
NASA - NA  
DLA - CC

## Preparing activity:

DLA - CC

(Project 5961-2013-005)

## Review activities:

Army - MI, SM  
Navy - AS, MC  
Air Force - 19

- \* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.



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