

4N51, 4N52
67023 4N53, 4N54 HERMETIC , NUMERIC AND HEXADECIMAL
DISPLAYS



11/19/03

Features:

- Conforms to MIL-PRF-87157
- Three character options
Numeric, Hexadecimal or Over range
- 4 X 7 dot matrix character
- Memory latch/decoder/driver is TTL compatible
- Categorized for luminous intensity

Applications:

- High reliability systems
- Instrumentation panels
- Communication equipment
- Medical equipment
- Harsh environments

DESCRIPTION

The **4N51, 4N52, 4N53 and 4N54** series are solid state numeric and hexadecimal displays for use in high reliability applications. The displays feature an on-board decoder/driver and memory (except 4N53). These displays are hermetically sealed and conform to MIL-PRF-87157, the general specification for light emitting diode displays. The character height is 0.290" (7.37mm).

The 4N51 is a numeric display which decodes positive BCD logic into the numbers "0-9", a "-" sign, a right-hand decimal point, and a test pattern (all LED's on).

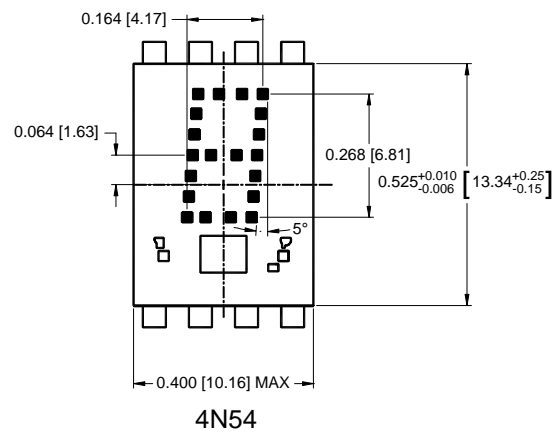
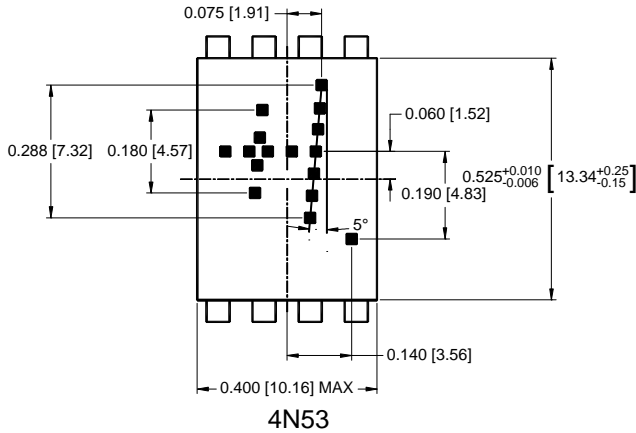
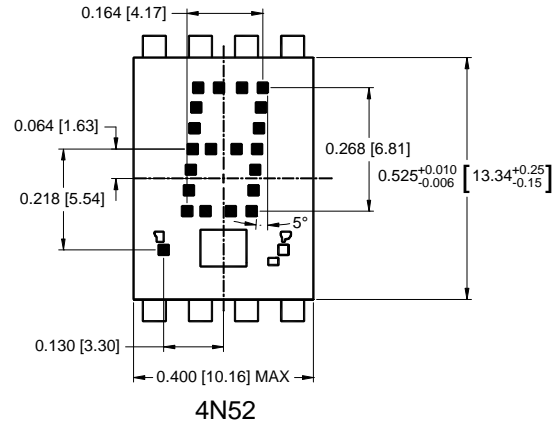
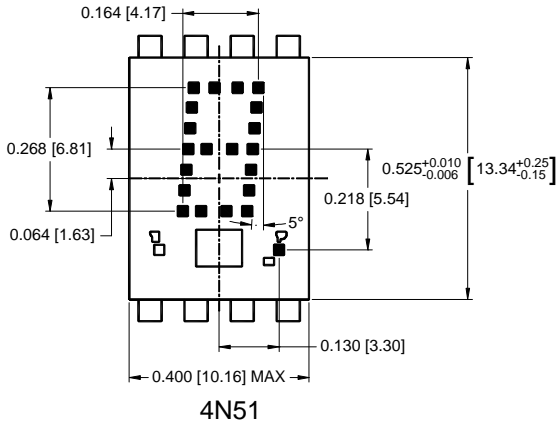
The 4N52 is the same as the 4N51, but the decimal point is located on the left side of the device.

The 4N53 is an over range device which displays "±1" and a right-hand decimal point. This display is typically driven using external switching transistors.

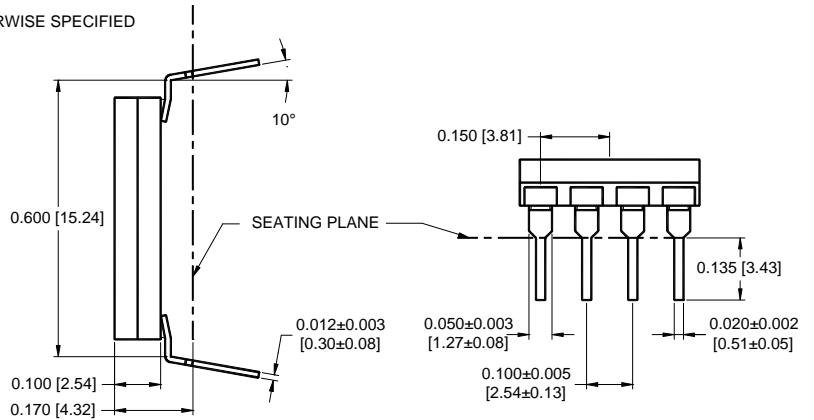
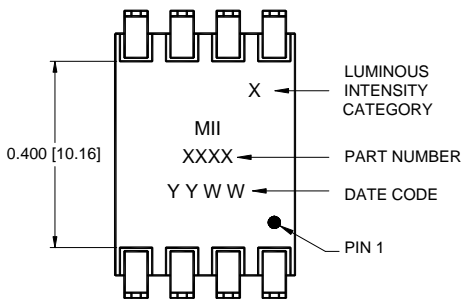
The 4N54 is a hexadecimal display which decodes positive BCD logic into 16 characters "0-9, A-F". Input is provided to blank the display (all LED's off) without losing the contents of the memory.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------|
| Supply Voltage (4N51, 4N52, 4N54) | -0.5 V to 7 V |
| Voltage Applied to Input Logic, DP and Enable Pins | -0.5 V to 7 V |
| Voltage Applied to Blanking Input (4N54 only)..... | -0.5 V to 7 V |
| Forward Current, Each LED (4N53 only)..... | 10 mA |
| Reverse Voltage, Each LED (4N53 only) | 4 V |
| Storage Temperature | -65°C to +125°C |
| Operating Free-Air Temperature Range..... | -55°C to +100°C |
| Lead Solder Temperature (10seconds, 1/16" below seating plane)..... | 260°C |



ALL TOLERANCES ARE ± 0.008 [0.20] UNLESS OTHERWISE SPECIFIED



ALL TOLERANCES ARE ± 0.015 UNLESS OTHERWISE SPECIFIED

ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].

*JEDEC Registered Data

**4N51, 4N52,
67023 4N53, 4N54**

HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS

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***ELECTRICAL OPTICAL CHARACTERISTICS**

T_A = -55°C to +100°C unless otherwise specified.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS | NOTE |
|---|-----------------|----------------------|--------------------------|--------------------------|-------|---|------|
| Supply Current 4N51 4N52 4N54 | I _{CC} | | 112 112 112 | 170 170 170 | mA | V _{CC} = 5.5V Numeral 5 and DP lighted | 1 |
| Power Dissipation 4N51 4N52 4N53 4N54 | P _T | | 560 560 280 560 | 935 935 320 935 | mW | V _{CC} = 5.5V Numeral 5 and DP lighted | 1, 3 |
| Luminous Intensity per LED 4N51 4N52 4N53 4N54 | I _V | 40 40 45 40 | 85 85 85 85 | | μcd | V _{CC} = 5V, T _A = 25°C V _{CC} = 5V, T _A = 25°C I _F = 10mA, T _A = 25°C V _{CC} = 5V, T _A = 25°C | 2 |
| Forward Voltage per LED 4N53 | V _F | | 1.6 | 2.0 | V | I _F = 10mA | |
| Logic Low-Level Input Voltage 4N51 4N52 4N54 | V _{IL} | | | 0.8 0.8 0.8 | V | V _{CC} = 4.5V | |
| Logic High-Level Input Voltage 4N51 4N52 4N54 | V _{IH} | 2 2 2 | | | V | V _{CC} = 4.5V | |
| Enable Low-Voltage; Data Being Entered 4N51 4N52 4N54 | V _{EL} | | | 0.8 0.8 0.8 | V | V _{CC} = 4.5V | |
| Enable High-Voltage; data not being entered 4N51 4N52 4N54 | V _{EH} | 2 2 2 | | | V | V _{CC} = 4.5V | |
| Blanking Low-Voltage display not blanked 4N54 | V _{BL} | | | 0.8 | V | V _{CC} = 4.5V | |
| Blanking High-Voltage display not blanked 4N54 | V _{BH} | 3.5 | | | V | V _{CC} = 4.5V | |
| Leak Rate ALL | | | | 5x10 ⁻⁸ | | cc/sec | |
| Blanking Low-Level Input Current 4N54 | I _{BL} | | | 50 | mA | V _{CC} = 5.5V, V _{BL} = 0.8V | |
| Blanking High-Level Input Current 4N54 | I _{BH} | | | 1.0 | mA | V _{CC} = 5.5V, V _{BH} = 4.5V | |
| Logic Low-Level Input Current 4N51 4N52 4N54 | I _{IL} | | | -1.6 | mA | V _{CC} = 5.5V, V _{IL} = 0.4V | |
| Logic High-Level Input Current 4N51 4N52 4N54 | I _{IH} | | | +100 | μA | V _{CC} = 5.5V, V _{IH} = 2.4V | |
| Enable Low-Level Input Current 4N51 4N52 4N54 | I _{EL} | | | -1.6 | mA | V _{CC} = 5.5V, V _{EL} = 0.4V | |
| Enable High-Level Input Current 4N51 4N52 4N54 | I _{EH} | | | +130 | μA | V _{CC} = 5.5V, V _{EH} = 2.4V | |
| Wavelength at Peak Emission ALL | λ _P | | 655 | | nm | T _A = 25°C | |
| Dominant Wavelength ALL | d | | 640 | | | T _A = 25°C | 2 |
| Forward Voltage per LED 4N53 | V _F | | 1.6 | 2.0 | V | I _F = 10mA | |
| Weight ALL | | | 1 | | gm | | |

NOTES:

1. All typical values at V_{CC} = 5.0 volts, t_A = 25°C.
2. The dominant wavelength, λ_d is a single wavelength that defines the saturated color of monochromatic light, as derived from the CIE chromaticity diagram.
3. For 4N53 test conditions, I_F = 10mA, all diodes lit.

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4N51, 4N52, 4N54 Logic

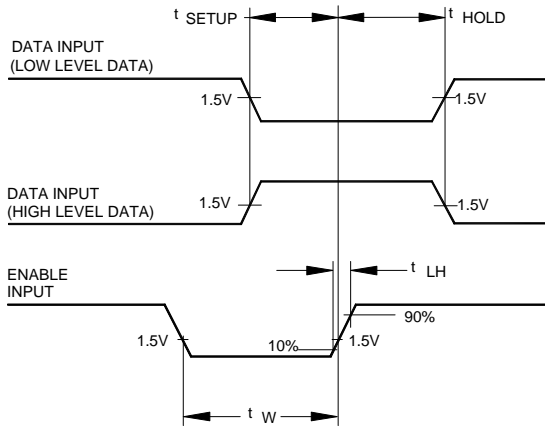


FIGURE 1. Timing Diagram of 4N51, 4N52 and 4N54 Series Logic

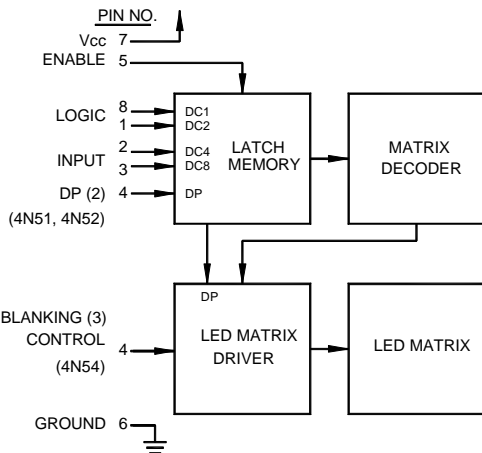


FIGURE 2. Block Diagram of 4N51, 4N52 and 4N54 Series Logic

| TRUTH TABLE | | | | | | |
|----------------------------|----------------|----------------|----------------|-------------|---------------------|--|
| BCD DATA ⁽¹⁾ | | | | 4N51/4N52 | 4N54 | |
| X ₈ | X ₄ | X ₂ | X ₁ | | | |
| L | L | L | L | 0 | 0 | |
| L | L | L | H | 1 | 1 | |
| L | L | H | L | 2 | 2 | |
| L | L | H | H | 3 | 3 | |
| L | H | L | L | 4 | 4 | |
| L | H | L | H | 5 | 5 | |
| L | H | H | L | 6 | 6 | |
| L | H | H | H | 7 | 7 | |
| H | L | L | L | 8 | 8 | |
| H | L | L | H | 9 | 9 | |
| H | L | H | L | ⏏ | A | |
| H | L | H | H | (BLANK) | B | |
| H | H | L | L | (BLANK) | C | |
| H | H | L | H | | D | |
| H | H | H | L | (BLANK) | E | |
| H | H | H | H | (BLANK) | F | |
| DECIMAL PT. ⁽²⁾ | | | | ON | V _{DP} = L | |
| | | | | OFF | V _{DP} = H | |
| ENABLE ⁽¹⁾ | | | | LOAD DATA | V _E = L | |
| | | | | LATCH DATA | V _E = H | |
| BLANKING ⁽³⁾ | | | | DISPLAY ON | V _B = L | |
| | | | | DISPLAY OFF | V _B = H | |

NOTES:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon memory.

4N53 Over Range Character

| PIN | FUNCTION |
|-----|-------------|
| 1 | Plus |
| 2 | Numeral One |
| 3 | Numeral One |
| 4 | DP |
| 5 | Open |
| 6 | Open |
| 7 | Vcc |
| 8 | Minus/Plus |

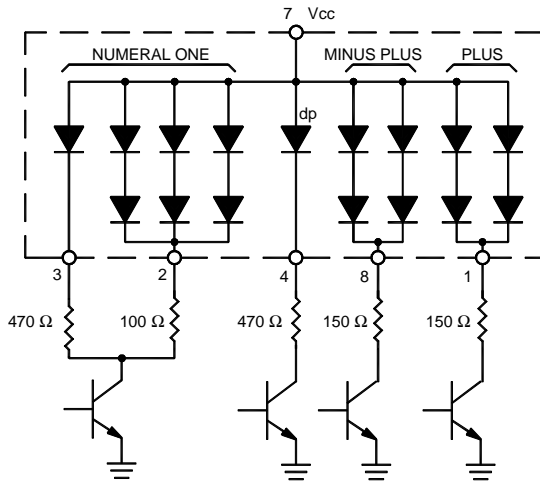


FIGURE 3. Typical Driving Circuit

TRUTH TABLE FOR TYPICAL DRIVING CIRCUIT

| CHARACTER | PIN | | | |
|---------------|-----|-----|---|---|
| | 1 | 2,3 | 4 | 8 |
| + | H | X | X | H |
| - | L | X | X | H |
| 1 | X | H | X | X |
| DECIMAL POINT | X | X | H | X |
| BLANK | L | L | L | L |

NOTES:

- L: Line switching transistor in figure 3 cutoff.
 H: Line transistor in figure 3 saturated.
 X: Don't Care.

***RECOMMENDED OPERATING CONDITIONS:**

| PARAMETER | | SYMBOL | MIN | MAX | UNITS |
|--|------|--------------------|-----|-----|-------|
| Supply Voltage | 4N51 | V _{CC} | 4.5 | 5.5 | V |
| | 4N52 | | 4.5 | 5.5 | V |
| | 4N53 | | NA | NA | NA |
| | 4N54 | | 4.5 | 5.5 | V |
| Operating Temperature | ALL | T _A | -55 | 100 | °C |
| Enable Pulse Width | 4N51 | t _W | 100 | | Ns |
| | 4N52 | | | | |
| | 4N54 | | | | |
| Time data must be held before positive transition of enable line | 4N51 | t _{SETUP} | 50 | | ns |
| | 4N52 | | | | |
| | 4N54 | | | | |
| Time data must be held after positive transition of enable line | 4N51 | t _{HOLD} | 50 | | ns |
| | 4N52 | | | | |
| | 4N54 | | | | |
| Enable pulse rise time | 4N51 | t _{TLH} | | 200 | ns |
| | 4N52 | | | | |
| | 4N54 | | | | |
| Forward Current | 4N53 | I _F | 5 | 10 | mA |

SELECTION GUIDE

| | |
|------------|--------------------------------|
| 67023-001 | 4N51 Commercial |
| 67023-011 | 4N51 Military Temp. Range |
| 67023-101 | 4N51 Screened, TXV level |
| 67023-101C | 4N51 DSCC P/N JM87157/00101AXX |
| 67023-002 | 4N52 Commercial |
| 67023-012 | 4N52 Military Temp. Range |
| 67023-102 | 4N52 Screened, TXV level |
| 67023-102C | 4N52 DSCC P/N JM87157/00102AXX |
| 67023-003 | 4N53 Commercial |
| 67023-013 | 4N53 Military Temp. Range |
| 67023-103 | 4N53 Screened, TXV level |
| 67023-103C | 4N53 DSCC P/N JM87157/00103AXX |
| 67023-004 | 4N54 Commercial |
| 67023-014 | 4N54 Military Temp. Range |
| 67023-104 | 4N54 Screened, TXV level |
| 67023-104C | 4N54 DSCC P/N JM87157/00104AXX |

NOTES:

1. When ordering DSCC part numbers, you may order by the MII part number or the DSCC part number.
2. The first X at the end of M87157/0010XA[X]X designates lead finish. In place of the X use A for hot solder dip or C for gold finish.
3. Second X at the end of the M87157/0010XA[X]X designates luminous intensity code. In place of the X use C thru K to indicate desired intensity level.

*JEDEC Registered Data

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