LCD TFT Module Specification

Riverdi

our pixels behave

RVT28AETNWC00

LCD TFT Datasheet

Rev.1.1

2015-06-24

ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally white	/
Size	2.83	Inch
Viewing Direction	6:00 (without image inversion)	O' Clock
Gray Scale Inversion Direction	12:00	O' Clock
LCM (W × H × D)	50.20 x 69.30 x 4.60	mm3
Active Area (W × H)	43.20 × 57.60	mm2
Dot Pitch (W × H)	0.18 × 0.18	mm2
Number Of Dots	240 x (RGB) × 320	/
Driver IC	ILI9341	/
Backlight Type	4 LEDs	/
Surface Luminance	255	cd/m2
Interface Type	CPU/RGB/SPI	/
Color Depth	65K/262K	/
Pixel Arrangement	RGB Vertical Stripe	/
Surface Treatment	Clear	
Input Voltage	2.8	V
With/Without TSP	Projected Capacitive Touch Panel	/
Weight	28.70	g

Note 1: RoHS compliant

Note 2: LCM weight tolerance: ± 5%.

REVISION RECORD

REVNO.	REVDATE	CONTENTS	REMARKS
1.0	2015-03-13	Initial Release	
1.1	2015-06-24	Update viewing direction	

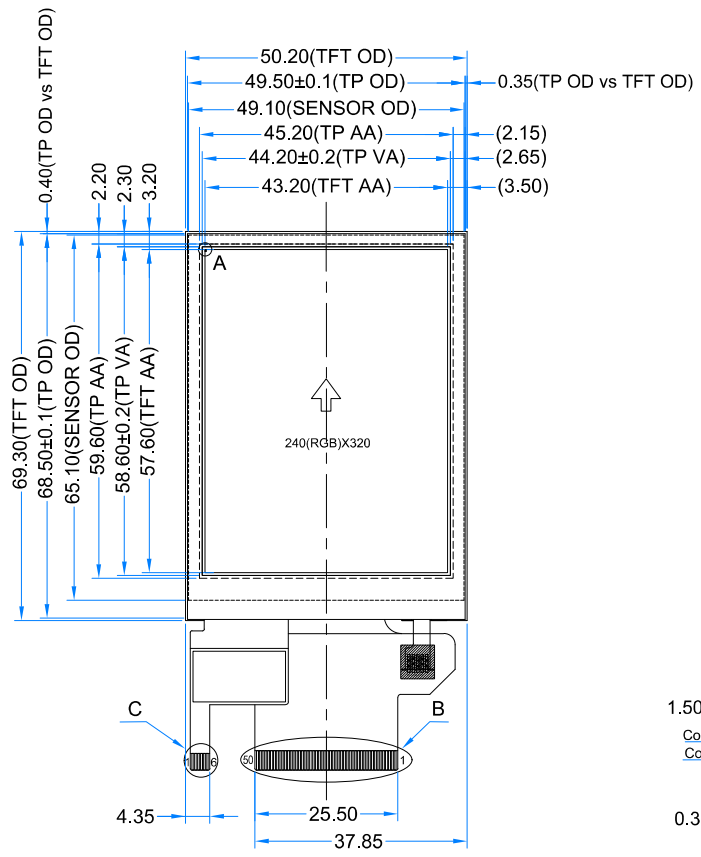
CONTENTS

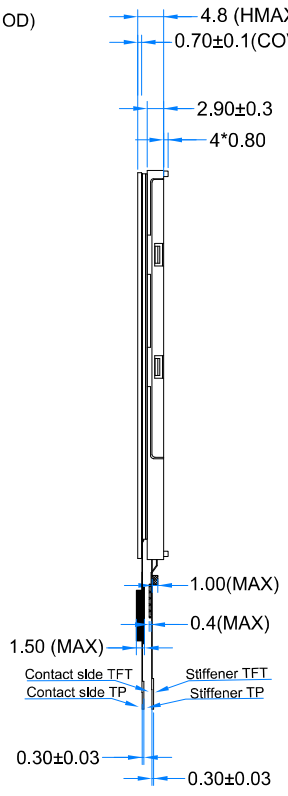
1 MODULE CLASSIFICATION INFORMATION

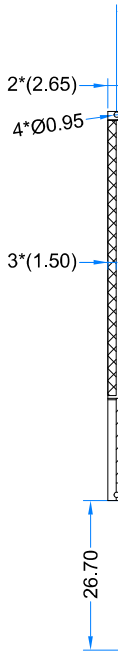
RV	T	28	A	E	T	N	W	C	00
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.

1.	**BRAND**	**RV** – Riverdi
2.	**PRODUCT TYPE**	**T – TFT Standard** **F** – TFT Custom
3.	**DISPLAY SIZE**	**28 – 2.83”** **35** – 3.5” **43** – 4.3” **70** – 7.0”
4.	**MODEL SERIAL NO.**	**A (A-Z)**
5.	**RESOLUTION**	**E– 240x320 px**
6.	**INTERFACE**	**T – TFT LCD, RGB** **L** – TFT LCD, LVDS **C** – TFT + Controller
7.	**FRAME**	**N – No Frame** **F –** Mounting Frame
8.	**BACKLIGHT TYPE**	**W – LED White**
9.	**TOUCH PANEL**	**N** – No Touch Panel **R –** Resistive Touch Panel **C – Capacitive Touch Panel**
10.	**VERSION**	**00(00-99)**

TFT PINOUT	
1	LEDK
2	LEDA1
3	LEDA2
4	LEDA3
5	LEDA4
6	IM0
7	IM1
8	IM2
9	IM3
10	RESET
11	VSYNC
12	HSYNC
13	DOTCLK
14	DE
15	DB17
16	DB16
17	DB15
18	DB14
19	DB13
20	DB12
21	DB11
22	DB10
23	DB9
24	DB8
25	DB7
26	DB6
27	DB5
28	DB4
29	DB3
30	DB2
31	DB1
32	DB0
33	SDO
34	SDI
35	RD
36	WRX(D/CX)
37	D/CX(SCL)
38	CSX
39	TE
40	VDDI
41	VDDI
42	VCI
43	GND
44	NC
45	NC
46	NC
47	NC
48	GND
49	GND
50	GND

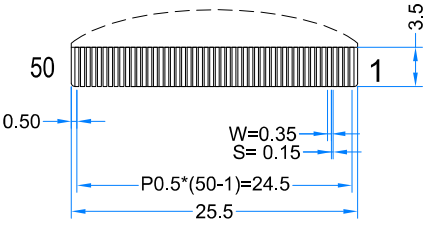




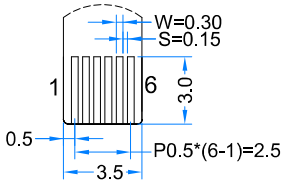


NOTES:
1. DISPLAY TYPE: TFT, TRANSMISSIVE, NORMALY WHITE
2. 2.83 INCH CAPACITIVE TOUCH PANEL
3. VIEWING DIRECTION: 6 O'CLOCK
4.OPERATION VOLTAGE: VDD= 2.8V
5. IC CONTROLLER: ILI9341
6. CTP IC DRIVER: FT6206
7. CTP RESOLUTION 240x320 DOTS
8. CTP MULTIFINGER: UP TO 2- TOUCH GESTURE
9. LED BACKLIGHT: 4-LED WHITE
10. SURFACE LUMINANCE: 255 cd/m^2
11.OPERATING TEMP: -20°C ~ +70°C
12. STORAGE TEMP: -30°C ~+80°C
13. GENERAL TOLERANCE: ±0.20
14. RoHS COMPLIANT

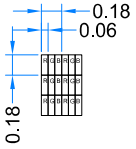
DETAIL B
SCALE 2:1



DETAIL C
SCALE 4:1



DETAIL A
SCALE 20:1



CUSTOME	
DRAWN	
DFTG CH	
ENGR CH	
APPROVA	

3 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage For LCD Logic	VDD	-0.3	4.6	V
Logic signal voltage	VDD	-0.3	4.6	V
Operating Temperature	T_{OP}	-20	70	°C
Storage Temperature	T_{ST}	-30	80	°C
Humidity	RH	-	90% (Max 60°C)	RH

4 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage For LCD Logic	VDD	2.5	2.8	3.3	V
Supply Voltage For CTP Logic	VDD	2.8	3.0	3.3	V
Input Current	IDD	-	TBD	-	mA
Input Voltage ' H ' level	V_{IH}	0.7VDD	-	VDD	V
Input Voltage ' L ' level	V_{IL}	GND	-	0.3VDD	V
Output Voltage ' H ' level	V_{OH}	0.8VDD	-	VDD	V
Output Voltage ' L ' level	V_{OL}	GND	-	0.2VDD	V

5 BACKLIGHT CHARACTERISTICS

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Voltage for LED backlight	V_f	-	3.2	3.4	V
Current for LED backlight	I_f	-	80	-	mA
Power consumption	W_{BL}	-	256	-	mW
LED Life Time	-	30000	40000	-	Hrs

Note:

1.The LED life time is defined as the module brightness decrease to 50% original brightness at Ta=25°C, 60%RH ±5 %.

2. The life time of LED will be reduced if LED is driven by high current, high ambient temperature and humidity conditions.

3. Typical operating life time is an estimated data.

4. Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded .Functional operation should be restricted to the conditions described under normal operating conditions.

6 ELECTRO-OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	REMARK	NOTE
Response Time		Tr+Tf	θ=0° Ø=0° Ta=25	-	25	30	ms	Figure 1	4
Contrast Ratio		Cr		-	500	-	---	Figure 2	1
Luminance Uniformity		δ WHITE		80	90	-	%	Figure 2	3
Surface Luminance		Lv		-	255	-	cd/m^2	Figure 2	2
Viewing Angle Range		θ	Ø = 90°	-	70	-	deg	Figure 3	6
			Ø = 270°	-	57	-	deg	Figure 3	
			Ø = 0°	-	70	-	deg	Figure 3	
			Ø = 180°	-	70	-	deg	Figure 3	
CIE (x, y) Chromaticity	Red	x	θ=0° Ø=0° Ta=25	-	0.6368	-	Figure 2		5
		y		-	0.3329	-			
	Green	x		-	0.3397	-			
		y		-	0.6138	-			
	Blue	x		-	0.1433	-			
		y		-	0.0807	-			
	White	x		-	0.2886	-			
		y		-	0.3194	-			
NTSC	-	S	-	55	67	-	%		-

Note 1. Contrast Ratio(CR) is defined mathematically as below, for more information see Figure 1

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see Figure 2.

$$\delta\ \text{WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see FIG 1. The test equipment is Autronic-Melchers's ConoScope series.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

Note 6. Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see Figure 3.

Note 7. For viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope series. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, CIE the test data is based on TOPCON's BM-5 photo detector.

Figure 1. The definition of response time

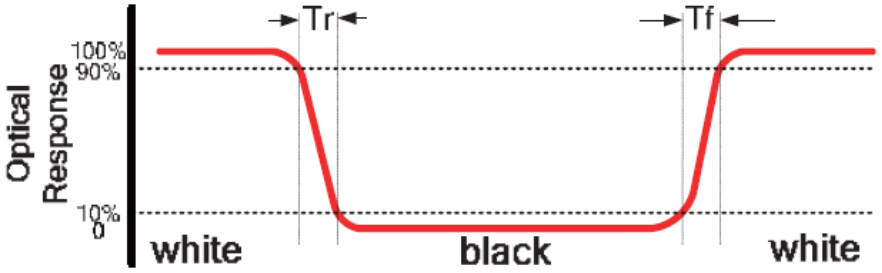


Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

A : 5 mm
B : 5 mm
H,V : Active Area
Light spot size ∅=5mm, 500mm distance from the LCD surface to detector lens
measurement instrument is TOPCON's luminance meter BM-5

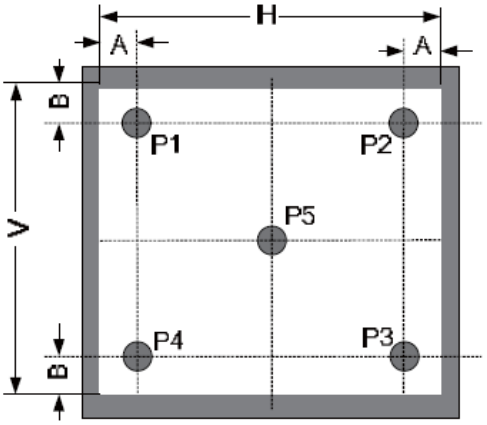
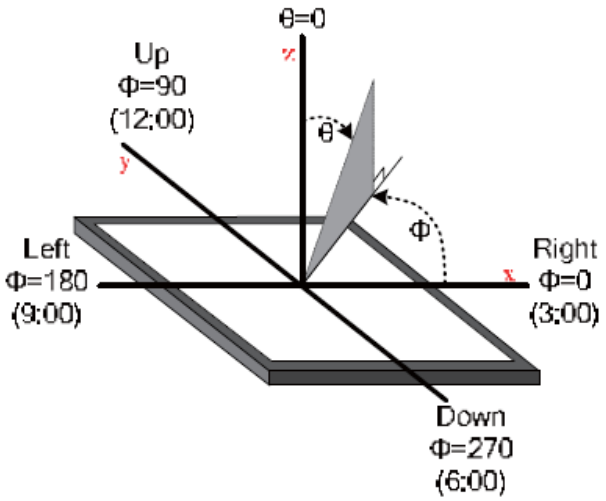


Figure 3.The definition of viewing angle



7 INTERFACE DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION	REMARK
1	LEDK	Cathode Of LED Backlight	
2	LEDA1	Anode No.1 for LED backlighting	
3	LEDA2	Anode No.2 for LED backlighting	
4	LEDA3	Anode No.3 for LED backlighting	
5	LEDA4	Anode No.4for LED backlighting	
6	IM0	Select Interface Mode	Note1
7	IM1		
8	IM2		
9	IM3		
10	RESET	Reset pin	
11	VSYNC	Frame Synchronizing Signal For RGB Interface	
12	HSYNC	Line Synchronizing Signal For RGB Interface	
13	DOTCLK	Dot Clock Signal For RGB Interface	
14	DE	Data Enable Signal For RGB Interface	
15- 32	DB17-DB0	DATA BUS	
33	SDO	Serial Output Signal	
34	SDI	Serial Input Signal	
35	RD	Read execution control pin	
36	WRX(D/CX)	Write execution control pin; Serial Register select s Signal	
37	D/CX(SCL)	Register select signal; Serial Interface Clock	
38	CSX	Hip Select Signal	
39	TE	Tearing effect out pin synchronize MPU to frame writing	
40	VDDI	Power Supply : + 2.8V	
41	VDDI	Power Supply : +2.8V	
42	VCI	Logic power, provide with 2.8V	
43	GND	Power Ground	
44	NC	No Connection	
45	NC	No Connection	
46	NC	No Connection	
47	NC	No Connection	
48	GND	Power Ground	
49	GND	Power Ground	
50	GND	Power Ground	

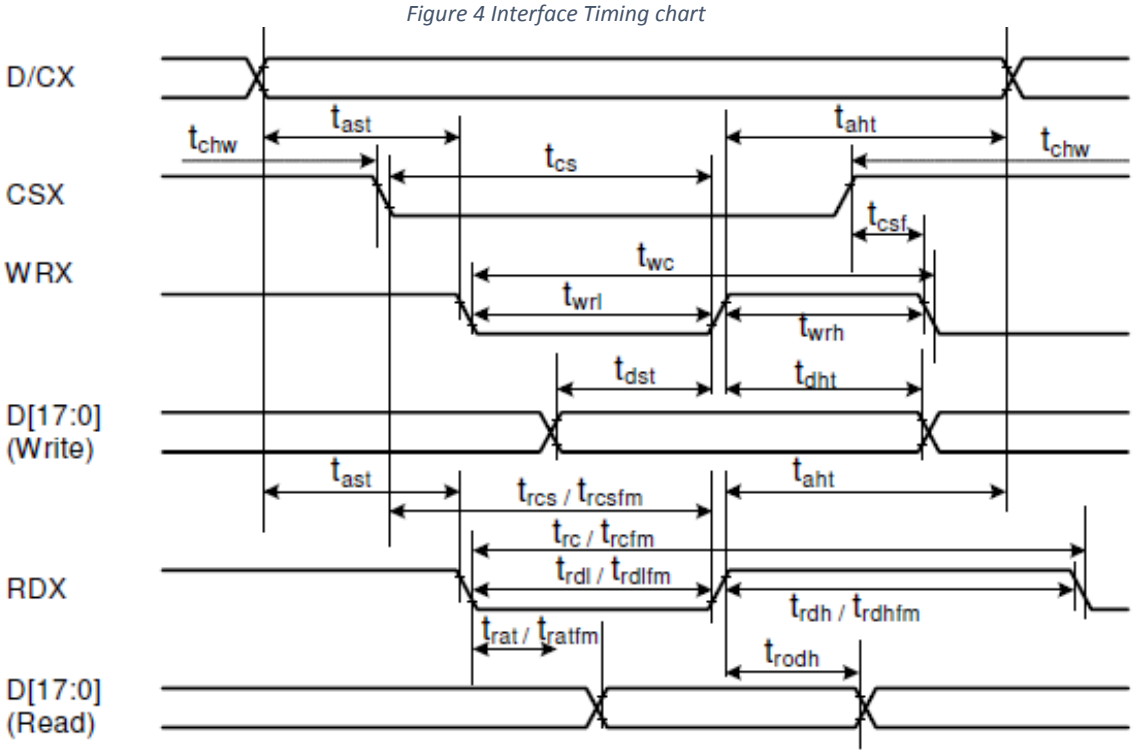
Note1: (pins 6-9)

IM 3	IM 2	IM 1	IM 0	MCU-Interface Mode	REGISTER/ CONTENT	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0], WRX, RDX, CSX, D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0], WRX, RDX, CSX, D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0], WRX, RDX, CSX, D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0], WRX, RDX, CSX, D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL, SDA, CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL, SDA, D/CX, CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1], WRX, RDX, CSX, D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10], WRX, RDX, CSX, D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0], WRX, RDX, CSX, D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9], WRX, RDX, CSX, D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL, SDA, SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL, SDA, D/CX, SDO, CSX	

8 LCD TIMING CHARACTERISTICS

8.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-I system)

Figure 4 Interface Timing chart



SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Wrote/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read IT)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select setup time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trc	Write Cycle(FM)	450	-	ns	
	trdh	Read Control H duration (FM)	90	-	ns	
	trdl	Read Control L duration (FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160		ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0] D[17:10] D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For max CL= 30pF For min CL= 8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note1: Ta= -30 to 70°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

Note2: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

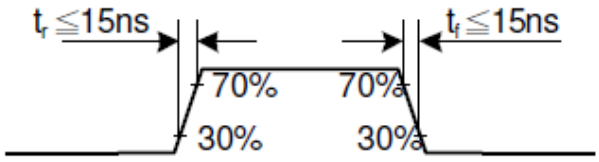
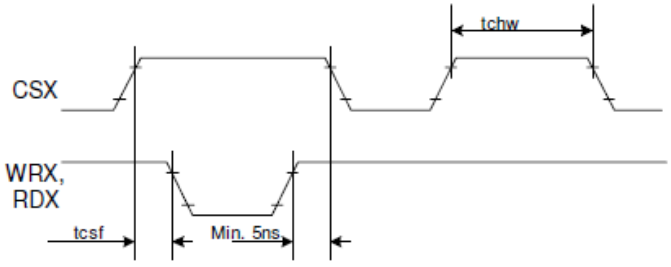


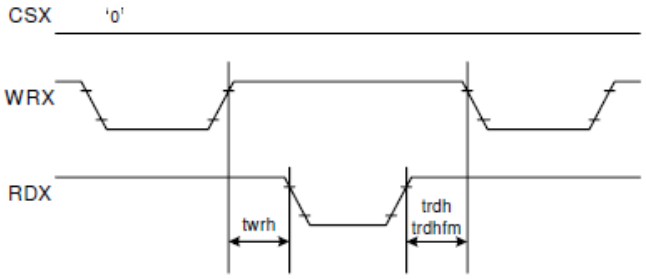
Figure 5 CSX timing



Note: Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

The details of controller command and communications are included in ILI9341 datasheet.

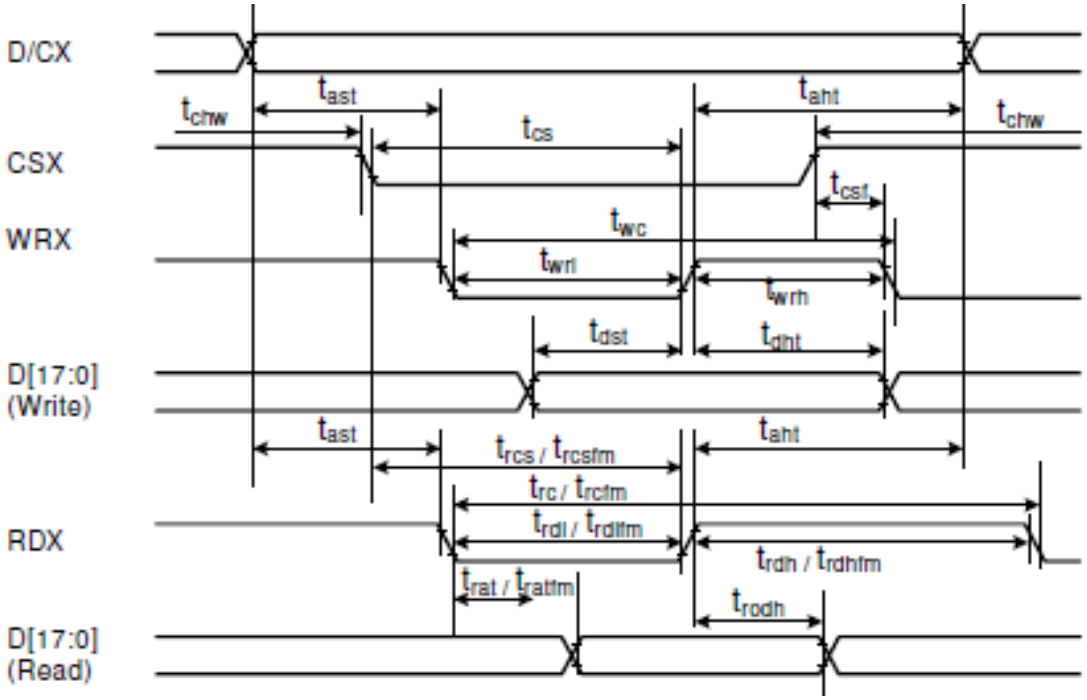
Figure 6 Writing to read or read to write timings



Note: Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

The details of controller command and communications are included in ILI9341 datasheet.

8.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-II system)



SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Wrote/Read)	0	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read IT)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select setup time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trc	Write Cycle(FM)	450	-	ns	

RDX(FM)	trdh	Read Control H duration (FM)	90	-	ns	
	trdl	Read Control L duration (FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160		ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0] D[17:10] D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For max CL= 30pF For min CL= 8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note1: Ta= -30 to 70°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

Note2: Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

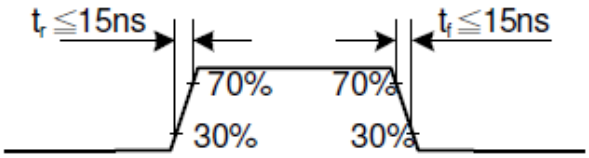
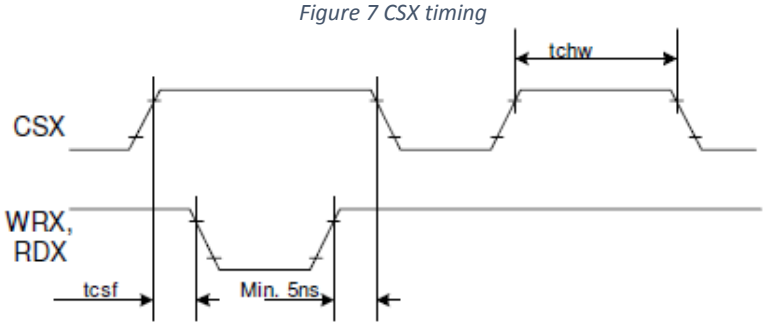
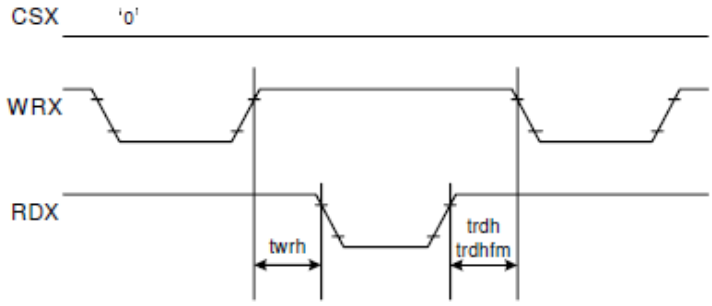


Figure 7 CSX timing



Note: Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

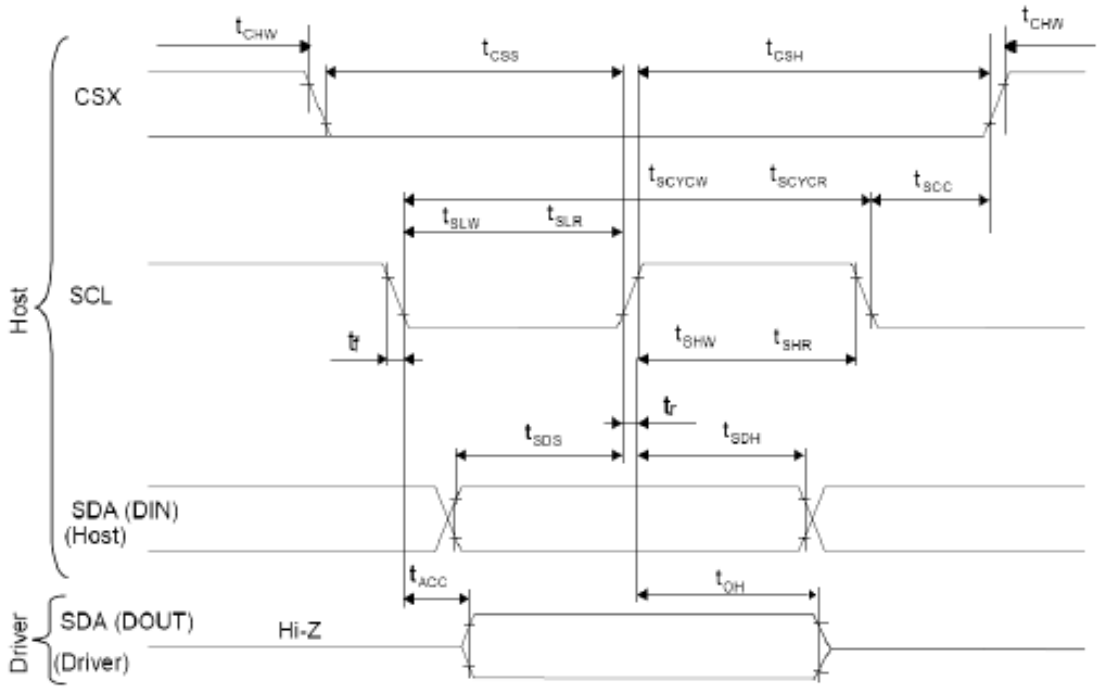
Figure 8 Writing to read or read to write timings



Note: Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

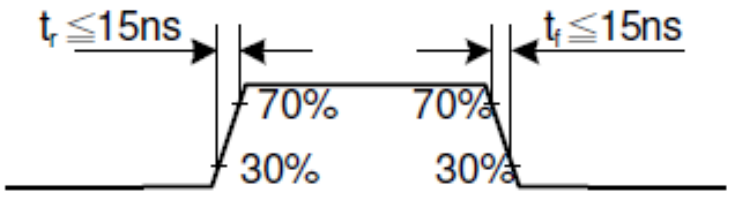
The details of controller command and communications are included in ILI9341 datasheet.

8.3 Display Serial Interface Timing Characteristics (3-line SPI system)



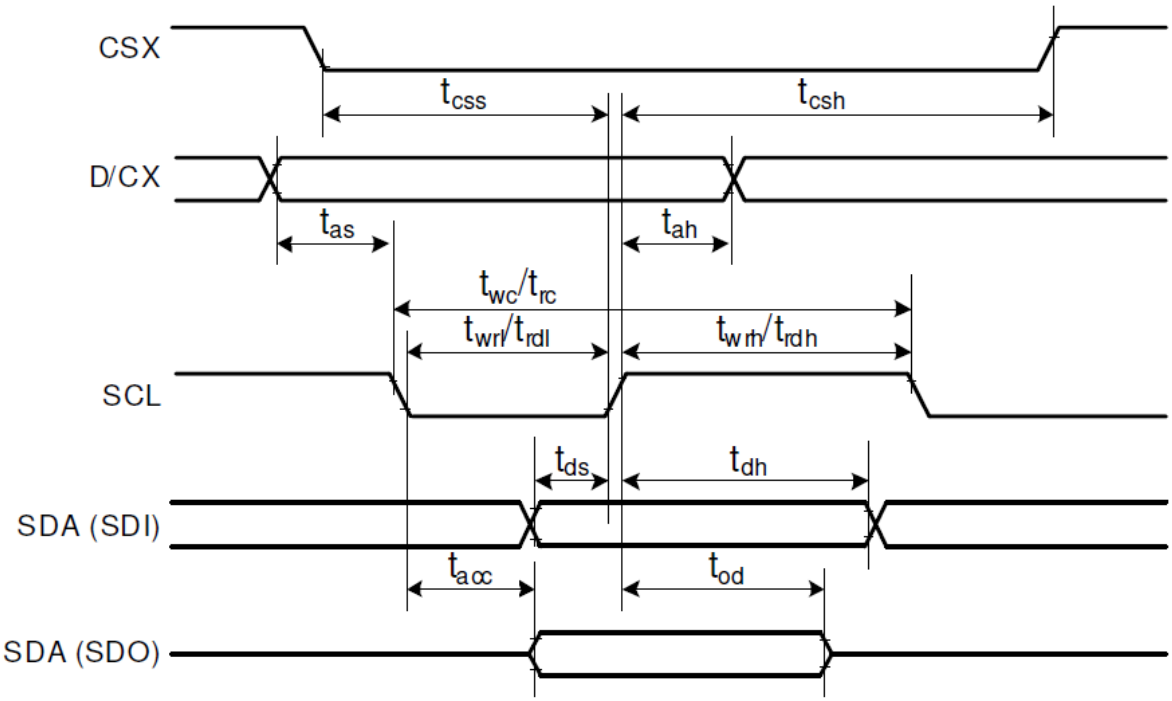
SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width(Write)	40	-	ns	
	tslw	SCL “L” Pulse Width(Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width(Read)	60	-	ns	
	tslr	SCL “L” Pulse Width(Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA/SDI (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	SCX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta25°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V.



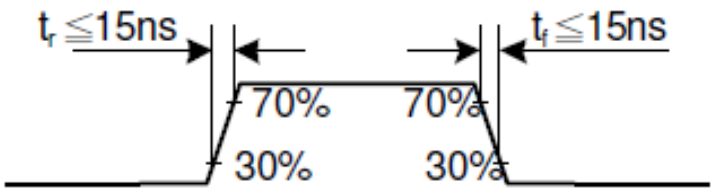
The details of controller command and communications are included in ILI9341 datasheet.

8.4 Display Serial Interface Timing Characteristics (4-line SPI system)



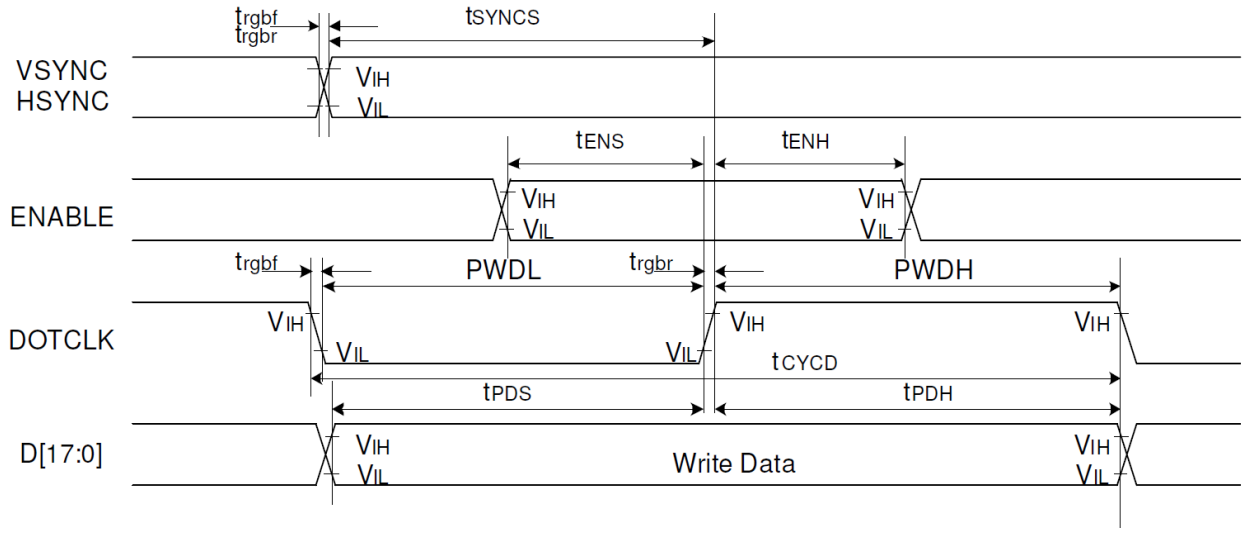
SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
CSX	tcss	Serial Clock Cycle (Write)	40	-	ns	
	tcsh	SCL "H" Pulse Width(Write)	40	-	ns	
SCL	twc	Serial Clock Cycle (Read)	100	-	ns	
	twrh	SCL "H" Pulse Width(Read)	40	-	ns	
	twrl	SCL "L" Pulse Width(Read)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width(Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write/ Read)	10	-		
SDA/SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA/SDI (Output)	tacc	Access time (Read)	10	-	ns	For max CL=30pF For min CL=8pF
	tod	Output disable time (Read)	10	50	ns	

Note: Ta25°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V.



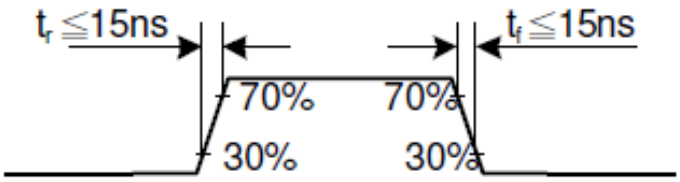
The details of controller command and communications are included in ILI9341 datasheet.

8.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16 –bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100			
	t_{rgbr}, t_{rgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6 –bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100			
	t_{rgbr}, t_{rgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: Ta25°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V.



The details of controller command and communications are included in ILI9341 datasheet.

9 INITIAL CODE

```
// Hardware reset
       GPIO_WriteBit(HW_Reset_Pin,1);
       delay_ms(50);
       GPIO_WriteBit(HW_Reset_Pin,0);
       delay_ms(50);
       GPIO_WriteBit(HW_Reset_Pin,1);
       delay_ms(50);

     LCD_WriteCommand(0x01); // Software reset
     delay_ms(5);
     LCD_WriteCommand(0x28); //Display off

    //------------------------------------------------------------
    LCD_WriteCommand(0xcf); //Power control B
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x83);
    LCD_WriteRAM(0x30);

    LCD_WriteCommand(0xed); //Power on sequence control
    LCD_WriteRAM(0x64);
    LCD_WriteRAM(0x03);
    LCD_WriteRAM(0x12);
    LCD_WriteRAM(0x81);

    LCD_WriteCommand(0xe8); //Driver timing control A
    LCD_WriteRAM(0x85);
    LCD_WriteRAM(0x01);
    LCD_WriteRAM(0x79);

    LCD_WriteCommand(0xcb); //Power control A
    LCD_WriteRAM(0x39);
    LCD_WriteRAM(0x2c);
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x34);
    LCD_WriteRAM(0x02);

    LCD_WriteCommand(0xf7); //Pump ratio control
    LCD_WriteRAM(0x20);

    LCD_WriteCommand(0xea); //Driver timing control B
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x00);

    //-----------------------Power Control--------------------
    LCD_WriteCommand(0xc0); // Power Control 1
    LCD_WriteRAM(0x26);

    LCD_WriteCommand(0xc1); // Power Control 2
    LCD_WriteRAM(0x11);

    //-------------------VCOM setting ------------------------
    LCD_WriteCommand(0xc5); // VCOM Control
    LCD_WriteRAM(0x35);
    LCD_WriteRAM(0x3e);

    LCD_WriteCommand(0xc7); // VCOM Control
    LCD_WriteRAM(0xbe);

    //--------------Memory Access Control--------------
    LCD_WriteCommand(0x36); //Memory Access Control
    LCD_WriteRAM(0x48); //my, mx, mv, ml, BGR, mh, 0.0

    LCD_WriteCommand(0x3a); // Pixel Format set
    LCD_WriteRAM(0x55);    // 16bit /pixel
```

```
    //------------------ Frame Rate-----------------------
    LCD_WriteCommand(0xb1); // Frame rate
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x10);

    //------------------Gamma---------------------------------
    LCD_WriteCommand(0xf2); // 3 Gamma Function Disable
    LCD_WriteRAM(0x08);

    LCD_WriteCommand(0x26); // Gamma set 4 gamma curve 01/02/04/08
    LCD_WriteRAM(0x01);

    LCD_WriteCommand(0xE0); // Positive Gamma Correction
    LCD_WriteRAM(0x1f);
    LCD_WriteRAM(0x1a);
    LCD_WriteRAM(0x18);
    LCD_WriteRAM(0x0a);
    LCD_WriteRAM(0x0f);
    LCD_WriteRAM(0x06);
    LCD_WriteRAM(0x45);
    LCD_WriteRAM(0x87);
    LCD_WriteRAM(0x32);
    LCD_WriteRAM(0x0a);
    LCD_WriteRAM(0x07);
    LCD_WriteRAM(0x02);
    LCD_WriteRAM(0x07);
    LCD_WriteRAM(0x05);
    LCD_WriteRAM(0x00);

    LCD_WriteCommand(0xE1); // Negative Gamma Correction
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x25);
    LCD_WriteRAM(0x27);
    LCD_WriteRAM(0x05);
    LCD_WriteRAM(0x10);
    LCD_WriteRAM(0x09);
    LCD_WriteRAM(0x3a);
    LCD_WriteRAM(0x78);
    LCD_WriteRAM(0x4d);
    LCD_WriteRAM(0x05);
    LCD_WriteRAM(0x18);
    LCD_WriteRAM(0x0d);
    LCD_WriteRAM(0x38);
    LCD_WriteRAM(0x3a);
    LCD_WriteRAM(0x1f);

    //------------------ddram----------------------
    LCD_WriteCommand(0x2a); // Column Set
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0xEF);

    LCD_WriteCommand(0x2b); // Page address set
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x00);
    LCD_WriteRAM(0x01);
    LCD_WriteRAM(0x3F);

    LCD_WriteCommand(0xb7); // Entry mode set
    LCD_WriteRAM(0x07);

    //---------------------Display----------------------
    LCD_WriteCommand(0xb6); // Display function control
    LCD_WriteRAM(0x0a);
    LCD_WriteRAM(0x82);
    LCD_WriteRAM(0x27);
    LCD_WriteRAM(0x00);
```

```
LCD_WriteCommand(0x11); // Sleep out
delay_ms(100);

LCD_WriteCommand(0x29); // Display on
delay_ms(50);

LCD_WriteCommand(0x2a); // Column set
LCD_WriteRAM(0x00);
LCD_WriteRAM(0x00);
LCD_WriteRAM(0x00);
LCD_WriteRAM(0xEF);

LCD_WriteCommand(0x2b); // Page address set
LCD_WriteRAM(0x00);
LCD_WriteRAM(0x00);
LCD_WriteRAM(0x01);
LCD_WriteRAM(0x3F);
```

10 CAPACITIVE TOUCH SCREEN PANEL SPECIFICATIONS

10.1 Mechanical characteristics

DESCRIPTION	INL SPECIFICATION	REMARK
Touch Panel Size	2.83 inch	
Outline Dimension (OD)	49.5mm x 68.75mm	Cover Lens Outline
Product Thickness	1.675mm	
Glass Thickness	0.70mm	
Ink View Area	44.2mm x 58.6mm	
Sensor Active Area	45.20mm x 59.60mm	
Input Method	2 Fingers	
Activation Force	Touch	
Surface Hardness	≥6H	

10.2 Electrical characteristics

DESCRIPTION		SPECIFICATION
Operating Voltage		DC 2.8~3.3V
Power Consumption (IDD)	Active Mode	12~4.5mA
	Sleep Mode	TBD
Interface		I^2C
Controller		FT6206
I2C address		0x38 (7 bit address)
Resolution		240*320

10.3 Interface description

PIN NO.	SYMBOL	DESCRIPTION	REMARK
1	VDD	Power supply	
2	/RES	Reset pin	
3	/INT	Interrupt signal from CTP	
4	SDA	I2C data signal	
5	SCK	I2C clock input	
6	GND	Ground	

10.4 Interface timing characteristics

PARAMETER	MIN	MAX	UNIT
SCL Frequency	0	400	kHz
Bus Free Time Between a STOP and START Condition	4.7	/	µs
Hold Time (repeated) START Condition	4.0	/	µs
Data Setup Time	250	/	ns
Setup Time for Repeated START Condition	4.7	/	µs
Setup Time for STOP Condition	4.0	/	µs

Note: For more information please go to IC specification.

10.5 CTP timing configuration

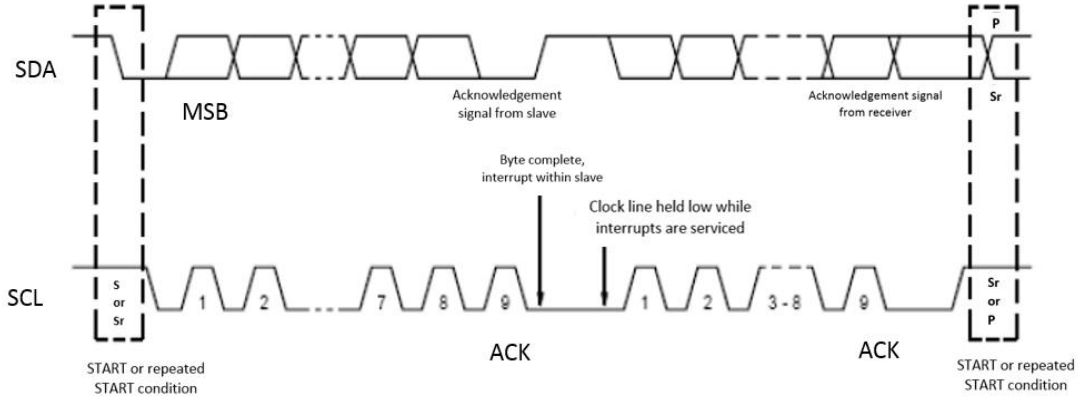


Figure 9. I2C master write, slave read

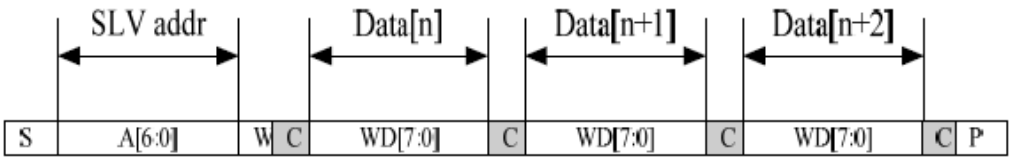
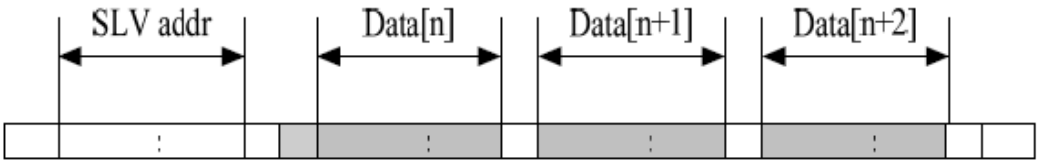


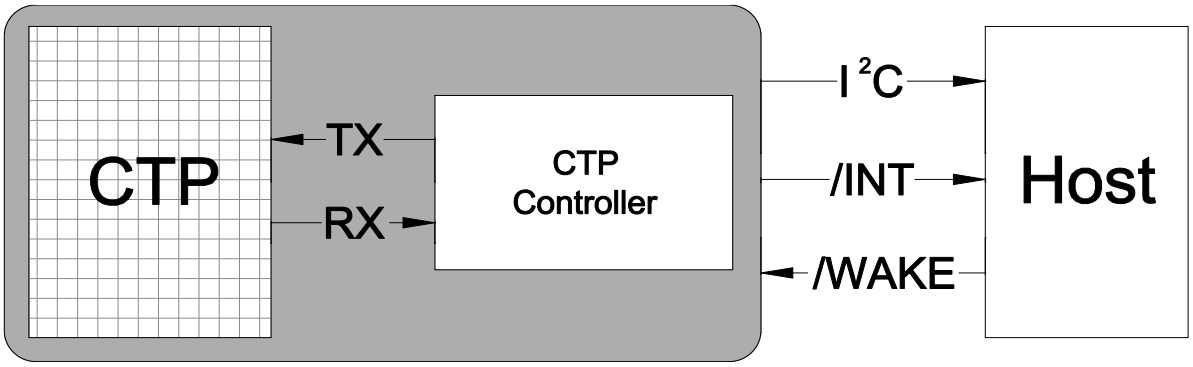
Figure 10. I2C master read, slave write



MNEMONICS	DESCRIPTIO
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b0: Read
C	ACK
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

10.6 Communication of the I2C interface with Host

Figure 11. Communication of the I2C interface with Host



10.7 Touch data read protocol

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	HOST ACCESS
00h	DEVIDE_MODE		Device Mode[2:0]							RW
01h	GEST_ID	Gesture ID[7:0]								R
02h	TD_STATUS					Number of touch points[3:0]				R
03h	TOUCH1_XH	1st Event Flag				1st Touch X Position[11:8]				R
04h	TOUCH1_XL	1st Touch X Position[7:0]								R
05h	TOUCH1_YH	1st Touch ID[3:0]				1st Touch X Position[11:8]				R
06h	TOUCH1_YL	1st Touch Y Position[7:0]								R

10.8 Data description

DEVICE_MODE

This register is the device mode register, configure it to determine the current mode of the chip.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
00h	6:4	Device Mode [2:0]	000b Work Mode 100b Factory Mode – Read Raw Data

GEST_ID

This register describes the gesture of a valid touch.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
01h	7:0	Gesture ID [7:0]	Gesture ID 0x10 Move Up 0x14 Move Down 0x18 Move Right 0x48 Zoom In 0x49 Zoom Out 0x00 No Gesture

TD_STATUS

This register is the Touch Data status register.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
02h	3:0	Number of Touch Points [2:0]	How Many Points Detected 1-5 is Valid
	7:4		

TOUCHn_XH(n:1-10)

This register describes MSB of the X coordinate of the nth touch point and the corresponding event flag.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
03h ~ 39h	7:6	Event Flag	00b: Put Down 01b: Put Up 10b: Contact 11b: Reserved
	5:4		Reserved
	3:0	Touch X Position [11:8]	MSB of Touch X Position in Pixels

TOUCHn_XL(n:1-10)

This register describes LSB of the X coordinate of the nth touch point.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
04h ~ 3Ah	7:0	Touch X Position [7:0]	LSB of the Touch X Position in Pixels

TOUCHn_YH(n:1-10)

This register describes MSB of the Y coordinate of the nth touch point and corresponding touch ID.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
05h	7:4	Touch ID[3:0]	Touch ID of Touch Point
~ 3Bh	3:0	Touch X Position [11:8]	MSB of Touch Y Position in Pixels

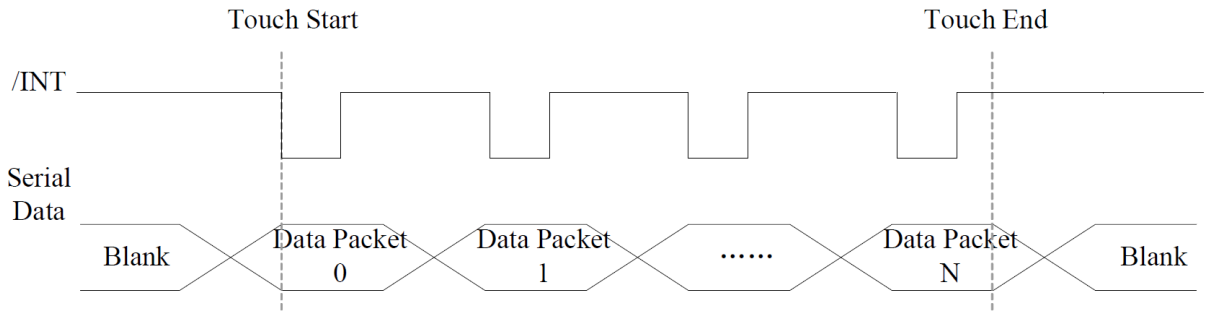
TOUCHn_YL(n:1-10)

This register describes LSB of the Y coordinate of the nth touch point.

ADRESS	BIT ADRESS	REGISTER NAME	DESCRIPTION
05h ~ 3Bh	7:0	Touch X Position [7:0]	LSB of the Touch Y Position in Pixels

10.9 Interrupt Trigger Mode

Figure 12. Interrupt trigger mode timing



11 RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	INSPECTION AFTER TEST
1	High Temperature Storage	80±2°C/96 hours	Inspection after 2~4 hours storage at room temperature and humidity. The condensation is not accepted. The sample shall be free from defects: 1. Air bubble in the LCD 2. Seal leak 3. Non-display 4. Missing segments 5. Glass crack
2	Low Temperature Storage	-30±2°C/96 hours	
3	High Temperature Operating	70±2°C/96 hours	
4	Low Temperature Operating	-20±2°C/96 hours	
5	Temperature Cycle	-30±2°C ~ 25~ 80± 2°C × 10 cycles (30 min.) (5min.) (30min.)	
6	Damp Proof Test	60°C ±5°C × 90%RH/96 hours	
7	Vibration Test	Frequency 10Hz~55Hz Stroke: 1.5mm Sweep: 10Hz~150 Hz~10Hz 2 hours For each direction of X, Y, Z	
8	Shock Test	Half-sine, wave, 300m/s	
9	Packing Drop Test	Height: 80 cm 1 corner, concrete floor	
11	Electrostatic Discharge Test	C=150pF, R=330 Ω Air: ±8KV 150pF/330Ω 30 times Contact: ±4KV,20 times	

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