# Ultralow Noise 0.37GHz to 6.39GHz Fractional-N Synthesizer with Integrated VCO

## FEATURES

- **Low Noise Fractional-N PLL with Integrated VCO**
- **No Δ-Σ Modulator Spurs**
- **18-Bit Fractional Denominator**
- **–226 dBc/Hz Normalized In-Band Phase Noise Floor**
- **–274 dBc/Hz Normalized In-Band 1/f Noise**
- **–157 dBc/Hz Wideband Output Phase Noise Floor**
- **Excellent Integer Boundary Spurious Performance**
- **Output Divider (1 to 6, 50% Duty Cycle)**
- **Output Buffer Muting**
- Reference Input Frequency Up to 425MHz
- Fast Frequency Switching
- FracNWizard™ Software Design Tool Support

## APPLICATIONS

- Wireless Basestations (LTE, WiMAX, W-CDMA, PCS)
- Microwave Data Links
- Military and Secure Radio
- Test and Measurement



## DESCRIPTION

The LTC®6948 is a high performance, low noise, 6.39GHz phase-locked loop (PLL) with a fully integrated VCO, including a reference divider, phase-frequency detector (PFD), ultralow noise charge pump, fractional feedback divider, and VCO output divider.

The fractional divider uses an advanced, 4th order ΔΣ modulator which provides exceptionally low spurious levels. This allows wide loop bandwidths, producing extremely low integrated phase noise values.

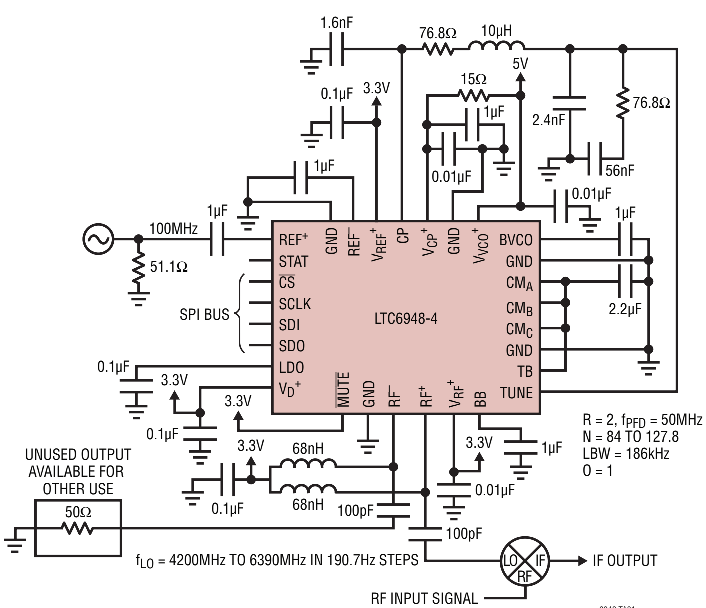
The programmable VCO output divider, with a range of 1 through 6, extends the output frequency range.

**Output Frequency Options**

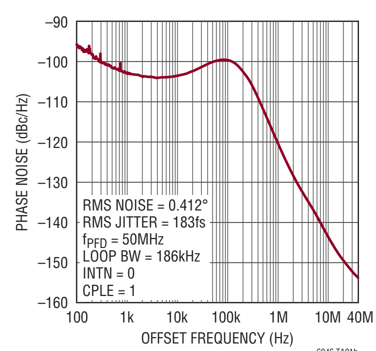
| | LTC6948-1 | LTC6948-2 | LTC6948-3 | LTC6948-4 |
|---|---|---|---|---|
| O_DIV = 1 | 2.240 to 3.740 | 3.080 to 4.910 | 3.840 to 5.790 | 4.200 to 6.390 |
| O_DIV = 2 | 1.120 to 1.870 | 1.540 to 2.455 | 1.920 to 2.895 | 2.100 to 3.195 |
| O_DIV = 3 | 0.747 to 1.247 | 1.027 to 1.637 | 1.280 to 1.930 | 1.400 to 2.130 |
| O_DIV = 4 | 0.560 to 0.935 | 0.770 to 1.228 | 0.960 to 1.448 | 1.050 to 1.598 |
| O_DIV = 5 | 0.448 to 0.748 | 0.616 to 0.982 | 0.768 to 1.158 | 0.840 to 1.278 |
| O_DIV = 6 | 0.373 to 0.623 | 0.513 to 0.818 | 0.640 to 0.965 | 0.700 to 1.065 |

## TYPICAL APPLICATION

**6.3GHz Wideband Receiver**




**LTC6948-4 Phase Noise, $f_{RF}$ = 6236MHz**



## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltages
- $V^+$ ($V_{REF}^+$, $V_{RF}^+$, $V_D^+$) to GND ............................... 3.6V
- $V_{CP}^+$, $V_{VCO}^+$ to GND ............................................ 5.5V

Voltage on CP Pin ................. GND – 0.3V to $V_{CP}^+$ + 0.3V

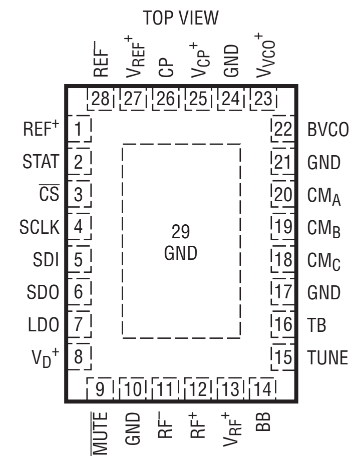
Voltage on all other Pins ........... GND – 0.3V to $V^+$ + 0.3V

Operating Junction Temperature Range, $T_J$ (Note 2)
- LTC6948I ......................................... –40°C to 105°C

Junction Temperature, $T_{JMAX}$ ............................... 125°C

Storage Temperature Range .................. –65°C to 150°C

## PIN CONFIGURATION




UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JCbottom}$ = 7°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION http://www.linear.com/product/LTC6948#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | JUNCTION TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6948IUFD-1#PBF | LTC6948IUFD-1#TRPBF | 69481 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 105°C |
| LTC6948IUFD-2#PBF | LTC6948IUFD-2#TRPBF | 69482 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 105°C |
| LTC6948IUFD-3#PBF | LTC6948IUFD-3#TRPBF | 69483 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 105°C |
| LTC6948IUFD-4#PBF | LTC6948IUFD-4#TRPBF | 69484 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 105°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## AVAILABLE OPTIONS

| VCO FREQUENCY RANGE (GHz) | PACKAGE STYLE | OUTPUT FREQUENCY RANGE vs OUTPUT DIVIDER SETTING (GHz) | | | | | |
|---|---|---|---|---|---|---|---|
| | QFN-28 (UFD28) | O DIV = 6 | O DIV = 5 | O DIV = 4 | O DIV = 3 | O DIV = 2 | O DIV = 1 |
| 2.240 to 3.740 | LTC6948IUFD-1 | 0.373 to 0.623 | 0.448 to 0.748 | 0.560 to 0.935 | 0.747 to 1.247 | 1.120 to 1.870 | 2.240 to 3.740 |
| 3.080 to 4.910 | LTC6948IUFD-2 | 0.513 to 0.818 | 0.616 to 0.982 | 0.770 to 1.228 | 1.027 to 1.637 | 1.540 to 2.455 | 3.080 to 4.910 |
| 3.840 to 5.790 | LTC6948IUFD-3 | 0.640 to 0.965 | 0.768 to 1.158 | 0.960 to 1.448 | 1.280 to 1.930 | 1.920 to 2.895 | 3.840 to 5.790 |
| 4.200 to 6.390 | LTC6948IUFD-4 | 0.700 to 1.065 | 0.840 to 1.278 | 1.050 to 1.598 | 1.400 to 2.130 | 2.100 to 3.195 | 4.200 to 6.390 |
| | | **Overlapping Frequency Bands** | | | | | |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{REF}^+$ = $V_D^+$ = $V_{RF}^+$ = 3.3V, $V_{CP}^+$ = $V_{VCO}^+$ = 5V unless otherwise specified (Note 2). All voltages are with respect to GND.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference Inputs (REF⁺, REF⁻)** | | | | | | | |
| $f_{REF}$ | Input Frequency | | ● | 10 | | 425 | MHz |
| $V_{REF}$ | Input Signal Level | Single-Ended, 1µF AC-Coupling Capacitors | ● | 0.5 | 2 | 2.7 | $V_{P-P}$ |
| | Input Slew Rate | | ● | 20 | | | V/µs |
| | Input Duty Cycle | | | | 50 | | % |
| | Self-Bias Voltage | | ● | 1.65 | 1.85 | 2.25 | V |
| | Input Resistance | Differential | ● | 5.8 | 8.4 | 11.6 | kΩ |
| | Input Capacitance | Differential | | | 14 | | pF |
| **VCO** | | | | | | | |
| $f_{VCO}$ | Frequency Range | LTC6948-1 (Note 3)<br>LTC6948-2 (Note 3)<br>LTC6948-3 (Note 3)<br>LTC6948-4 (Note 3) | ●<br>●<br>●<br>● | 2.24<br>3.08<br>3.84<br>4.20 | | 3.74<br>4.91<br>5.79<br>6.39 | GHz<br>GHz<br>GHz<br>GHz |
| $K_{VCO}$ | Tuning Sensitivity | LTC6948-1 (Notes 3, 4)<br>LTC6948-2 (Notes 3, 4)<br>LTC6948-3 (Notes 3, 4)<br>LTC6948-4 (Notes 3, 4) | ●<br>●<br>●<br>● | | 4.7 to 7.2<br>4.7 to 7.0<br>4.0 to 6.0<br>4.5 to 6.5 | | %Hz/V<br>%Hz/V<br>%Hz/V<br>%Hz/V |
| **RF Output (RF⁺, RF⁻)** | | | | | | | |
| $f_{RF}$ | Output Frequency | | ● | 0.373 | | 6.39 | GHz |
| O | Output Divider Range | All Integers Included | ● | 1 | | 6 | |
| | Output Duty Cycle | | | | 50 | | % |
| | Output Resistance | Single-Ended, Each Output to $V_{RF}^+$ | ● | 100 | 136 | 175 | Ω |
| $P_{RF-SE}$ | Output Power, Single-Ended, $f_{RF}$ = 900MHz | RFO[1:0] = 0, $R_Z$ = 50Ω, LC Match<br>RFO[1:0] = 1, $R_Z$ = 50Ω, LC Match<br>RFO[1:0] = 2, $R_Z$ = 50Ω, LC Match<br>RFO[1:0] = 3, $R_Z$ = 50Ω, LC Match | ●<br>●<br>●<br>● | –9<br>–6.1<br>–2.9<br>0.1 | –7.3<br>–4.5<br>–1.4<br>1.5 | –5.5<br>–2.8<br>0.2<br>3 | dBm<br>dBm<br>dBm<br>dBm |
| | Output Power, Muted, $f_{RF}$ = 900MHz | $R_Z$ = 50Ω, Single-Ended, O = 2 to 6 | ● | | | –80 | dBm |
| | Mute Enable Time | | ● | | | 110 | ns |
| | Mute Disable Time | | ● | | | 170 | ns |
| **Phase/Frequency Detector** | | | | | | | |
| $f_{PFD}$ | Input Frequency | Integer mode<br>Fractional mode<br>LDOEN = 0<br>LDOV = 3, LDOEN = 1<br>LDOV = 2, LDOEN = 1<br>LDOV = 1, LDOEN = 1<br>LDOV = 0, LDOEN = 1 | ●<br><br>●<br>●<br>●<br>●<br>● | | | 100<br><br>76.1<br>66.3<br>56.1<br>45.9<br>34.3 | MHz<br><br>MHz<br>MHz<br>MHz<br>MHz<br>MHz |
| **Charge Pump** | | | | | | | |
| $I_{CP}$ | Output Current Range | 8 Settings (See Table 6) | | 1 | | 11.2 | mA |
| | Output Current Source/Sink Accuracy | All Settings, V(CP) = $V_{CP}^+/2$ | | | | ±6 | % |
| | Output Current Source/Sink Matching | $I_{CP}$ = 1.0mA to 2.8mA, V(CP) = $V_{CP}^+/2$<br>$I_{CP}$ = 4.0mA to 11.2mA, V(CP) = $V_{CP}^+/2$ | | | | ±3.5<br>±2 | %<br>% |
| | Output Current vs Output Voltage Sensitivity | (Note 5) | ● | | 0.2 | 1 | %/V |
| | Output Current vs Temperature | V(CP) = $V_{CP}^+/2$ | ● | | 170 | | ppm/°C |
| | Output Hi-Z Leakage Current | $I_{CP}$ = 11.2mA, CPCLO = CPCHI = 0 (Note 5) | | | 0.03 | | nA |

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V unless otherwise specified (Note 2). All voltages are with respect to GND.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CLMP-LO}$ | Low Clamp Voltage | CPCLO = 1 | | | 0.84 | | V |
| $V_{CLMP-HI}$ | High Clamp Voltage | CPCHI = 1, Referred to $V_{CP}^+$ | | | –0.96 | | V |
| $V_{MID}$ | Mid-Supply Output Bias Ratio | Referred to ($V_{CP}^+$ – GND) | | | 0.48 | | V/V |
| **Reference (R) Divider** | | | | | | | |
| R | Divide Range | All Integers Included | ● | 1 | | 31 | Counts |
| **VCO (N) Divider** | | | | | | | |
| N | Divide Range | All Integers Included, Integer Mode<br>All Integers Included, Fractional Mode | ●<br>● | 32<br>35 | | 1023<br>1019 | Counts<br>Counts |
| **Fractional ΔΣ Modulator** | | | | | | | |
| | Numerator Range | All Integers Included | ● | 1 | | 262143 | Counts |
| **Modulator LDO** | | | | | | | |
| | Output Voltage | LDO Enabled, Four Values<br>LDO Disabled | | | 1.7 to 2.6<br>$V_D^+$ | | V<br>V |
| | External Pin Capacitance | Required for LDO Stability | ● | 0.047 | 0.1 | 1 | µF |
| **Digital Pin Specifications** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $\overline{MUTE}$, $\overline{CS}$, SDI, SCLK | ● | 1.55 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $\overline{MUTE}$, $\overline{CS}$, SDI, SCLK | ● | | | 0.8 | V |
| $V_{IHYS}$ | Input Voltage Hysteresis | $\overline{MUTE}$, $\overline{CS}$, SDI, SCLK | | | 250 | | mV |
| | Input Current | $\overline{MUTE}$, $\overline{CS}$, SDI, SCLK | ● | | | ±1 | µA |
| $I_{OH}$ | High Level Output Current | SDO and STAT, $V_{OH} = V_D^+$ – 400mV | ● | | –3.3 | –1.9 | mA |
| $I_{OL}$ | Low Level Output Current | SDO and STAT, $V_{OL}$ = 400mV | ● | 2.0 | 3.4 | | mA |
| | SDO Hi-Z Current | | ● | | | ±1 | µA |
| **Digital Timing Specifications (See Figure 6 and Figure 7)** | | | | | | | |
| $t_{CKH}$ | SCLK High Time | | ● | 25 | | | ns |
| $t_{CKL}$ | SCLK Low Time | | ● | 25 | | | ns |
| $t_{CSS}$ | $\overline{CS}$ Setup Time | | ● | 10 | | | ns |
| $t_{CSH}$ | $\overline{CS}$ High Time | | ● | 10 | | | ns |
| $t_{CS}$ | SDI to SCLK Setup Time | | ● | 6 | | | ns |
| $t_{CH}$ | SDI to SCLK Hold Time | | ● | 6 | | | ns |
| $t_{DO}$ | SCLK to SDO Time | To $V_{IH}/V_{IL}$/Hi-Z with 30pF Load | ● | | | 16 | ns |
| **Power Supply Voltages** | | | | | | | |
| | $V_{REF}^+$ Supply Range | | ● | 3.15 | 3.3 | 3.45 | V |
| | $V_D^+$ Supply Range | | ● | 3.15 | 3.3 | 3.45 | V |
| | $V_{RF}^+$ Supply Range | | ● | 3.15 | 3.3 | 3.45 | V |
| | $V_{VCO}^+$ Supply Range | | ● | 4.75 | 5.0 | 5.25 | V |
| | $V_{CP}^+$ Supply Range | | ● | 4.0 | | 5.25 | V |
| **Power Supply Currents** | | | | | | | |
| $I_{DD}$ | $V_D^+$ Supply Current | Digital Inputs at Supply Levels, Integer Mode<br>Digital Inputs at Supply Levels, Fractional Mode, $f_{PFD}$ = 66.3MHz, LDOV[1:0] = 3 | ●<br>● | | <br>18.2 | 1500<br>22 | µA<br>mA |
| $I_{CC(5V)}$ | Sum $V_{CP}^+$, $V_{VCO}^+$ Supply Currents | $I_{CP}$ = 11.2mA<br>$I_{CP}$ = 1.0mA<br>PDALL = 1 | ●<br>●<br>● | | 48<br>26<br>450 | 60<br>35<br>1000 | mA<br>mA<br>µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V unless otherwise specified (Note 2). All voltages are with respect to GND.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{CC(3.3V)}$ | Sum $V_{REF}^+$, $V_{RF}^+$ Supply Currents | RF Muted, OD[2:0] = 1<br>RF Enabled, RFO[1:0] = 0, OD[2:0] = 1<br>RF Enabled, RFO[1:0] = 3, OD[2:0] = 1<br>RF Enabled, RFO[1:0] = 3, OD[2:0] = 2<br>RF Enabled, RFO[1:0] = 3, OD[2:0] = 3<br>RF Enabled, RFO[1:0] = 3, OD[2:0] = 4 to 6<br>PDALL = 1 | ●<br>●<br>●<br>●<br>●<br>●<br>● | | 70.4<br>81.1<br>91.3<br>109.2<br>114.8<br>119.6<br>53 | 80<br>95<br>105<br>125<br>135<br>140<br>250 | mA<br>mA<br>mA<br>mA<br>mA<br>mA<br>µA |
| **Phase Noise and Spurious** | | | | | | | |
| $L_{VCO}$ | VCO Phase Noise (LTC6948-1, $f_{VCO}$ = 3.0GHz, $f_{RF}$ = 3.0GHz, OD[2:0] = 1 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –80<br>–130<br>–157 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-2, $f_{VCO}$ = 4.0GHz, $f_{RF}$ = 4.0GHz, OD[2:0] = 1 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –77<br>–127<br>–156 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 5.0GHz, OD[2:0] = 1 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –75<br>–126<br>–155 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-4, $f_{VCO}$ = 6.0GHz, $f_{RF}$ = 6.0GHz, OD[2:0] = 1 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –73<br>–123<br>–154 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 2.50GHz, OD[2 :0] = 2 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –81<br>–132<br>–155 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 1.667GHz, OD[2 :0] = 3 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –84<br>–135<br>–156 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 1.25GHz, OD[2 :0] = 4 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –87<br>–138<br>–156 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 1.00GHz, OD[2 :0] = 5 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –89<br>–140<br>–157 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| | VCO Phase Noise (LTC6948-3, $f_{VCO}$ = 5.0GHz, $f_{RF}$ = 0.833GHz, OD[2 :0] = 6 (Note 6)) | 10kHz Offset<br>1MHz Offset<br>40MHz Offset | | | –90<br>–141<br>–158 | | dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| $L_{NORM(INT)}$ | Integer Normalized In-Band Phase Noise Floor | INTN = 1, $I_{CP}$ = 5.6mA (Notes 7, 8, 10) | | | –226 | | dBc/Hz |
| $L_{NORM(FRAC)}$ | Fractional Normalized In-Band Phase Noise Floor | INTN = 0, CPLE = 1, $I_{CP}$ = 5.6mA (Notes 7, 8, 10) | | | –225 | | dBc/Hz |
| $L_{1/f}$ | Normalized In-Band 1/f Phase Noise | $I_{CP}$ = 11.2mA (Notes 7, 11) | | | –274 | | dBc/Hz |
| | In-Band Phase Noise Floor | Fractional Mode, CPLE = 1 (Notes 7, 9, 10, 12) | | | –113 | | dBc/Hz |
| | Integrated Phase Noise from 100Hz to 40MHz | Fractional Mode, CPLE = 1 (Notes 9, 12) | | | 0.14 | | °RMS |
| | Spurious | Fractional Mode, $f_{OFFSET} = f_{PFD}$, PLL locked (Notes 8, 13, 14) | | | –98 | | dBc |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6948I is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C.

## ELECTRICAL CHARACTERISTICS

**Note 3:** Valid for 1.60V ≤ V(TUNE) ≤ 2.85V with part calibrated after a power cycle or software power-on reset (POR).

**Note 4:** Based on characterization.

**Note 5:** For 0.9V < V(CP) < ($V_{CP}^+$ – 0.9V).

**Note 6:** Measured outside the loop bandwidth, using a narrowband loop, RFO[1:0] = 3.

**Note 7:** Measured inside the loop bandwidth with the loop locked.

**Note 8:** Reference frequency supplied by Wenzel 501-04516, $f_{REF}$ = 100MHz, $P_{REF}$ = 10dBm.

**Note 9:** Reference frequency supplied by Wenzel 500-23571, $f_{REF}$ = 61.44MHz, $P_{REF}$ = 10dBm.

**Note 10:** Output phase noise floor is calculated from normalized phase noise floor by $L_{OUT} = L_{NORM} + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{RF}/f_{PFD})$.

**Note 11:** Output 1/f noise is calculated from normalized 1/f phase noise by $L_{OUT(1/f)} = L_{1/f} + 20\log_{10}(f_{RF}) – 10\log10(f_{OFFSET})$.

**Note 12:** $I_{CP}$ = 5.6mA, $f_{PFD}$ = 61.44MHz, FILT[1:0] = 0, Loop BW = 180kHz; $f_{RF}$ = 2377.7MHz, $f_{VCO}$ = 4755.4MHz (LTC6948-3)

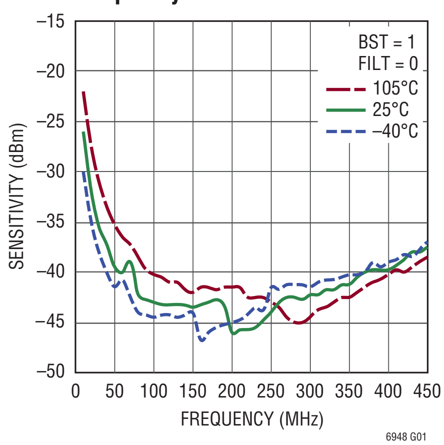
**Note 13:** $I_{CP}$ = 5.6mA, $f_{PFD}$ = 25MHz, FILT[1:0] = 0, Loop BW = 73kHz; $f_{RF}$ = 891.85MHz, $f_{VCO}$ = 2675Hz (LTC6948-1), $f_{VCO}$ = 4459MHz (LTC6948-2), $f_{VCO}$ = 5351MHz (LTC6948-3, LTC6948-4).

**Note 14:** Measured using DC1959.

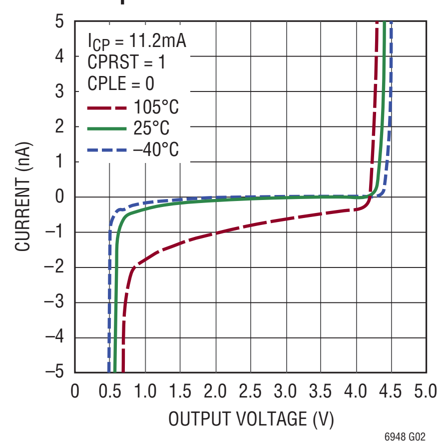
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.**

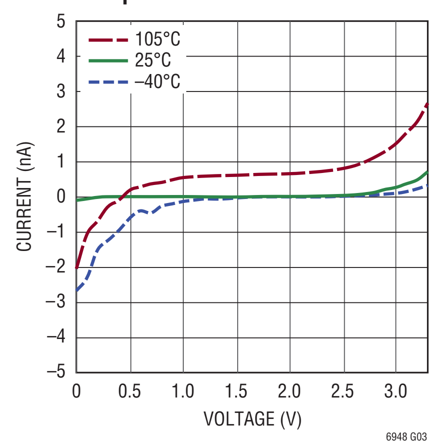
**REF Input Sensitivity vs Frequency**



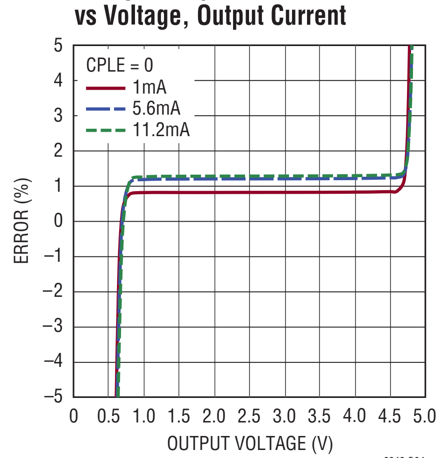

**CP Hi-Z Current vs Voltage, Temperature**



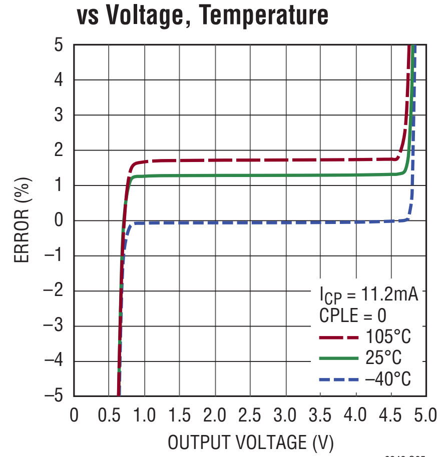

**TUNE Current vs Voltage, Temperature**



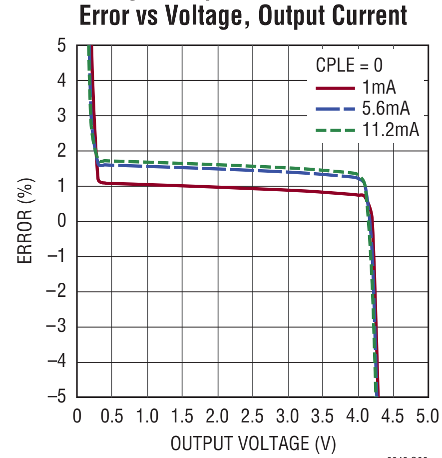

**Charge Pump Sink Current Error vs Voltage, Output Current**




**Charge Pump Sink Current Error vs Voltage, Temperature**




**Charge Pump Source Current Error vs Voltage, Output Current**

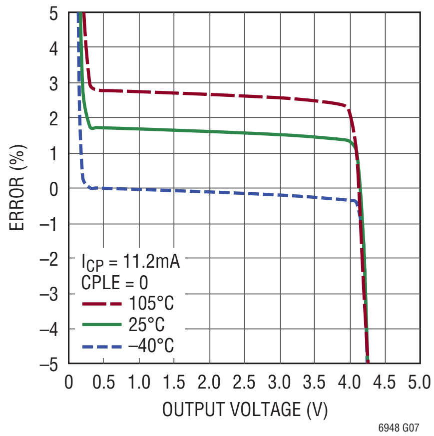



6948fa

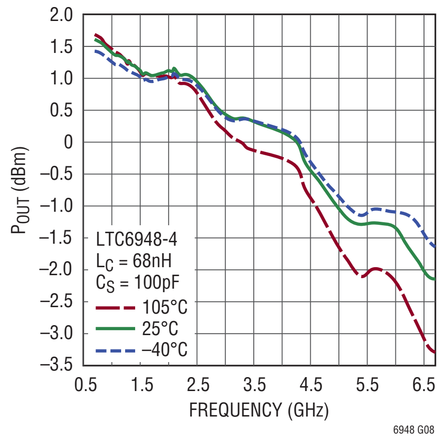
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C. $V_{REF}^+$ = $V_D^+$ = $V_{RF}^+$ = 3.3V, $V_{CP}^+$ = $V_{VCO}^+$ = 5V, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

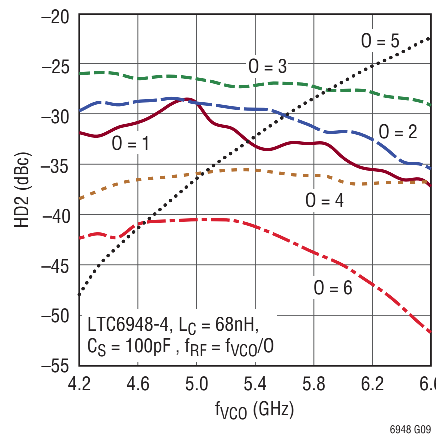
**Charge Pump Source Current Error vs Voltage, Temperature**



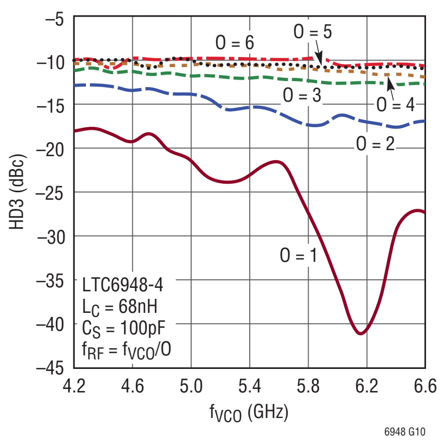

**RF Output Power vs Frequency (Single-Ended on RF+)**



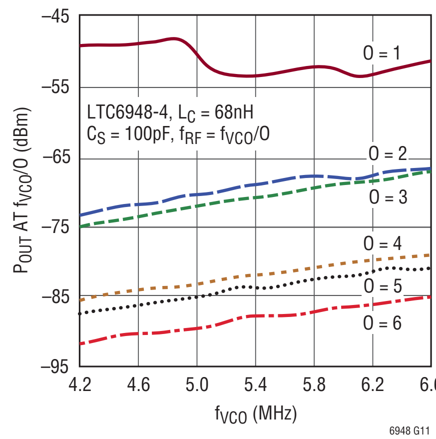

**RF Output HD2 vs Output Divide (Single-Ended on RF+)**



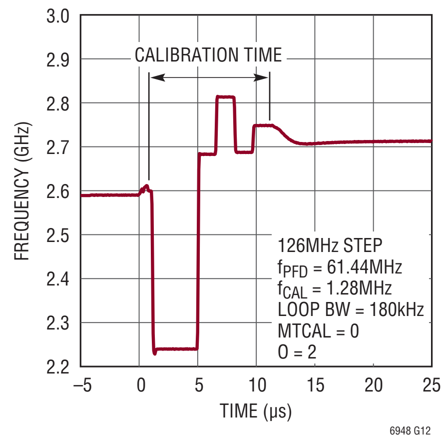

**RF Output HD3 vs Output Divide (Single-Ended on RF+)**



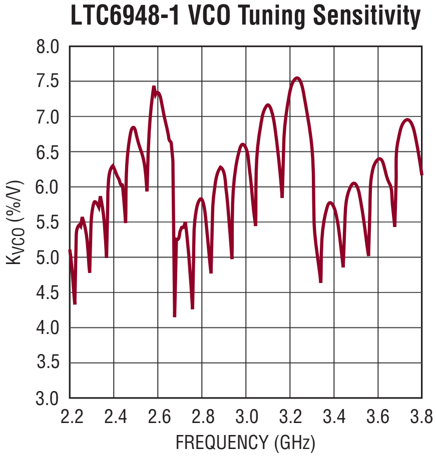

**MUTE Output Power vs $f_{VCO}$ and Output Divide (Single-Ended on RF+)**



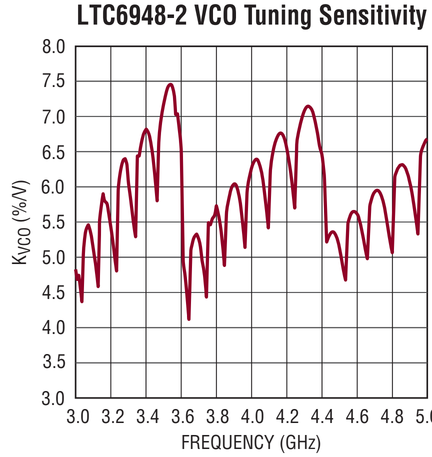

**LTC6948-3 Frequency Step Transient**



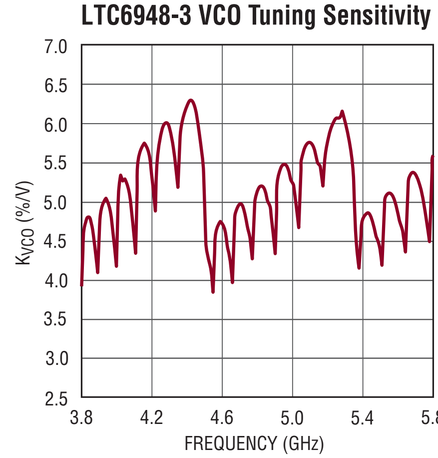

**LTC6948-1 VCO Tuning Sensitivity**




**LTC6948-2 VCO Tuning Sensitivity**



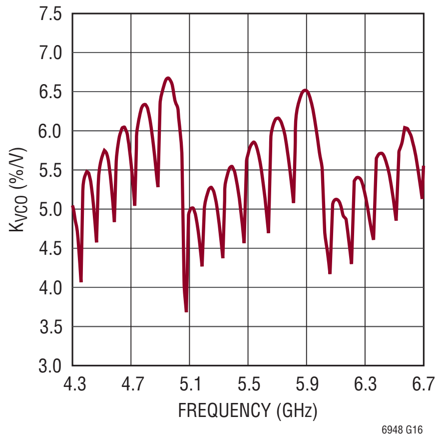

**LTC6948-3 VCO Tuning Sensitivity**



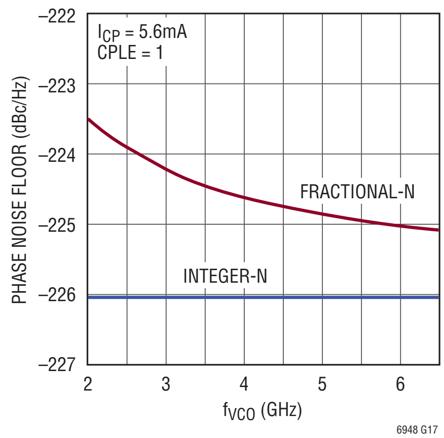
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$. $V_{REF}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

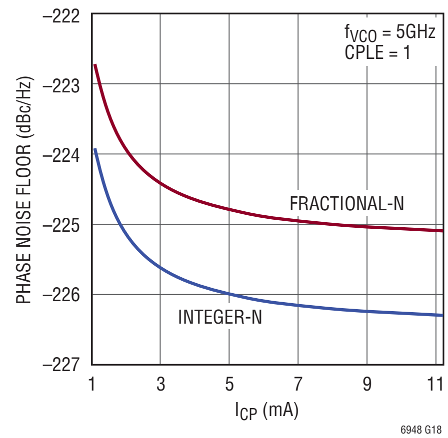
**LTC6948-4 VCO Tuning Sensitivity**



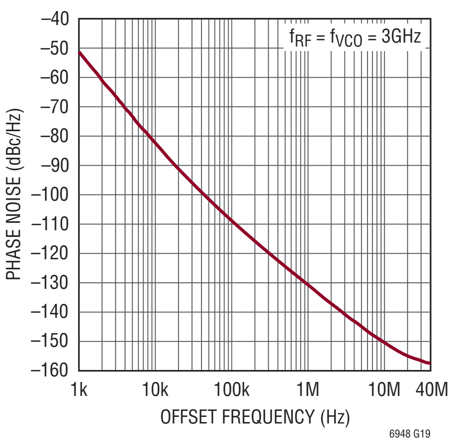

**Normalized In-Band Phase Noise Floor vs $f_{VCO}$**



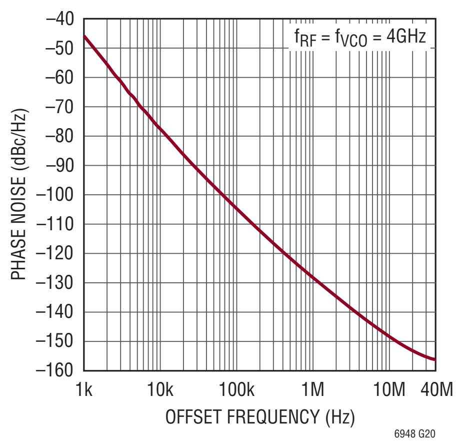

**Normalized In-Band Phase Noise Floor vs CP Current**



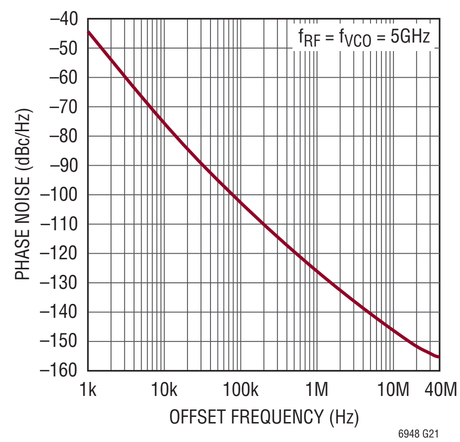

**LTC6948-1 VCO Phase Noise**



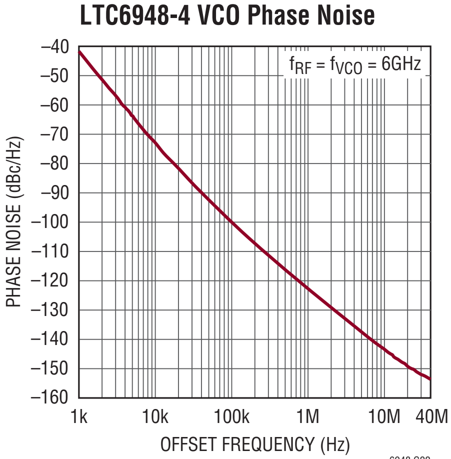

**LTC6948-2 VCO Phase Noise**



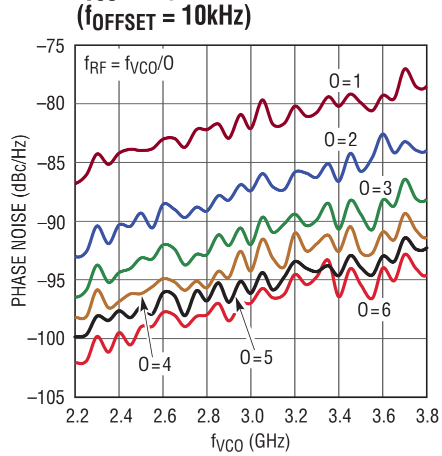

**LTC6948-3 VCO Phase Noise**



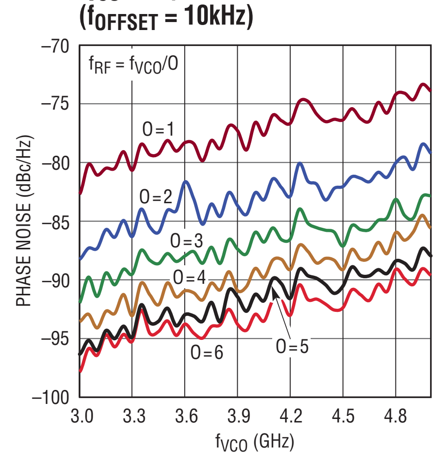

**LTC6948-4 VCO Phase Noise**




**LTC6948-1 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 10kHz)**



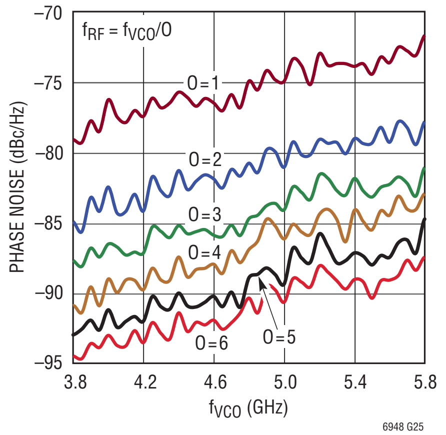

**LTC6948-2 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 10kHz)**



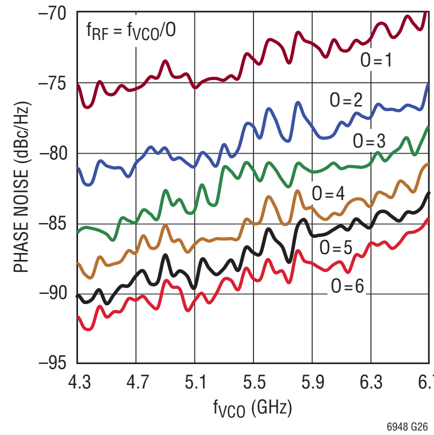
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$. $V_{REF}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

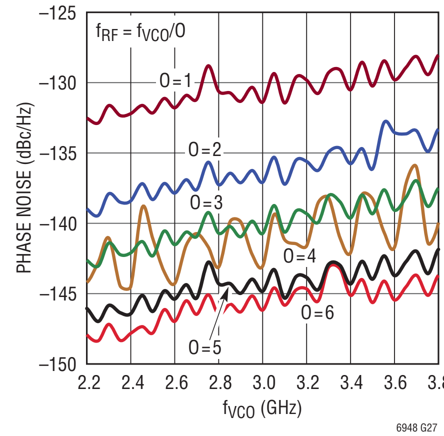
**LTC6948-3 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 10kHz)**



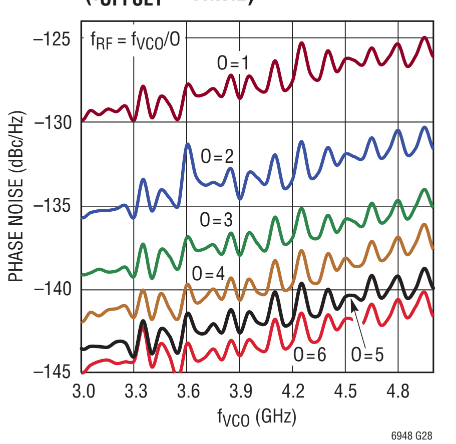

**LTC6948-4 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 10kHz)**



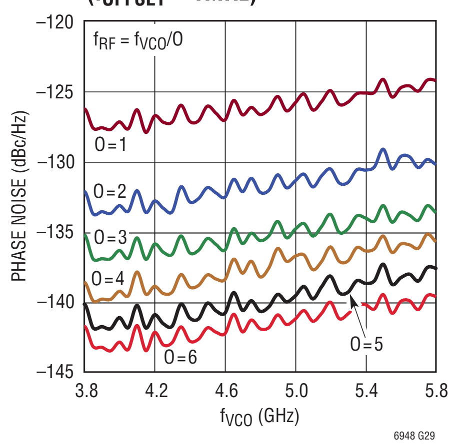

**LTC6948-1 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 1MHz)**



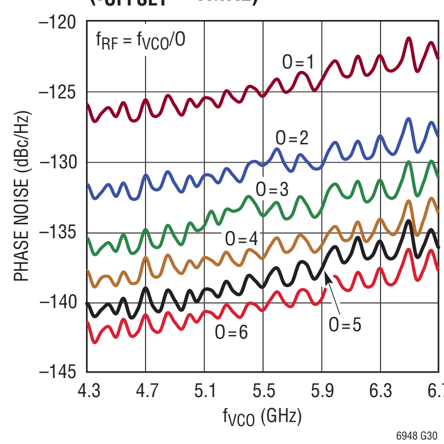

**LTC6948-2 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 1MHz)**



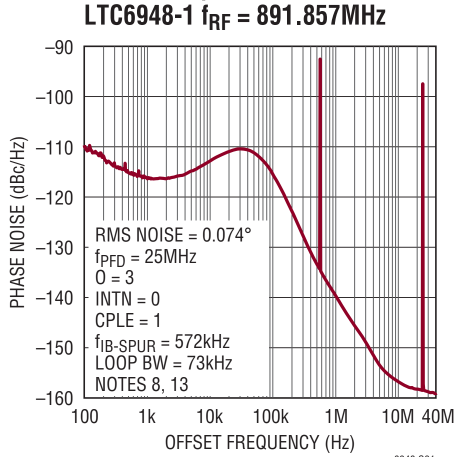

**LTC6948-3 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 1MHz)**



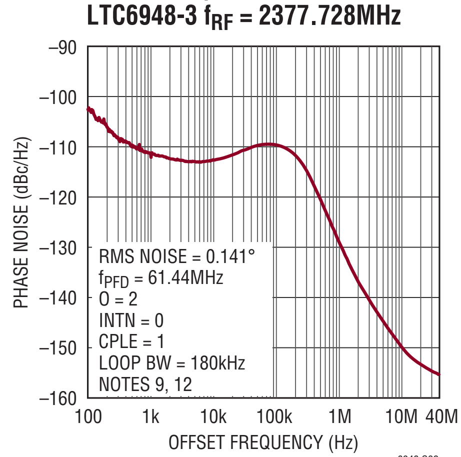

**LTC6948-4 VCO Phase Noise vs $f_{VCO}$, Output Divide ($f_{OFFSET}$ = 1MHz)**



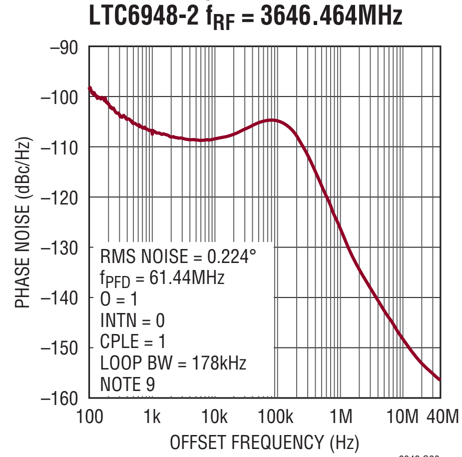

**Closed-Loop Phase Noise, LTC6948-1 $f_{RF}$ = 891.857MHz**




**Closed-Loop Phase Noise, LTC6948-3 $f_{RF}$ = 2377.728MHz**



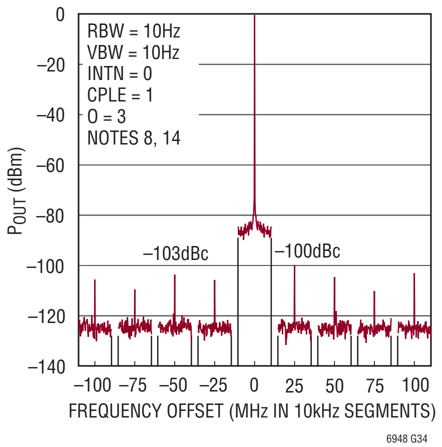

**Closed-Loop Phase Noise, LTC6948-2 $f_{RF}$ = 3646.464MHz**



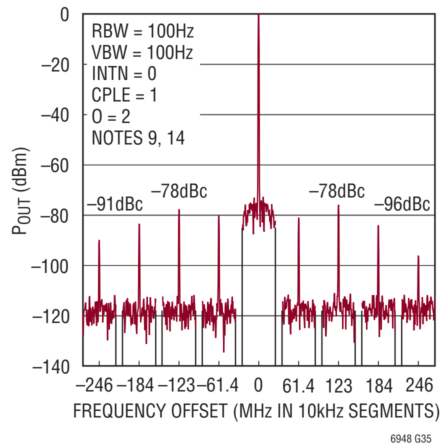
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C. $V_{REF}^+$ = $V_D^+$ = $V_{RF}^+$ = 3.3V, $V_{CP}^+$ = $V_{VCO}^+$ = 5V, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

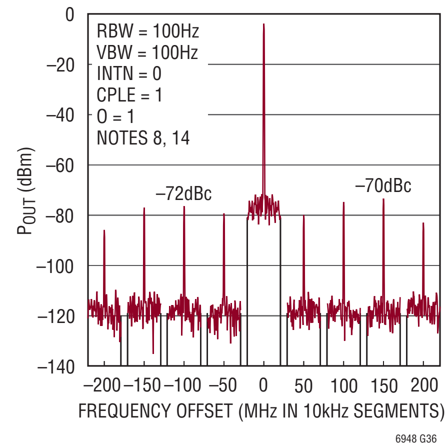
### LTC6948-1 Spurious Response $f_{RF}$ = 891.85MHz, $f_{REF}$ = 100MHz, $f_{PFD}$ = 25MHz, Loop BW = 74kHz



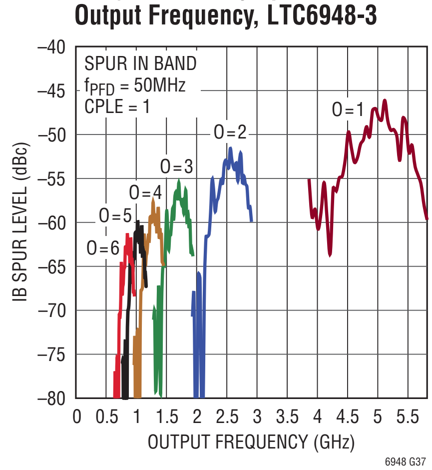

### LTC6948-3 Spurious Response $f_{RF}$ = 2377.73MHz, $f_{REF}$ = 61.44MHz, $f_{PFD}$ = 61.44MHz, Loop BW = 180k



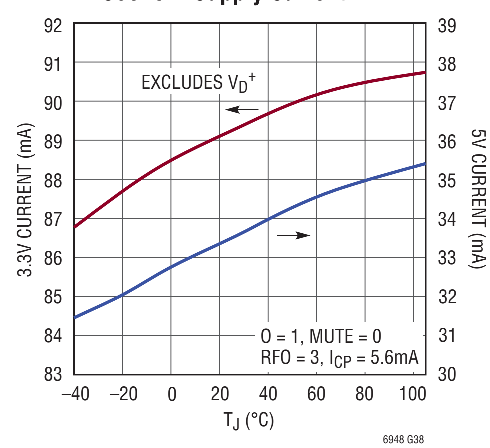

### LTC6948-4 Spurious Response $f_{RF}$ = 6236MHz, $f_{REF}$ = 100MHz, $f_{PFD}$ = 50MHz, Loop BW = 152kHz



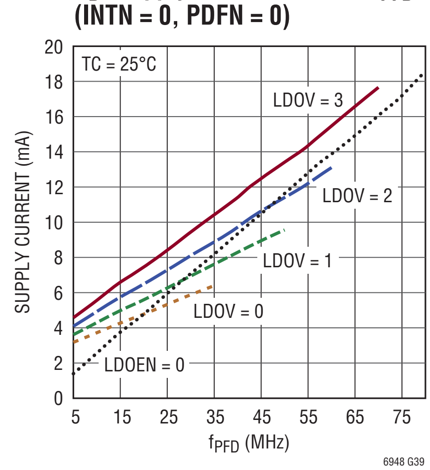

### Integer Boundary Spur Power vs Output Frequency, LTC6948-3



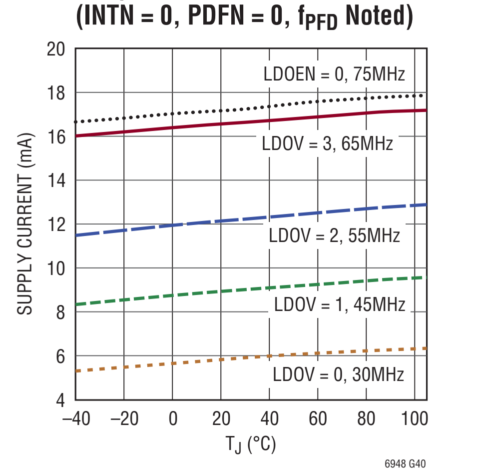

### LTC6948-4 Supply Current




### $V_D^+$ Supply Current vs LDOV, $f_{PFD}$ (INTN = 0, PDFN = 0)




### $V_D^+$ Supply Current vs LDOV, Temperature (INTN = 0, PDFN = 0, $f_{PFD}$ Noted)



## PIN FUNCTIONS

**$REF^+$, $REF^–$ (Pins 1, 28):** Reference Input Signals. This differential input is buffered with a low noise amplifier, which feeds the reference divider. They are self-biased and must be AC-coupled with 1µF capacitors. If used single-ended with $V_{REF}^+ \leq 2.7V_{P-P}$, bypass $REF^–$ to GND with a 1µF capacitor. If used single-ended with $V_{REF}^+ > 2.7V_{P-P}$, bypass $REF^–$ to GND with a 47pF capacitor.

**STAT (Pin 2):** Status Output. This signal is a configurable logical OR combination of the UNLOK, LOK, ALCHI, ALCLO, THI, and TLO status bits, programmable via the STATUS register. See the Operation section for more details.

**$\overline{CS}$ (Pin 3):** Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high. See the Operation section for more details.

**SCLK (Pin 4):** Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Operation section for more details.

**SDI (Pin 5):** Serial Port Data Input. The serial port uses this CMOS input for data. See the Operation section for more details.

**SDO (Pin 6):** Serial Port Data Output. This CMOS three-state output presents data from the serial port during a read communication burst. Optionally attach a resistor of >200k to GND to prevent a floating output. See the Applications Information section for more details.

**LDO (Pin 7):** ΔΣ Modulator LDO Bypass Pin. This pin should be bypassed directly to the ground plane using a low ESR (<0.8Ω) 0.1µF ceramic capacitor as close to the pin as possible.

**$V_D^+$ (Pin 8):** 3.15V to 3.45V Positive Supply Pin for Serial Port and ΔΣ Modulator Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

**$\overline{MUTE}$ (Pin 9):** RF Mute. The CMOS active-low input mutes the $RF^\pm$ differential outputs while maintaining internal bias levels for quick response to deassertion.

**GND (Pins 10, 17, 21, Exposed Pad Pin 29):** Negative Power Supply (Ground). These pins should be tied directly to the ground plane with multiple vias for each pin. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

**$RF^–$, $RF^+$ (Pins 11, 12):** RF Output Signals. The VCO output divider is buffered and presented differentially on these pins. The outputs are open-collector, with 136Ω (typical) pull-up resistors tied to $V_{RF}^+$ to aid impedance matching. If used single-ended, the unused output should be terminated to 50Ω. See the Applications Information section for more details on impedance matching.

**$V_{RF}^+$ (Pin 13):** 3.15V to 3.45V Positive Supply Pin for RF circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

**BB (Pin 14):** RF Reference Bypass. This output has a 2.5k resistance and must be bypassed with a 1µF ceramic capacitor to GND. Do not couple this pin to any other signal.

**TUNE (Pin 15):** VCO Tuning Input. This frequency control pin is normally connected to the external loop filter. See the Applications Information section for more details.

## PIN FUNCTIONS

**TB (Pin 16):** VCO Bypass. This output has a 2k resistance and must be bypassed with a 2.2µF ceramic capacitor to GND. It is normally connected to $CM_A$, $CM_B$, and $CM_C$ with a short trace. Do not couple this pin to any other signal.

**$CM_A$, $CM_B$, $CM_C$ (Pins 18, 19, 20):** VCO Bias Inputs. These inputs are normally connected to TB with a short trace and bypassed with a 2.2µF ceramic capacitor to GND. Do not couple these pins to any other signal. *For best phase noise performance, DO NOT place a trace between these pads underneath the package.*

**BVCO (Pin 22):** VCO Bypass Pin. This output must be bypassed with a 1µF ceramic capacitor to GND. Do not couple this pin to any other signal.

**$V_{VCO}^+$ (Pin 23):** 4.75V to 5.25V Positive Supply Pin for VCO Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

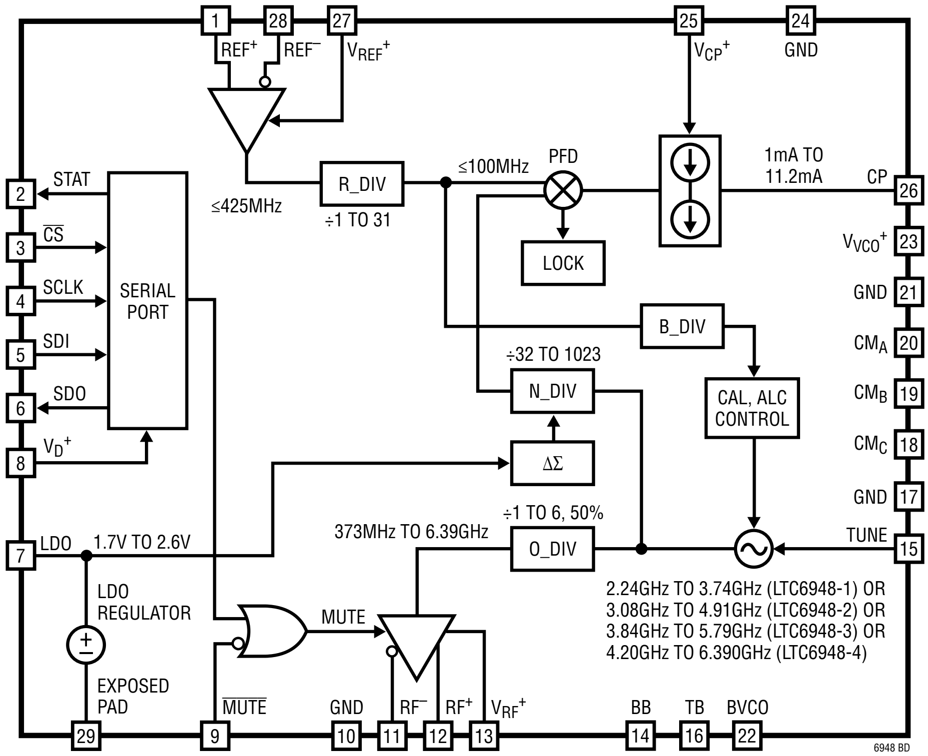
**GND (24):** Negative Power Supply (Ground). This pin is attached directly to the die attach paddle (DAP) and should be tied directly to the ground plane.

**$V_{CP}^+$ (Pin 25):** 4V to 5.25V Positive Supply Pin for Charge Pump Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

**CP (Pin 26):** Charge Pump Output. This bidirectional current output is normally connected to the external loop filter. See the Applications Information section for more details.

**$V_{REF}^+$ (Pin 27):** 3.15V to 3.45V Positive Supply Pin for Reference Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

# BLOCK DIAGRAM



# OPERATION

The LTC6948 is a high-performance fractional-N PLL complete with a low noise VCO available in four different frequency range options. The output frequency range may be further extended by utilizing the output divider (see Available Options table for more details). The device is able to achieve superior integrated phase noise by the combination of its extremely low in-band phase noise performance and excellent VCO noise characteristics.

The fractional-N feedback divider uses an advanced ΔΣ modulator, resulting in virtually no discrete modulator spurious tones. The modulator may be disabled if integer-N feedback is required.

## REFERENCE INPUT BUFFER

The PLL's reference frequency is applied differentially on pins $REF^+$ and $REF^-$. These high impedance inputs are self-biased and must be AC-coupled with 1µF capacitors (see Figure 1 for a simplified schematic). Alternatively, the inputs may be used single-ended by applying the reference frequency at $REF^+$ and bypassing $REF^-$ to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, then use a 47pF capacitor for the GND bypass.

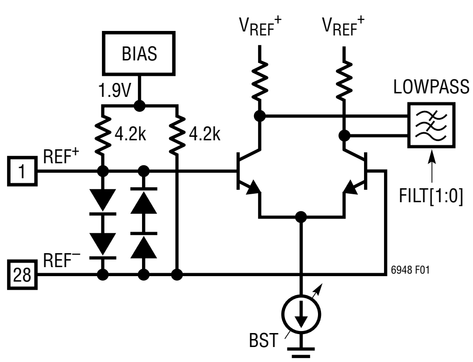



**Figure 1. Simplified REF Interface Schematic**

A high quality signal must be applied to the REF± inputs as they provide the frequency reference to the entire PLL. To achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

Additional options are available through serial port register h0B to further refine the application. Bits FILT[1:0] control the reference input buffer's lowpass filter, and should be set based upon $f_{REF}$ to limit the reference's wideband noise. The FILT[1:0] bits must be set correctly to reach the $L_{NORM}$ normalized in-band phase noise floor. See Table 1 for recommended settings.

**Table 1. FILT[1:0] Programming**

| FILT[1:0] | $f_{REF}$ |
|---|---|
| 3 | <20MHz |
| 2 | NA |
| 1 | 20MHz to 50MHz |
| 0 | >50MHz |

The BST bit should be set based upon the input signal level to prevent the reference input buffer from saturating. See Table 2 for recommended settings and the Applications Information section for programming examples.

**Table 2. BST Programming**

| BST | $V_{REF}$ |
|---|---|
| 1 | $<2V_{P-P}$ |
| 0 | $\geq 2V_{P-P}$ |

## REFERENCE (R) DIVIDER

A 5-bit divider, R_DIV, is used to reduce the frequency seen at the PFD. Its divide ratio R may be set to any integer from 1 to 31, inclusive. Use the RD[4:0] bits found in registers h06 to directly program the R divide ratio. See the Applications Information section for the relationship between R and the $f_{REF}$, $f_{PFD}$, $f_{VCO}$, and $f_{RF}$ frequencies.

## PHASE/FREQUENCY DETECTOR (PFD)

The phase/frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase-lock the loop, forcing a phase align-

## OPERATION

ment at the PFD's inputs. The PFD may be disabled with the CPRST bit which prevents UP and DOWN pulses from being produced. See Figure 2 for a simplified schematic of the PFD.

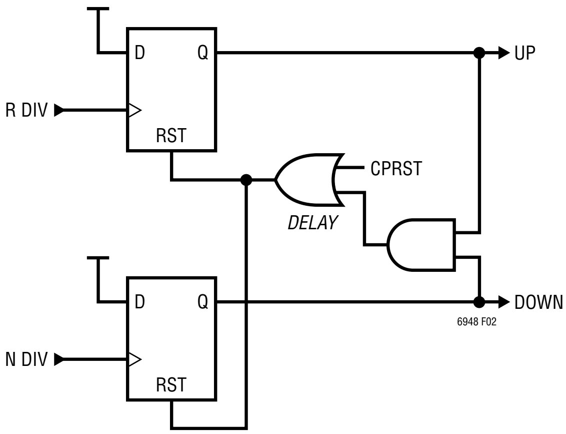



**Figure 2. Simplified PFD Schematic**

### LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by programming LKCT[1:0] in the serial port register h0C (see Table 5), and produces both LOCK and UNLOCK status flags, available through both the STAT output and serial port register h00.

The user sets the phase difference lock window time $t_{LWW}$ for a valid LOCK condition with the LKWIN[2:0] bits. When using the device as a fractional-N synthesizer (fractional mode), the $\Delta\Sigma$ modulator changes the instantaneous phase seen at the PFD on every R_DIV and N_DIV cycle. The maximum allowable time difference in this case depends upon both the VCO frequency $f_{VCO}$ and also the charge pump linearization enable bit CPLE (see the Charge Pump Linearizer section for an explanation of this function). Table 3 contains recommended settings for LKWIN[2:0] when using the device in fractional mode. See the Applications Information section for examples.

**Table 3. LKWIN[2:0] Fractional Mode Programming**

| LKWIN[2:0] | $t_{LWW}$ | $f_{VCO}$ (CPLE = 1) | $f_{VCO}$ (CPLE = 0) |
|---|---|---|---|
| 0 | 5.0ns | ≥2.97GHz | ≥1.35GHz |
| 1 | 7.35ns | ≥2.00GHz | ≥919MHz |
| 2 | 10.7ns | ≥1.39GHz | ≥632MHz |
| 3 | 15.8ns | ≥941MHz | ≥428MHz |
| 4 | 23.0ns | ≥646MHz | ≥294MHz |
| 5 | 34.5ns | ≥431MHz | ≥196MHz |
| 6 | 50.5ns | ≥294MHz | ≥134MHz |
| 7 | 76.0ns | ≥196MHz | ≥89MHz |

When using the device as an integer-N synthesizer (integer mode), the phase difference seen at the PFD is minimized by the feedback of the PLL and no longer depends upon $f_{VCO}$. Table 4 contains recommended settings for different $f_{PFD}$ frequencies. See the Applications Information section for examples.

**Table 4. LKWIN[2:0] Integer Mode Programming**

| LKWIN[2:0] | $t_{LWW}$ | $f_{PFD}$ |
|---|---|---|
| 0 | 5.0ns | >6.8MHz |
| 1 | 7.35ns | ≤6.8MHz |
| 2 | 10.7ns | ≤4.7MHz |
| 3 | 15.8ns | ≤3.2MHz |
| 4 | 23.0ns | ≤2.2MHz |
| 5 | 34.5ns | ≤1.5MHz |
| 6 | 50.5ns | ≤1.0MHz |
| 7 | 76.0ns | ≤660kHz |

The PFD phase difference must be less than $t_{LWW}$ for the COUNTS number of successive counts before the lock indicator asserts the LOCK flag. The LKCT[1:0] bits found in register h0C are used to set COUNTS depending upon the application. Set LKCT to 0 to disable the lock indicator. See Table 5 for LKCT[1:0] programming and the Applications Information section for examples.

# OPERATION

**Table 5. LKCT[1:0] Programming**

| LKCT[1:0] | COUNTS |
|---|---|
| 0 | Lock Indicator Disabled |
| 1 | 32 |
| 2 | 256 |
| 3 | 2048 |

When the PFD phase difference is greater than $t_{LWW}$, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than $t_{LWW}$. See Figure 3 for more details.

*Note that $f_{REF}$ must be present for the LOCK and UNLOCK flags to properly assert and clear.*

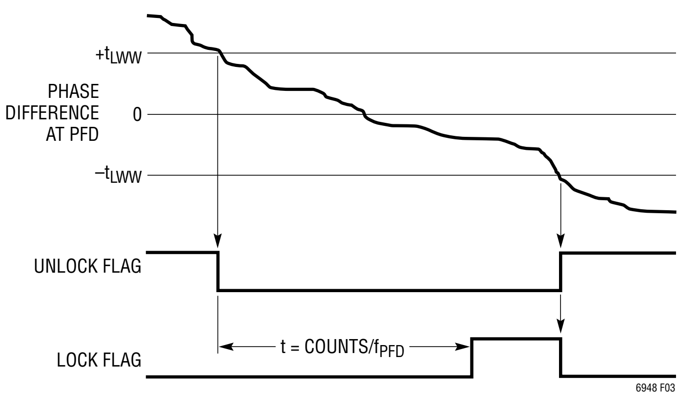



**Figure 3. UNLOCK and LOCK Timing**

## CHARGE PUMP

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin, which should be connected to an appropriate loop filter. See Figure 4 for a simplified schematic of the charge pump.

The output current magnitude $I_{CP}$ may be set from 1mA to 11.2mA using the CP[2:0] bits found in serial port register h0C. A larger $I_{CP}$ can result in lower in-band noise due to the lower impedance of the loop filter components, although currents larger than 5.6mA typically cause worse spurious performance. See Table 6 for programming specifics and the Applications Information section for loop filter examples.

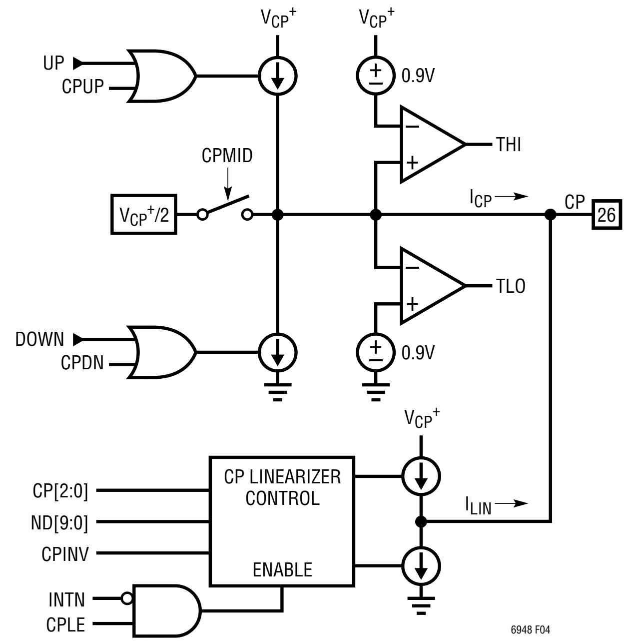



**Figure 4. Simplified Charge Pump Schematic**

**Table 6. CP[2:0] Programming**

| CP[2:0] | $I_{CP}$ |
|---|---|
| 0 | 1.0mA |
| 1 | 1.4mA |
| 2 | 2.0mA |
| 3 | 2.8mA |
| 4 | 4.0mA |
| 5 | 5.6mA |
| 6 | 8.0mA |
| 7 | 11.2mA |

The CPINV bit found in register h0D should be set for applications requiring signal inversion from the PFD, such as for complex external loops using an inverting op amp. A passive loop filter as shown in Figure 13 requires CPINV = 0.

## OPERATION

### Charge Pump Functions

The charge pump contains additional features to aid in system startup. See Table 7 below for a summary.

**Table 7. Charge Pump Function Bit Descriptions**

| BIT | DESCRIPTION |
|---|---|
| CPCHI | Enable High Voltage Output Clamp |
| CPCLO | Enable Low Voltage Output Clamp |
| CPDN | Force Sink Current |
| CPINV | Invert PFD Phase |
| CPLE | Linearizer Enable |
| CPMID | Enable Mid-Voltage Bias |
| CPRST | Reset PFD |
| CPUP | Force Source Current |
| CPWIDE | Extend Current Pulse Width |
| THI | High Voltage Clamp Flag |
| TLO | Low Voltage Clamp Flag |

The CPCHI and CPCLO bits found in register h0D enable the high and low voltage clamps, respectively. When CPCHI is enabled and the CP pin voltage exceeds approximately $V_{CP}^+$ – 0.9V, the THI status flag is set, and the charge pump sourcing current is disabled. Alternately, when CPCLO is enabled and the CP pin voltage is less than approximately 0.9V, the TLO status flag is set, and the charge pump sinking current is disabled. See Figure 4 for a simplified schematic.

The CPMID bit also found in register h0D enables a resistive $V_{CP}^+/2$ output bias which may be used to pre-bias troublesome loop filters into a valid voltage range. When using CPMID, it is recommended to also assert the CPRST bit, forcing a PFD reset. Both CPMID and CPRST must be set to 0 for normal operation.

The CPUP and CPDN bits force a constant $I_{CP}$ source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with the CPUP and CPDN bits, allowing a precharge of the loop to a known state, if required. CPUP, CPDN, and CPRST must be set to 0 to allow the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value (see Figure 2). CPWIDE is normally set to 0.

### Charge Pump Linearizer

When the LTC6948 is operated in fractional mode, the charge pump's current output versus its phase stimulus (its gain linearity) must be extremely accurate. The CP gain linearizer automatically adds a correction current $I_{LIN}$ to minimize the charge pump's impact on in-band phase noise and spurious products during fractional operation.

The CP gain linearizer is enabled by setting CPLE = 1. It is automatically disabled when in integer mode. CPLE should be set to 0 if CPRST or CPMID are asserted to prevent the linearizer from producing unintended currents.

### VCO

The integrated VCO is available in one of four frequency ranges. The output frequency range may be further extended by utilizing the output divider (see Available Options table, for more details). The wide frequency range of the VCO, coupled with the output divider capability, allows the LTC6948 to cover an extremely wide range of continuously selectable frequencies.

The BB and TB pins are used to bias internal VCO circuitry. The BB pin has a 2k output resistance and should be bypassed with a 1μF ceramic capacitor to GND, giving a time constant of 2ms. The TB pin has a 2.5k output resistance and should be bypassed with a 2.2μF ceramic capacitor to GND, resulting in a time constant of 5.5ms. Stable bias voltages are achieved after approximately 3 time constants following power-up.

### VCO Calibration

*The VCO must be calibrated each time its frequency is changed* by changing any of $f_{REF}$, the R divider value, the N divider value, or ΔΣ modulator fractional value, but not the O divider (see the Applications Information section

## OPERATION

for the relationship between R, N, NUM, O, and the $f_{REF}$, $f_{PFD}$, $f_{VCO}$, and $f_{RF}$ frequencies). *The output frequency is then stable over the LTC6948's entire temperature range, regardless of the temperature at which it was calibrated, until the part is reset due to a power cycle or software power-on reset (POR).*

The output of the B divider is used to clock digital calibration circuitry as shown in the Block Diagram. The B value, programmed with bits BD[3:0], and $f_{PFD}$ determine the calibration frequency $f_{CAL}$. Calculate the B value using Equation 1.

$$B \geq \frac{f_{PFD}}{f_{CAL\text{-}MAX}} \quad (1)$$

The maximum calibration frequency $f_{CAL\text{-}MAX}$ for each part option is shown in Table 8.

**Table 8. Maximum Calibration Frequency**

| PART | $f_{CAL\text{-}MAX}$ (MHz) |
|---|---|
| LTC6948-1 | 1.0 |
| LTC6948-2 | 1.33 |
| LTC6948-3 | 1.7 |
| LTC6948-4 | 1.8 |

The relationship between bits BD(3:0) and the B value is shown in Table 9.

**Table 9. BD[3:0] Programming**

| BD[3:0] | B DIVIDE VALUE |
|---|---|
| 0 | 8 |
| 1 | 12 |
| 2 | 16 |
| 3 | 24 |
| 4 | 32 |
| 5 | 48 |
| 6 | 64 |
| 7 | 96 |
| 8 | 128 |
| 9 | 192 |
| 10 | 256 |
| 11 | 384 |
| 12 to 15 | Invalid |

Once the RD[4:0], ND[9:0], NUM[17:0], and BD[3:0] bits are written and the reference frequency $f_{REF}$ is present and stable at the $REF^{\pm}$ inputs, the VCO must be calibrated by setting CAL = 1 (the bit is self-clearing). The calibration cycle takes between 12 and 14 clocks of the B divider output. The MTCAL bit may be set to mute the RF output during the calibration.

*Note that the $f_{REF}$ frequency and TB and BB voltages must be stable for proper calibration.* Stable bias voltages are achieved after approximately 3 time constants following power-up.

Setting AUTOCAL = 1 causes the CAL bit to be set automatically whenever any of serial port registers h06 through h0A is written. When AUTOCAL is enabled, there is no need for a separate register write to set the CAL bit. See Table 10 for a summary of the VCO bits.

**Table 10. VCO Bit Descriptions**

| BIT | DESCRIPTION |
|---|---|
| AUTOCAL | Calibrate VCO Whenever Registers h06 to h0A Are Written |
| CAL | Start VCO Calibration (Auto Clears) |
| MTCAL | Mute RF Output During Calibration |

### VCO Automatic Level Control (ALC)

The VCO uses an internal automatic level control (ALC) algorithm to maintain an optimal amplitude on the VCO resonator, and thus optimal phase noise performance. The user has several ALC configuration and status reporting options as seen in Table 11.

**Table 11. ALC Bit Descriptions**

| BIT | DESCRIPTION |
|---|---|
| ALCCAL | Auto Enable ALC during CAL operation |
| ALCEN | Always Enable ALC (Overrides ALCCAL, ALCMON, and ALCULOK) |
| ALCHI | ALC too High Flag (Resonator Amplitude too High) |
| ALCLO | ALC too Low Flag (Resonator Amplitude too Low) |
| ALCMON | Enable ALC Monitoring for Status Flags Only; Does Not Enable Amplitude Control |
| ALCULOK | Auto Enable ALC when PLL Unlocked |

## OPERATION

Changes in the internal ALC output can cause extremely small jumps in the VCO frequency. These jumps may be acceptable in some applications but not in others. Use the above table to choose when the ALC is active. The ALCHI and ALCLO flags, valid only when the ALC is active or the ALCMON bit is set, may be used to monitor the resonator amplitude.

*The ALC must be allowed to operate during or after a calibration cycle. At least one of the ALCCAL, ALCEN, or ALCULOK bits must be set.*

### VCO (N) DIVIDER

The 10-bit N divider provides the feedback from the VCO to the PFD. Its divide ratio N is restricted to any integer from 35 to 1019, inclusive, when in fractional mode. The divide ratio may be programmed from 32 to 1023, inclusive, when in integer mode. Use the ND[9:0] bits found in registers h06 and h07 to directly program the N divide ratio. See the Applications Information section for the relationship between N and the $f_{REF}$, $f_{PFD}$, $f_{VCO}$, and $f_{RF}$ frequencies.

### ΔΣ MODULATOR

The ΔΣ modulator changes the N divider's ratio each PFD cycle to achieve an average fractional divide ratio. The fractional numerator NUM[17:0] is programmable from 1 to 262143, or $2^{18} – 1$. The fractional denominator is fixed at 262144 (or $2^{18}$), with the resulting fractional ratio F given by Equation 4. See the Applications Information section for the relationship between NUM, F, and the $f_{REF}$, $f_{PFD}$, $f_{VCO}$, and $f_{RF}$ frequencies.

The ΔΣ modulator uses digital signal processing (DSP) techniques to achieve an average fractional divide ratio. The modulator is clocked at the $f_{PFD}$ rate. This process produces output modulation noise known as quantization noise with a highpass frequency response. The external lowpass loop filter is used to filter this quantization noise to a level beneath the phase noise of the VCO. This prevents the noise from contributing to the overall phase noise of the system. The loop filter must be designed to adequately filter the quantization noise.

The oversampling ratio OSR is defined as the ratio of the ΔΣ modulator clock frequency $f_{PFD}$ to the loop bandwidth BW of the PLL (see Equation 11). See the Applications Information section for guidelines concerning the OSR and the loop filter.

When the desired output frequency is such that the needed NUM value is 0, the LTC6948 should be operated in integer mode (INTN = 1). In integer mode, the modulator is placed in standby, with all blocks still powered up, thus allowing it to resume fractional operation immediately.

Enable numerator dither mode (DITHEN = 1) to further reduce spurious produced by the modulator. Dither has no measurable impact on in-band phase noise, and is enabled by default. See Table 12 for a complete list of modulator bit descriptions.

#### Modulator Reset

To achieve consistent spurious performance, the modulator DSP circuitry should be re-initialized by setting RSTFN = 1 whenever NUM[17:0] is changed. Setting AUTORST = 1 causes the RSTFN bit to be set automatically whenever any of serial port registers h05 through h0A are written. When AUTORST is enabled, there is no need for a separate register write to set the RSTFN bit. See Table 12 for a summary of the modulator bits.

**Table 12. Fractional Modulator Bit Descriptions**

| BIT | DESCRIPTION |
|---|---|
| AUTORST | Automatically Reset Modulator when Registers h05 to h0A Are Written |
| DITHEN | Enable Fractional Numerator Dither |
| INTN | Integer Mode; Fractional Modulator Placed in Standby |
| RSTFN | Reset Modulator (Auto Clears) |
| SEED | Seed Value for Pseudorandom Dither Algorithm |

## OPERATION

### LDO REGULATOR

The adjustable low dropout (LDO) regulator supplies power to the ΔΣ modulator. The regulator requires a low ESR ceramic capacitor (ESR < 0.8Ω) connected to the LDO pin (pin 7) for stability. The capacitor value may range from 0.047μF to 1μF.

The LDO voltage is set using the LDOV[1:0] bits, and should be chosen based upon the $f_{PFD}$ frequency to minimize power and spurious. The regulator is disabled by setting the LDOEN bit to 0. When disabled by using either the LDOEN or PDFN bits, the LDO pin is connected directly to $V_D^+$ using a low impedance switch, and the regulator is powered down. See Table 13 for programming details.

**Table 13. LDOV[1:0] and LDOEN Programming**

| LDOV[1:0] | LDOEN | $V_{LDO}$ | $f_{PFD}$ |
|---|---|---|---|
| 0 | 1 | 1.7V | ≤34.3MHz |
| 1 | 1 | 2.0V | ≤45.9MHz |
| 2 | 1 | 2.3V | ≤56.1MHz |
| 3 | 1 | 2.6V | ≤66.3MHz |
| X | 0 | $V_D^+$ | ≤76.1MHz |

### OUTPUT (O) DIVIDER

The 3-bit O divider can reduce the frequency from the VCO to extend the output frequency range. Its divide ratio O may be set to any integer from 1 to 6, inclusive, outputting a 50% duty cycle even with odd divide values. Use the OD[2:0] bits found in register h0B to directly program the O divide ratio. See the Applications Information section for the relationship between O and the $f_{REF}$, $f_{PFD}$, $f_{VCO}$, and $f_{RF}$ frequencies.

### RF OUTPUT BUFFER

The low noise, differential output buffer produces a differential output power of –4.3dBm to +4.5dBm, settable with bits RFO[1:0] according to Table 14. The outputs may be combined externally, or used individually. Terminate any unused output with a 50Ω resistor to $V_{RF}^+$.

**Table 14. RFO[1:0] Programming**

| RFO[1:0} | $P_{RF}$ (DIFFERENTIAL) | $P_{RF}$ (SINGLE-ENDED) |
|---|---|---|
| 0 | –4.3dBm | –7.3dBm |
| 1 | –1.5dBm | –4.5dBm |
| 2 | 1.6dBm | –1.4dBm |
| 3 | 4.5dBm | 1.5dBm |

Each output is open-collector with 136Ω pull-up resistors to $V_{RF}^+$, easing impedance matching at high frequencies. See Figure 5 for circuit details and the Applications Information section for matching guidelines. The buffer may be muted with either the OMUTE bit, found in register h02, or by forcing the $\overline{MUTE}$ input low.

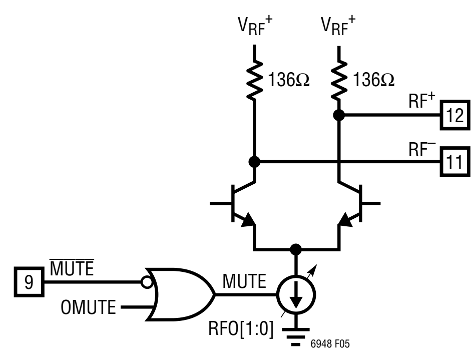



**Figure 5. Simplified RF Interface Schematic**

### SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality. A configurable status output STAT gives additional instant monitoring.

#### Communication Sequence

The serial bus is comprised of $\overline{CS}$, SCLK, SDI, and SDO. Data transfers to the part are accomplished by the serial bus master device first taking $\overline{CS}$ low to enable the LTC6948's port. Input data applied on SDI is clocked on

## OPERATION

the rising edge of SCLK, with all transfers *MSB first*. The communication burst is terminated by the serial bus master returning $\overline{CS}$ high. See Figure 6 for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC6948 connected in parallel on the serial bus), as SDO is three-stated (Hi-Z) when $\overline{CS}$ = 1, or when data is not being read from the part. *If the LTC6948 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a high value resistor of greater than 200k between SDO and GND to ensure the line returns to a known level during Hi-Z states.* See Figure 7 for details.

### Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 15 byte-wide registers. All data bursts are comprised of at least two bytes. The seven most significant bits of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 8 for an example of a detailed write sequence, and Figure 9 for a read sequence.

Figure 10 shows an example of two write communication bursts. The first byte of the first burst sent from the serial bus master on SDI contains the destination register address

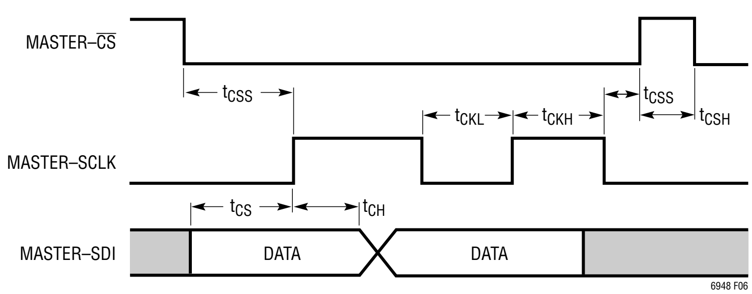



**Figure 6. Serial Port Write Timing Diagram**

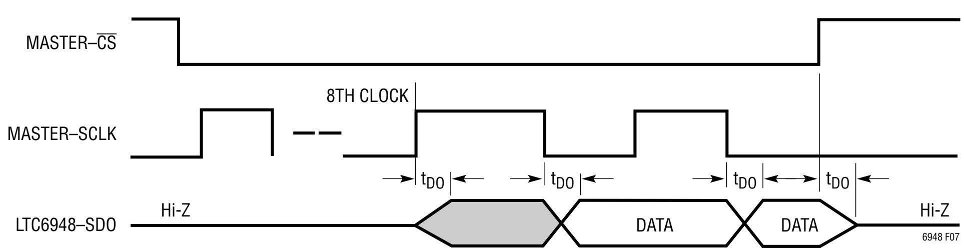



**Figure 7. Serial Port Read Timing Diagram**

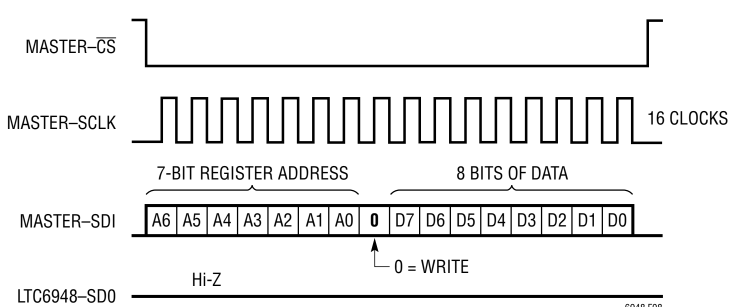



**Figure 8. Serial Port Write Sequence**

## OPERATION

(Addr0) and an LSB of 0 indicating a write. The next byte is the data intended for the register at address Addr0. $\overline{CS}$ is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (Addr1) and an LSB indicating a write. The next byte on SDI is the data intended for the register at address Addr1. $\overline{CS}$ is then taken high to terminate the transfer.

### Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC6948's register address auto-increment feature as shown in Figure 11. The serial port master sends the destination register address in the first byte and its data in the second byte as before, but continues sending bytes destined for subsequent registers. Byte 1's address is Addr0+1, Byte 2's address is Addr0+2, and so on. If the register address pointer attempts to increment past 14 (h0E), it is automatically reset to 0.

An example of an auto-increment read from the part is shown in Figure 12. The first byte of the burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of 1 indicating a read. Once the LTC6948 detects a read burst, it takes SDO out of the Hi-Z condition and sends data bytes sequentially, beginning with data from register Addr0. The part ignores all other data on SDI until the end of the burst.

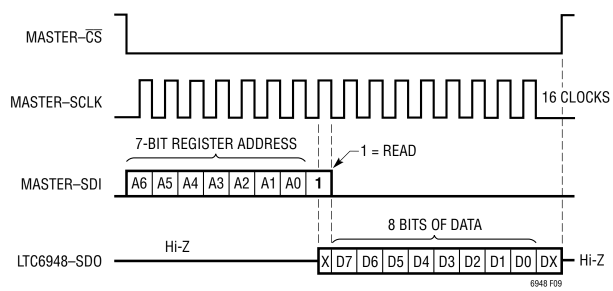



**Figure 9. Serial Port Read Sequence**

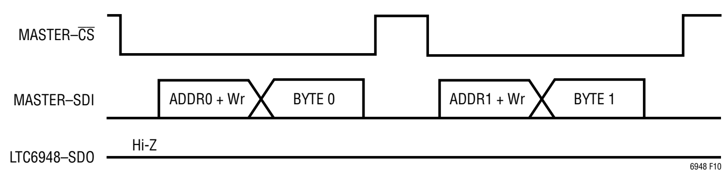



**Figure 10. Serial Port Single Byte Write**

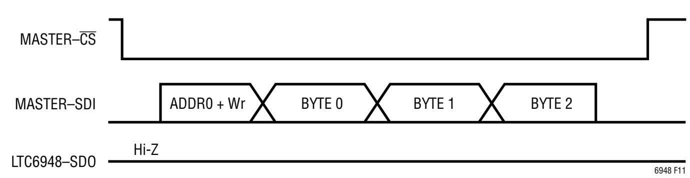



**Figure 11. Serial Port Auto-Increment Write**

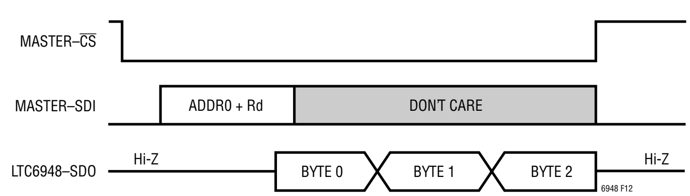



**Figure 12. Serial Port Auto-Increment Read**

# OPERATION

### Multidrop Configuration

Several LTC6948s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate $\overline{CS}$ for each LTC6948 and ensure that only one device has $\overline{CS}$ asserted at any time. It is recommended to attach a high value resistor to SDO to ensure the line returns to a known level during Hi-Z states.

### Serial Port Registers

The memory map of the LTC6948 may be found below in Table 15, with detailed bit descriptions found in Table 16. The register address shown in hexadecimal format under the ADDR column is used to specify each register. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset is shown at the right.

The read-only register at address h00 is used to determine different status flags. These flags may be instantly output on the STAT pin by configuring register h01. See STAT Output section that follows for more information.

The read-only register at address h0E is a ROM byte for device identification.

### STAT Output

The STAT output pin is configured with the x[5:0] bits of register h01. These bits are used to bit-wise mask, or enable, the corresponding status flags of status register h00, according to Equation 2. The result of this bit-wise Boolean operation is then output on the STAT pin.

STAT = OR (Reg00[5:0] AND Reg01[5:0]) (2)

or, expanded,

STAT = (UNLOCK AND x[5]) OR
(ALCHI AND x[4]) OR
(ALCLO AND x[3]) OR
(LOCK AND x[2]) OR
(THI AND x[1]) OR
(TLO AND x[0])

For example, if the application requires STAT to go high whenever the ALCHI, ALCLO, or THI flags are set, then x[4], x[3], and x[1] should be set to 1, giving a register value of h1A.

**Table 15. Serial Port Register Contents**

| ADDR | MSB | [6] | [5] | [4] | [3] | [2] | [1] | LSB | R/W | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|
| h00 | * | * | UNLOCK | ALCHI | ALCLO | LOCK | THI | TLO | R | |
| h01 | * | * | x[5] | x[4] | x[3] | x[2] | x[1] | x[0] | R/W | h04 |
| h02 | PDALL | PDPLL | PDVCO | PDOUT | PDFN | MTCAL | OMUTE | POR | R/W | h06 |
| h03 | ALCEN | ALCMON | ALCCAL | ALCULOK | AUTOCAL | AUTORST | DITHEN | INTN | R/W | h3E |
| h04 | BD[3] | BD[2] | BD[1] | BD[0] | CPLE | LDOEN | LDOV[1] | LDOV[0] | R/W | h47 |
| h05 | SEED[7] | SEED[6] | SEED[5] | SEED[4] | SEED[3] | SEED[2] | SEED[1] | SEED[0] | R/W | h11 |
| h06 | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | * | ND[9] | ND[8] | R/W | h08 |
| h07 | ND[7] | ND[6] | ND[5] | ND[4] | ND[3] | ND[2] | ND[1] | ND[0] | R/W | hFA |
| h08 | * | * | NUM[17] | NUM[16] | NUM[15] | NUM[14] | NUM[13] | NUM[12] | R/W | h3F |
| h09 | NUM[11] | NUM[10] | NUM[9] | NUM[8] | NUM[7] | NUM[6] | NUM[5] | NUM[4] | R/W | hFF |
| h0A | NUM[3] | NUM[2] | NUM[1] | NUM[0] | * | * | RSTFN | CAL | R/W | hF0 |
| h0B | BST | FILT[1] | FILT[0] | RFO[1] | RFO[0] | OD[2] | OD[1] | OD[0] | R/W | hF9 |
| h0C | LKWIN[2] | LKWIN[1] | LKWIN[0] | LKCT[1] | LKCT[0] | CP[2] | CP[1] | CP[0] | R/W | h4F |
| h0D | CPCHI | CPCLO | CPMID | CPINV | CPWIDE | CPRST | CPUP | CPDN | R/W | hE4 |
| h0E | REV[3] | REV[2] | REV[1] | REV[0] | PART[3] | PART[2] | PART[1] | PART[0] | R | hxx† |

*unused †varies depending on version

# OPERATION

## Block Power-Down Control

The LTC6948's power-down control bits are located in register h02, described in Table 16. Different portions of the device may be powered down independently. *Care must be taken with the LSB of the register, the POR (power-on-reset) bit. When written to a 1, this bit forces a full reset of the part's digital circuitry to its power-up default state.*

**Table 16. Serial Port Register Bit Field Summary**

| BITS | DESCRIPTION | DEFAULT |
|---|---|---|
| ALCCAL | Auto Enable ALC During CAL Operation | 1 |
| ALCEN | Always Enable ALC (Override) | 1 |
| ALCHI | ALC too Hi Flag | |
| ALCLO | ALC too Low Flag | |
| ALCMON | Enable ALC Monitor for Status Flags Only | 0 |
| ALCULOK | Enable ALC When PLL Unlocked | 1 |
| AUTOCAL | Calibrate VCOs Whenever Registers h06 to h0A Are Written | 1 |
| AUTORST | Reset Modulator Whenever Registers h05 to h0A Are Written | 1 |
| BD[3:0] | Calibration B Divider Value | h4 |
| BST | REF Buffer Boost Current | 1 |
| CAL | Start VCO Calibration (Auto Clears) | 0 |
| CP[2:0] | CP Output Current | h7 |
| CPCHI | Enable Hi-Voltage CP Output Clamp | 1 |
| CPCLO | Enable Low-Voltage CP Output Clamp | 1 |
| CPDN | Force CP Pump Down | 0 |
| CPINV | Invert CP Phase | 0 |
| CPLE | CP Linearizer Enable | 0 |
| CPMID | CP Bias to Mid-Rail | 1 |
| CPRST | CP Tri-State | 1 |
| CPUP | Force CP Pump Up | 0 |
| CPWIDE | Extend CP Pulse Width | 0 |
| DITHEN | Enable Fractional Numerator Dither | 1 |
| FILT[1:0] | REF Input Buffer Filter | h3 |
| INTN | Integer Mode; Fractional Modulator Placed in Standby | 0 |
| LDOEN | LDO Enable | 1 |
| LDOV[1:0] | LDO Voltage | h3 |
| LKCT[1:0] | PLL Lock Cycle Count | h1 |
| LKWIN[2:0] | PLL Lock Indicator Window | h2 |
| LOCK | PLL Lock Indicator Flag | |
| MTCAL | Mute RF Output During Calibration | 1 |
| ND[9:0] | N Divider Value (ND[9:0] ≥ 32) | h0FA |
| NUM[17:0] | Fractional Numerator Value | h3FFF |
| OD[2:0] | Output Divider Value (0 < OD[2:0] < 7) | h1 |
| OMUTE | Mutes RF Output | 1 |
| PART[3:0] | Part Code (h01 for -1, h02 for -2, h03 for -3, h04 for -4 version) | h01, h02, h03, h04 |
| PDALL | Full Chip Powerdown | 0 |
| PDFN | Powers Down LDO and Modulator Clock | 0 |
| PDOUT | Powers Down O_DIV, RF Output Buffer | 0 |
| PDPLL | Powers Down REF, R_DIV, PFD, CPUMP, N_DIV | 0 |
| PDVCO | Powers Down VCO, N_DIV | 0 |
| POR | Force Power-On-Reset | 0 |
| RD[4:0] | R Divider Value (RD[4:0] > 0) | h001 |
| REV[3:0] | Rev Code | h1 |
| RFO[1:0] | RF Output Power | h3 |
| RSTFN | Force Modulator Reset (Auto Clears) | 0 |
| SEED[7:0] | Modulator Dither Seed Value | h11 |
| THI | CP Clamp High Flag | |
| TLO | CP Clamp Low Flag | |
| UNLOK | PLL Unlock Flag | |
| x[5:0] | STAT Output OR Mask | h04 |

# APPLICATIONS INFORMATION

## INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the frequency input at REF± and outputs a higher frequency at RF±. The PFD, charge pump, N divider, VCO and external loop filter form a feedback loop to accurately control the output frequency (see Figure 13).

The external loop filter is used to set the PLL's loop bandwidth BW. Lower bandwidths generally have better spurious performance and lower ΔΣ modulator quantization noise. Higher bandwidths can have better total integrated phase noise.

The R and O divider and input frequency $f_{REF}$ are used to set the output frequency resolution. When in fractional mode, the ΔΣ modulator changes the N divider's ratio each PFD cycle to produce an average fractional divide ratio. This achieves a much smaller frequency resolution for a given $f_{PFD}$ as compared to integer mode.

## OUTPUT FREQUENCY

When the loop is locked, the frequency $f_{VCO}$ (in Hz) produced at the output of the VCO is determined by the reference frequency $f_{REF}$, the R and N divider values, and the fractional value F, given by Equation 3:

$$f_{VCO} = \frac{f_{REF} \bullet (N + F)}{R} \quad (3)$$

where the fractional value F is given by Equation 4:

$$F = \frac{NUM}{2^{18}} \quad (4)$$

NUM is programmable from 1 to 262143, or $2^{18} – 1$. When using the LTC6948 in integer mode, F = 0.

The PFD frequency $f_{PFD}$ is given by the following equation:

$$f_{PFD} = \frac{f_{REF}}{R} \quad (5)$$

and $f_{VCO}$ may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet (N + F) \quad (6)$$

The output frequency $f_{RF}$ produced at the output of the O divider is given by Equation 7:

$$f_{RF} = \frac{f_{VCO}}{O} \quad (7)$$

Using the above equations, the minimum output frequency resolution $f_{STEP(MIN)}$ produced by a unit change in the fractional numerator NUM while in fractional mode is given by Equation 8:

$$f_{STEP(MIN)} = \frac{f_{REF}}{R \bullet O \bullet 2^{18}} \quad (8)$$

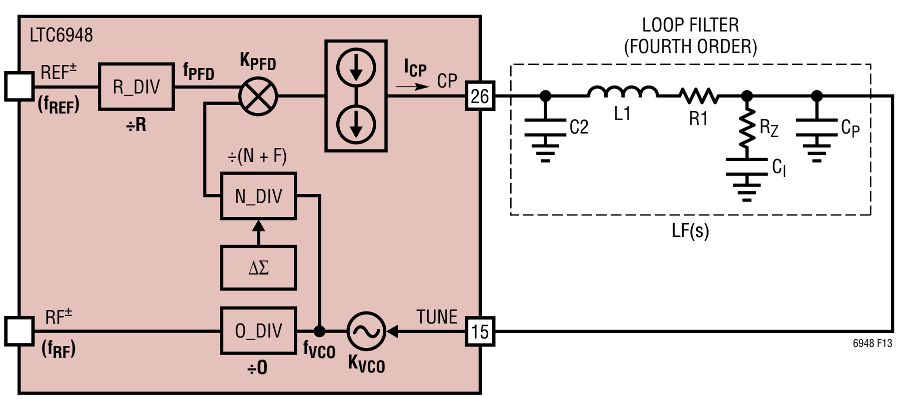



Figure 13. PLL Loop Diagram

## APPLICATIONS INFORMATION

Alternatively, to calculate the numerator step size $NUM_{STEP}$ needed to produce a given frequency step $f_{STEP(FRAC)}$, use Equation 9:

$$NUM_{STEP} = \frac{f_{STEP(FRAC)} \bullet R \bullet O \bullet 2^{18}}{f_{REF}} \quad (9)$$

The output frequency resolution $f_{STEP(INT)}$ produced by a unit change in N while in integer mode is given by Equation 10:

$$f_{STEP(INT)} = \frac{f_{REF}}{R \bullet O} \quad (10)$$

### LOOP FILTER DESIGN

A stable PLL system requires care in designing the external loop filter. The Linear Technology FracNWizard application, available from www.linear.com, aids in design and simulation of the complete system.

The loop design should use the following algorithm:

1) *Determine the output frequency $f_{RF}$ and frequency step size $f_{STEP}$ based on application requirements.* Using Equations 3, 5, 7, and 8, change $f_{REF}$, N, R, and O until the application frequency constraints are met. Use the minimum R value that still satisfies the constraints. Then calculate B using Equation 1 and Tables 8 and 9.

2) *Select the open loop bandwidth BW constrained by $f_{PFD}$ and oversampling ratio OSR.* The OSR is the ratio of $f_{PFD}$ to BW (see Equation 11):

$$OSR = \frac{f_{PFD}}{BW} \quad (11)$$

or

$$BW = \frac{f_{PFD}}{OSR}$$

where BW and $f_{PFD}$ are in Hz.

A stable loop, both in integer and fractional mode, requires that the OSR is greater than or equal to 10. Further, in fractional mode, OSR must be high enough to allow the loop filter to reduce modulator quantization noise to an acceptable level.

Choosing a higher order loop filter when using the ΔΣ modulator allows for a smaller OSR, and thus a larger loop bandwidth. Linear Technology's FracNWizard helps choose the appropriate OSR and BW values.

3) *Select loop filter component $R_Z$ and charge pump current $I_{CP}$ based on BW and the VCO gain factor, $K_{VCO}$.* BW (in Hz) is approximated by the following equation:

$$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N} \quad (12)$$

or

$$R_Z = \frac{2 \bullet \pi \bullet BW \bullet N}{I_{CP} \bullet K_{VCO}}$$

where $K_{VCO}$ is in Hz/V, $I_{CP}$ is in Amps, and $R_Z$ is in Ohms. $K_{VCO}$ is obtained from the VCO Tuning Sensitivity in the Electrical Characteristics. Use $I_{CP}$ = 5.6mA to lower in-band noise unless component values force a lower setting.

4) *Select loop filter components $C_I$ and $C_P$ based on BW and $R_Z$.* A reliable second-order loop filter design can be achieved by using the following equations for the loop capacitors (in Farads).

$$C_I = \frac{3.5}{2 \bullet \pi \bullet BW \bullet R_Z} \quad (13)$$

$$C_P = \frac{1}{7 \bullet \pi \bullet BW \bullet R_Z} \quad (14)$$

Use FracNWizard to aid in the design of higher order loop filters.

# APPLICATIONS INFORMATION

## DESIGN AND PROGRAMMING EXAMPLE

This programming example uses the DC1959 with the LTC6948-2. Assume the following parameters of interest:

$f_{REF}$ = 100MHz at 7dBm into 50Ω

$f_{STEP}$ = 50kHz

$f_{RF}$ = 1921.650MHz

From the Electrical Characteristics table:

$f_{VCO}$ = 3.080GHz to 4.910GHz

$K_{VCO\%}$ = 4.7%Hz/V to 7%Hz/V

### Determining Divider Values

Following the loop filter design algorithm, first determine all the divider values. The maximum $f_{PFD}$ while in fractional mode is less than 100MHz, so R must be greater than 1.

R = 2

Then, using Equations 5 and 7, calculate the following values:

O = 2

$f_{PFD}$ = 50MHz

Then using Equation 6:

$$N+F=\frac{2\bullet 1921.650\text{MHz}}{50\text{MHz}}=76.866$$

Therefore:

N = 76

F = 0.866

Then, from Equation 4,

NUM = 0.866 • $2^{18}$ = 227017

Also, from Equation 1 and Tables 8 and 9 determine B:

B = 48 and BD[3:0] = h5

A calibration cycle takes 12 to 14 clock cycles of $f_{CAL}$. This gives a VCO calibration time of approximately:

$$t_{CAL}\cong\frac{14}{f_{CAL}}=14\bullet\frac{B}{f_{PFD}}=13.4\mu s$$

### Selecting Filter Type and Loop Bandwidth

The next step in the algorithm is choosing the open loop bandwidth. Select the minimum bandwidth resulting from the below constraints.

1) The OSR must be at least 10 (sets absolute maximum BW).
2) The integrated phase noise due to thermal noise should be minimized, neglecting any modulator noise.
3) The loop bandwidth must be narrow enough to adequately filter the modulator's quantization noise.

FracNWizard reports the loop bandwidths resulting from each of the above constraints. The quantization noise constrained results vary according to the shape of the external loop filter. FracNWizard reports an optimal bandwidth for several filter types.

FracNWizard reports the thermal noise optimized loop bandwidth is 211kHz. Filter 3 (fourth order response) has a quantization noise constrained BW of 150kHz, making it a good choice. Select Filter 3 and use the smaller of the two bandwidths (150kHz) for optimal integrated phase noise. Use Equation 11 to calculate OSR:

$$OSR=\frac{50\text{MHz}}{150\text{kHz}}=333.3$$

## APPLICATIONS INFORMATION

### Loop Filter Component Selection

Now set loop filter resistor $R_Z$ and charge pump current $I_{CP}$. Because the $K_{VCO}$ varies over the VCO's frequency range, using the $K_{VCO}$ geometric mean gives good results:

$$K_{VCO} = 3.843 \bullet 10^9 \bullet \sqrt{0.047 \bullet 0.07}$$
$$= 220.4\text{MHz/V}$$

Using an $I_{CP}$ of 5.6mA, the FracNWizard uses Equation 12 to determine $R_Z$:

$$R_Z = \frac{2 \bullet \pi \bullet 150k \bullet 76}{5.6m \bullet 220.4M}$$
$$R_Z = 58.0\Omega$$

For the 4th order Filter 3, FracNWizard uses modified Equations 13 and 14 to calculate $C_I$, $C_P$:

$$C_I = \frac{4.5}{2 \bullet \pi \bullet 150k \bullet 58} = 82.3\text{nF}$$
$$C_P = \frac{1}{10.5 \bullet \pi \bullet 150k \bullet 58} = 3.5\text{nF}$$

FracNWizard calculates R1, L1, and C2 to be:

R1 = 58.0Ω

C2 = 2.3nF

L1 = 7.8µH

### Status Output Programming

This example will use the STAT pin to alert the system whenever the LTC6948 generates a fault condition. Program x[5], x[4], x[3], x[1], x[0] = 1 to force the STAT pin high whenever any of the UNLOCK, ALCHI, ALCLO, THI, or TLO flags asserts:

Reg01 = h3B

### Power Register Programming

For correct PLL operation all internal blocks should be enabled. OMUTE may remain asserted (or the $\overline{\text{MUTE}}$ pin held low) until programming is complete. For OMUTE = 1:

Reg02 = h02

### VCO ALC, AUTOCAL, and AUTORST Programming

Set the ALC options (ALCMON = ALCULOK = ALCCAL = 1), the auto reset options (AUTOCAL = AUTORST = 1), and the ΔΣ modulator modes (DITHEN = 1, INTN = 0) at the same time:

Reg03 = h7E

The ALC will only be active during a calibration cycle or when the loop is unlocked, but the ALCHI and ALCLO status conditions will be monitored continuously. The VCO will be calibrated and the ΔΣ modulator will be reset at the end of the SPI write communication burst (assuming an auto-increment write is used to write all registers).

### LDO Programming

Use Table 13 and $f_{PFD}$ = 50MHz to determine V(LDO) and LDOV[1:0]:

V(LDO) = 2.3V and LDOV[1:0] = 2

Use LDOV[1:0], LDOEN = 1 to enable the LDO, and the previously determined BD[3:0] value to set Reg04. CPLE should be set to 1 to reduce in-band noise and spurious due to the ΔΣ modulator:

Reg04 = h5E

### SEED Programming

The SEED[7:0] value is used to initialize the ΔΣ modulator dither circuitry. Use the default value:

Reg05 = h11

## APPLICATIONS INFORMATION

### R and N Divider and Numerator Programming

Program registers Reg06 to Reg0A with the previously determined R and N divider and numerator values. Because the AUTORST and AUTOCAL bits were previously set to 1, CAL and RSTFN do not need to be set:

Reg06 = h10

Reg07 = h4C

Reg08 = h37

Reg09 = h6C

Reg0A = h90

### Reference Input Settings and Output Divider Programming

From Table 1, FILT = 0 for a 100MHz reference frequency. Next, convert 7dBm into $V_{P-P}$. For a CW tone, use the following equation with R = 50:

$$V_{P\text{-}P} \cong \sqrt{R} \bullet 10^{(dBm-21)/20} \quad (15)$$

This gives $V_{P\text{-}P}$ = 1.41V, and, according to Table 2, set BST = 1.

Now program Reg0B, assuming maximum $RF^{\pm}$ output power (RFO[1:0] = 3 according to Table 14) and OD[2:0] = 2:

Reg0B = h9A

### Lock Detect and Charge Pump Current Programming

Next, determine the lock indicator window from $f_{PFD}$. From Table 3 we see that LKWIN[1:0] = 0 with a $t_{LWW}$ of 5ns for CPLE = 1 and $f_{VCO}$ = 3.843GHz. The LTC6948 will consider the loop locked as long as the phase coincidence at the PFD is within 90°, as calculated below.

$$\text{phase} = 360° \bullet t_{LWW} \bullet f_{PFD} = 360 \bullet 5n \bullet 50M = 90°$$

Choosing the correct COUNTS value depends upon the OSR. Smaller ratios dictate larger COUNTS values, although application requirements will vary. A COUNTS value of 32 will work for the OSR of 333. From Table 5, LKCT[1:0] = 1 for 32 counts.

Using Table 6 with the previously selected $I_{CP}$ of 5.6mA gives CP[3:0] = 7. This gives enough information to program Reg0C:

Reg0C = h0D

### Charge Pump Function Programming

This example uses the additional voltage clamp features to allow the monitoring of fault conditions by setting CPCHI = 1 and CPCLO = 1. If something occurs and the system can no longer lock to its intended frequency, the charge pump output will move toward either GND or $V_{CP}^{+}$, thereby setting either the TLO or THI status flags, respectively. Disable all the other charge pump functions (CPMID, CPINV, CPRST, CPUP, and CPDN), allowing the loop to lock:

Reg0D = hC0

The loop should now lock. Now un-mute the output by setting OMUTE = 0 (assumes the $\overline{\text{MUTE}}$ pin is high).

Reg02 = h04

## APPLICATIONS INFORMATION

### REFERENCE SOURCE CONSIDERATIONS

A high quality signal must be applied to the $REF^{\pm}$ inputs as they provide the frequency reference to the entire PLL. As mentioned previously, to achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

The LTC6948 may be driven single-ended to CMOS levels (greater than $2.7V_{P-P}$ ). Apply the reference signal at $REF^{+}$, and bypass $REF^{-}$ to GND with a 47pF capacitor. The BST bit must also be set to 0, according to guidelines given in Table 2.

The LTC6948 achieves an integer mode in-band normalized phase noise floor $L_{NORM(INT)}$ = –226dBc/Hz typical, and a fractional mode phase noise floor $L_{NORM(FRAC)}$ = –225 dBc/Hz typical. To calculate its equivalent input phase noise floor $L_{IN}$, use the following Equation 16.

$$L_{IN} = L_{NORM} + 10 \bullet \log_{10}(f_{REF}) \quad (16)$$

For example, using a 10MHz reference frequency in integer mode gives an input phase noise floor of –156dBc/Hz. The reference frequency source's phase noise must be at least 3dB better than this to prevent limiting the overall system performance.

### IN-BAND OUTPUT PHASE NOISE

The in-band phase noise floor $L_{OUT}$ produced at $f_{RF}$ may be calculated by using Equation 17.

$$L_{OUT} = L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}(f_{RF}/f_{PFD}) \quad (17)$$

or

$$L_{OUT} \approx L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}(N/O)$$

where $L_{NORM}$ is –226dBc/Hz for integer mode and –225dBc/Hz for fractional mode. See the Typical Performance Characteristics section for graphs showing $L_{NORM}$ variation versus $I_{CP}$ and $f_{VCO}$.

As can be seen from Equation 17 for a given PFD frequency $f_{PFD}$, the output in-band phase noise increases at a 20dB-per-decade rate with the N divider count. So, for a given output frequency $f_{RF}$, $f_{PFD}$ should be as large as possible (or N should be as small as possible) while still satisfying the application's frequency step size requirements.

### OUTPUT PHASE NOISE DUE TO 1/f NOISE

In-band phase noise at very low offset frequencies may be influenced by the LTC6948's 1/f noise, depending upon $f_{PFD}$. Use the normalized in-band 1/f noise $L_{1/f}$ of –274dBc/Hz with Equation 18 to approximate the output 1/f phase noise at a given frequency offset $f_{OFFSET}$.

$$L_{OUT(1/f)}(f_{OFFSET}) = L_{1/f} + 20 \bullet \log_{10}(f_{RF}) - 10 \bullet \log_{10}(f_{OFFSET}) \quad (18)$$

Unlike the in-band noise floor $L_{OUT}$, the 1/f noise $L_{OUT(1/f)}$ does not change with $f_{PFD}$, and is not constant over offset frequency. See Figure 14 for an example of integer mode in-band phase noise for $f_{PFD}$ equal to 3MHz and 100MHz. The total phase noise will be the summation of $L_{OUT}$ and $L_{OUT(1/f)}$.

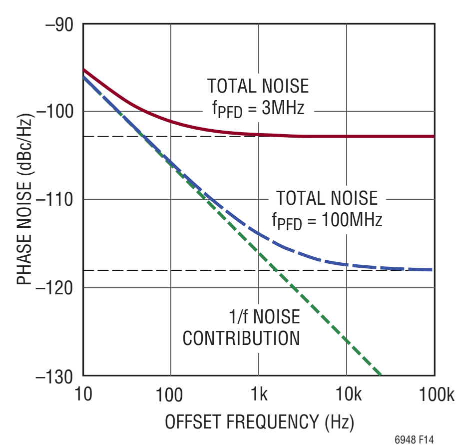



**Figure 14. Theoretical Integer Mode In-Band Phase Noise, $f_{RF}$ = 2500MHz**

## APPLICATIONS INFORMATION

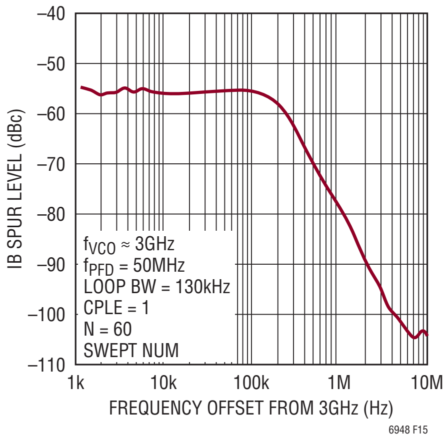



**Figure 15. Integer Boundary Spur Power vs Frequency Offset from Boundary, LTC6948-1**

### INTEGER BOUNDARY SPURS

Integer boundary spurs are caused by intermodulation between harmonics of the PFD frequency $f_{PFD}$ and the VCO frequency $f_{VCO}$. The coupling between the frequency source harmonics can occur either on- or off-chip. The spurs are located at offset frequencies defined by the beat frequency between the reference harmonics and the VCO frequency, and are attenuated by the loop filter. The spurs only occur while in fractional mode.

Integer boundary spurs are most commonly seen when the fractional value F approaches either zero or one such that the VCO frequency offset from an integer frequency is within the loop bandwidth:

$$f_{PFD} \bullet F \le BW$$

or

$$f_{PFD} \bullet (1 - F) \le BW$$

The spur will have a relatively constant power in-band, and be attenuated by the loop out-of-band. An example integer boundary spur measurement is shown in Figure 15.

### RF OUTPUT MATCHING

The $RF^{\pm}$ outputs may be used in either single-ended or differential configurations. Using both RF outputs differentially will result in approximately 3dB more output power than single-ended. Impedance matching to an external load in both cases requires external chokes tied to $V_{RF}^{+}$. Measured $RF^{\pm}$ S-parameters are shown below in Table 17 to aid in the design of impedance matching networks.

**Table 17. Single-Ended RF Output Impedance**

| FREQUENCY (MHz) | IMPEDANCE (Ω) | S11 (dB) |
|---|---|---|
| 100 | 133.0 – j16.8 | –6.7 |
| 500 | 110.8 – j46.1 | –6.8 |
| 1000 | 74.9 – j57.0 | –6.9 |
| 1500 | 49.0 – j51.3 | –6.7 |
| 2000 | 34.4 – j41.4 | –6.5 |
| 2500 | 27.0 – j32.1 | –6.5 |
| 3000 | 23.2 – j24.1 | –6.6 |
| 3500 | 21.6 – j15.9 | –7.1 |
| 4000 | 20.9 – j7.7 | –7.5 |
| 4500 | 20.1 – j0.2 | –7.4 |
| 5000 | 18.1 + j7.4 | –6.4 |
| 5500 | 16.7 + j12.5 | –5.6 |
| 6000 | 17.1 + j16.1 | –5.5 |
| 6500 | 20.2 + j20.1 | –6.2 |
| 7000 | 26.9 + j24.6 | –7.6 |
| 7500 | 38.8 + j32.3 | –8.8 |
| 8000 | 52.9 + j43.1 | –8.2 |

## APPLICATIONS INFORMATION

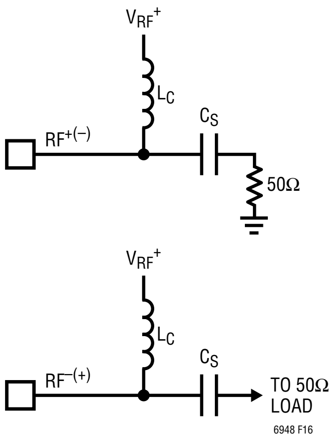



Figure 16. Single-Ended Output Matching Schematic

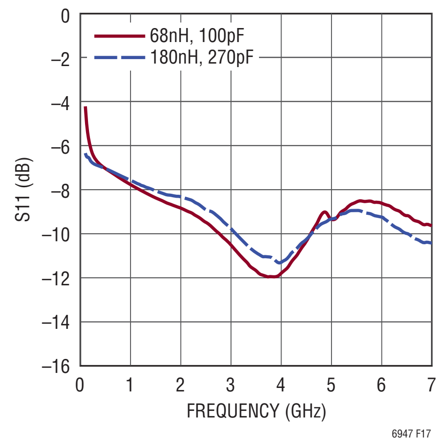



Figure 17. RF Single-Ended Return Loss

Single-ended impedance matching is accomplished using the circuit of Figure 16, with component values found in Table 18. *Using smaller inductances than recommended can cause phase noise degradation, especially at lower center frequencies.*

**Table 18. Suggested Single-Ended Matching Component Values**

| $f_{RF}$ (MHz) | $L_C$ (nH) | $C_S$ (pF) |
|---|---|---|
| 350 to 1500 | 180 | 270 |
| 1000 to 5800 | 68 | 100 |

Return loss measured on the DC1959 using the above component values is shown in Figure 17. A broadband match is achieved using an {$L_C$, $C_S$} of either {68nH, 100pF} or {180nH, 270pF}. However, for maximum output power and best phase noise performance, use the recommended component values of Table 18. $L_C$ should be a wirewound inductor selected for maximum Q factor and SRF, such as the Coilcraft HP series of chip inductors.

The LTC6948's differential $RF^{\pm}$ outputs may be combined using an external balun to drive a single-ended load. The advantages are approximately 3dB more output power than each output individually and better 2nd order harmonic performance.

For lower frequencies, transmission line (TL) baluns such as the M/A-COM MABACT0065 and the TOKO #617DB-1673 provide good results. At higher frequencies, surface mount (SMT) baluns such as those produced by TDK, Anaren, and Johanson Technology, can be attractive alternatives. See Table 19 for recommended balun part numbers versus frequency range.

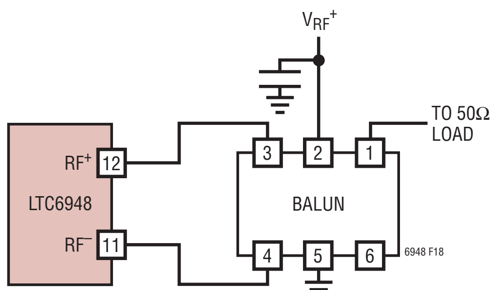
The listed SMT baluns contain internal chokes to bias $RF^{\pm}$ and also provide input-to-output DC isolation. The pin denoted as GND or DC FEED should be connected to the $V_{RF}^{+}$ voltage. Figure 18 shows a surface mount balun's connections with a DC FEED pin.

**Table 19. Suggested Baluns**

| $f_{RF}$ (MHz) | PART NUMBER | MANUFACTURER | TYPE |
|---|---|---|---|
| 350 to 900 | #617DB-1673 | TOKO | TL |
| 400 to 600 | HHM1589B1 | TDK | SMT |
| 600 to 1400 | BD0810J50200 | Anaren | SMT |
| 600 to 3000 | MABACT0065 | M/A-COM | TL |
| 1000 to 2000 | HHM1518A3 | TDK | SMT |
| 1400 to 2000 | HHM1541E1 | TDK | SMT |
| 1900 to 2300 | 2450BL15B100E | Johanson | SMT |
| 2000 to 2700 | HHM1526 | TDK | SMT |
| 3700 to 5100 | HHM1583B1 | TDK | SMT |
| 4000 to 6000 | HHM1570B1 | TDK | SMT |

The listed TL baluns do not provide input-to-output DC isolation and must be AC-coupled at the output. Figure 19 displays $RF^{\pm}$ connections using these baluns.

# APPLICATIONS INFORMATION




**BALUN PIN CONFIGURATION**

| | |
|---|---|
| 1 | UNBALANCED PORT |
| 2 | GND OR DC FEED |
| 3 | BALANCED PORT |
| 4 | BALANCED PORT |
| 5 | GND |
| 6 | NC |

**Figure 18. Example SMT Balun Connection**

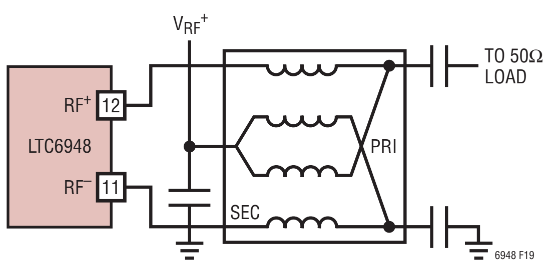



**Figure 19. Example TL Balun Connection**

## SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

Care must be taken when creating a PCB layout to minimize power supply decoupling and ground inductances. All power supply $V^+$ pins should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible. Multiple vias to the ground plane should be used for all ground connections, including to the power supply decoupling capacitors.

The package's exposed pad is a ground connection, and must be soldered directly to the PCB land pattern. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance (see Figure 20 for an example). See QFN Package Users Guide, page 8, on Linear Technology website's Packaging Information page for specific recommendations concerning land patterns and land via solder masks. A link is provided below.

http://www.linear.com/designtools/packaging

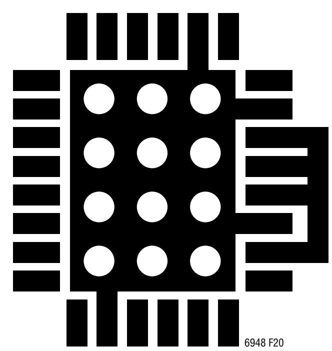



**Figure 20. Example Exposed Pad Land Pattern**

# APPLICATIONS INFORMATION

## REFERENCE SIGNAL ROUTING, SPURIOUS, AND PHASE NOISE

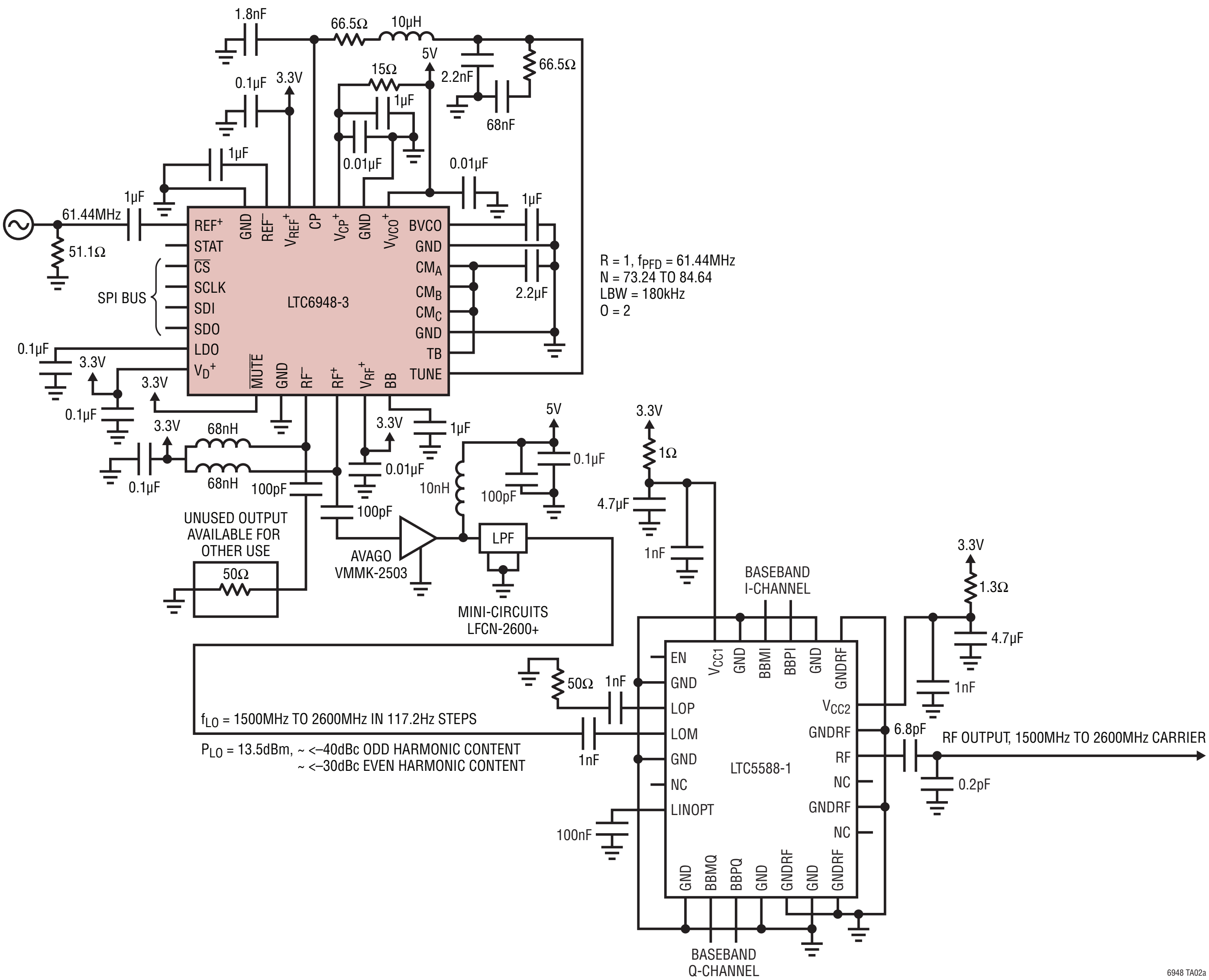
The charge pump operates at the PFD's comparison frequency $f_{PFD}$. The resultant output spurious energy is small and is further reduced by the loop filter before it modulates the VCO frequency.

However, improper PCB layout can degrade the LTC6948's inherent spurious performance. Care must be taken to prevent the reference signal $f_{REF}$ from coupling onto the VCO's tune line, or into other loop filter signals. Example suggestions are the following.

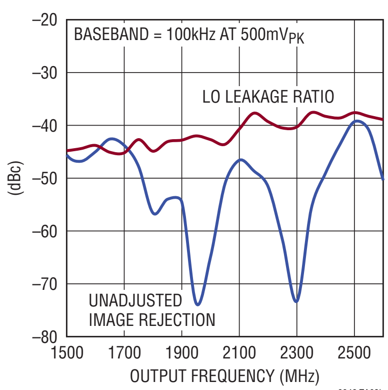
1) Do not share power supply decoupling capacitors between same-voltage power supply pins.
2) Use separate ground vias for each power supply decoupling capacitor, especially those connected to $V_{REF}^+$, $V_D^+$, LDO, $V_{CP}^+$, and $V_{VCO}^+$.
3) Physically separate the reference frequency signal from the loop filter and VCO.
4) *Do not place a trace between the $CM_A$, $CM_B$, and $CM_C$ pads underneath the package, as worse phase noise could result.*

# TYPICAL APPLICATIONS

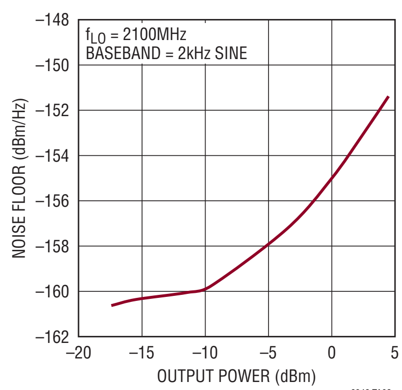
**Driving a Modulator LO for High Image Rejection and Low Noise Floor**




**Measured Image Rejection and LO Leakage Ratio vs Output Frequency**



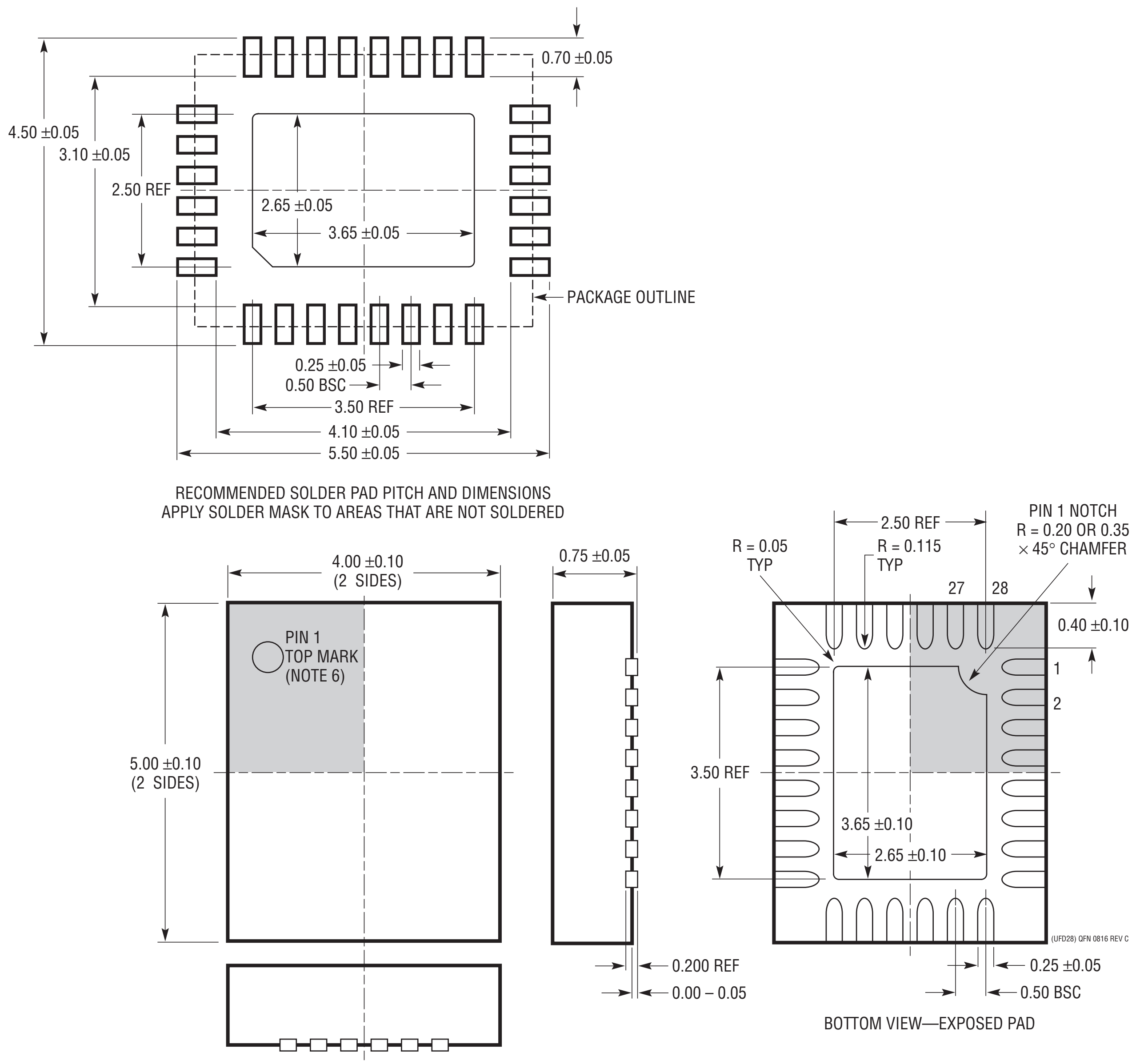

**Measured Noise Floor at 70MHz Offset vs RF Output Power**



# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC6948#packaging for the most recent package drawings.**

**UFD Package**
**28-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1712 Rev C)



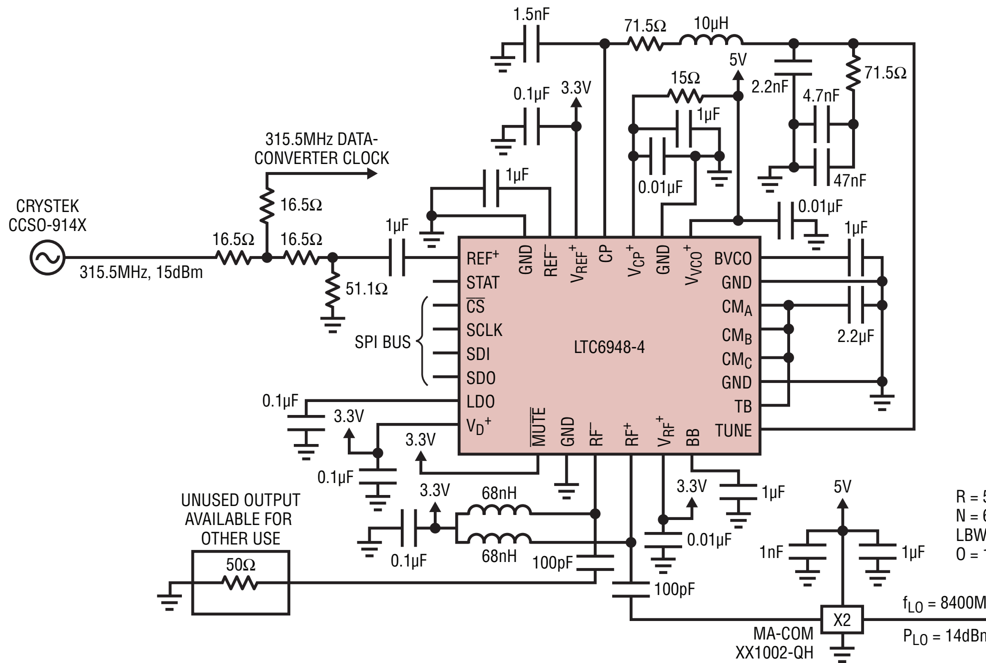

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# REVISION HISTORY

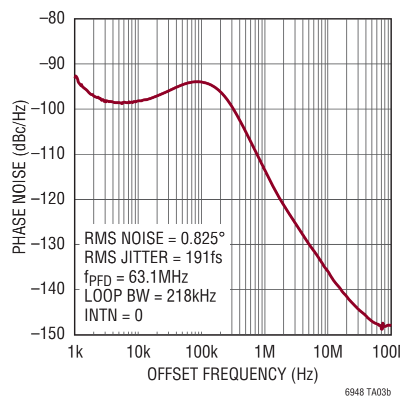
| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 04/17 | Corrected defaults for ALCULOK and BD[3:0]. | 24 |

# TYPICAL APPLICATIONS

Generating a 12GHz LO Signal




System Phase Noise
$f_{RF}$ = 12.024GHz




# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC6946-x | Ultralow Noise and Spurious Integer-N Synthesizer with Integrated VCO | 370MHz to 6.4GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor |
| LTC6945 | Ultralow Noise and Spurious Integer-N Synthesizer | 350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor |
| LTC6947 | Ultralow Noise and Spurious Fractional-N Synthesizer | 350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor |
| LTC6957 | Low Phase Noise, Dual Output Buffer/Driver/ Logic Converter | Optimized Conversion of Sine Waves to Logic Levels, LVPECL/LVDS/CMOS Outputs, DC-300MHz, 45fsRMS additive jitter (LVPECL) |
| LTC5540/LTC5541/ LTC5542/LTC5543 | High Dynamic Range Downconverting Mixers | 8dB Conversion Gain, 26.4dBm IIP3, 9.6dB NF, 600MHz to 4GHz |
| LTC5590/LTC5591/ LTC5592/LTC5593 | High Linearity Dual Mixers | 600MHz to 4.5GHz, 8.5dB Gain, 26.2dBm IIP3, 9.9dB NF |
| LTC5569 | Broadband Dual Mixer | 300MHz to 4GHz, 26.8dBm IIP3, 2dB Gain, 11.7dB NF, 600mW Power |
| LTC5588-1 | Ultrahigh OIP3 I/Q Modulator | 200MHz to 6GHz, 31dBm OIP3, –160.6dBm/Hz Noise Floor |
| LT®5575 | Direct Conversion I/Q Demodulator | 800MHz to 2.7GHz, 22.6dBm IIP3, 60dBm IIP2, 12.7dB NF |





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