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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ528(L), 2SJ528(S)

Silicon P Channel MOS FET

REJ03G0878-0300
(Previous: ADE-208-641A)
Rev.3.00
Sep 07, 2005

Description

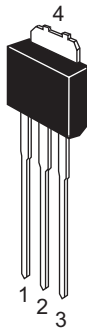
High speed power switching

Features

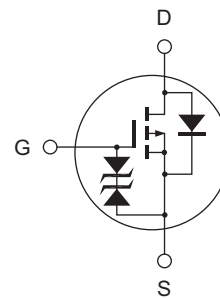
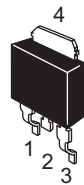
- Low on-resistance
 $R_{DS(on)} = 0.17 \Omega$ typ.
- 4 V gate drive devices
- High speed switching

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-7	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-28	A
Body to drain diode reverse drain current	I_{DR}	-7	A
Avalanche current	I_{AP} ^{Note 3}	-7	A
Avalanche energy	E_{AR} ^{Note 3}	4.2	mJ
Channel dissipation	P_{ch} ^{Note 2}	20	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

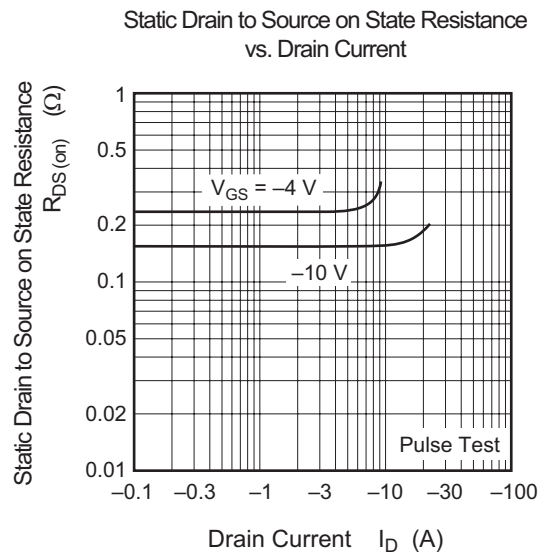
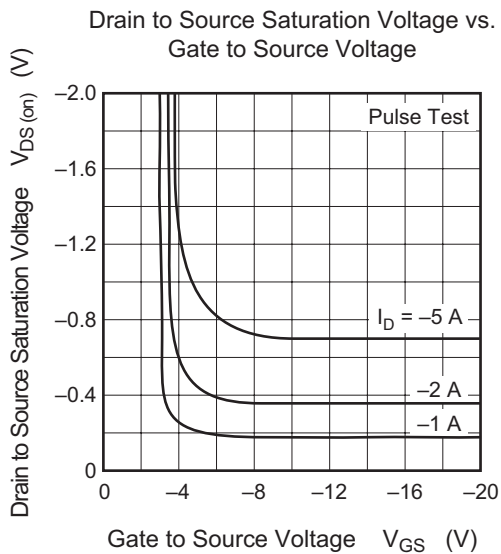
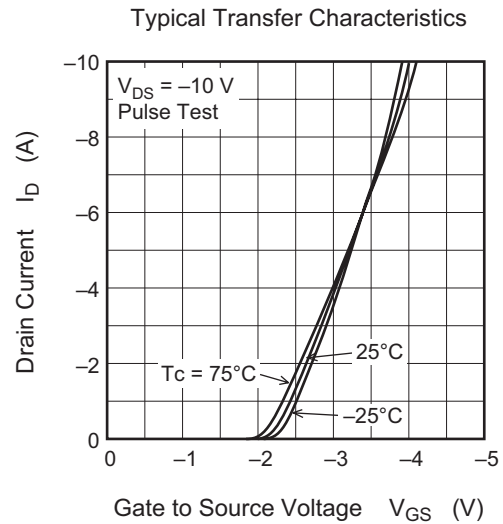
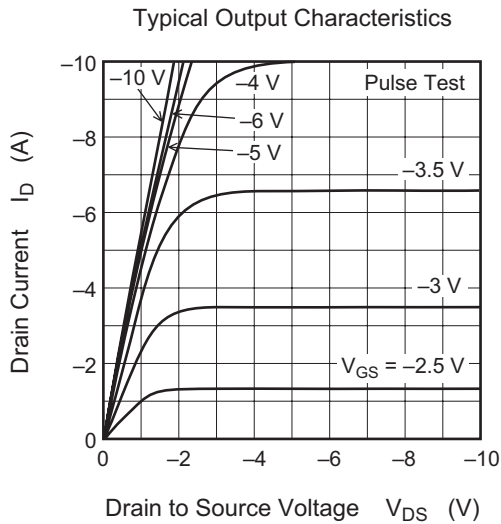
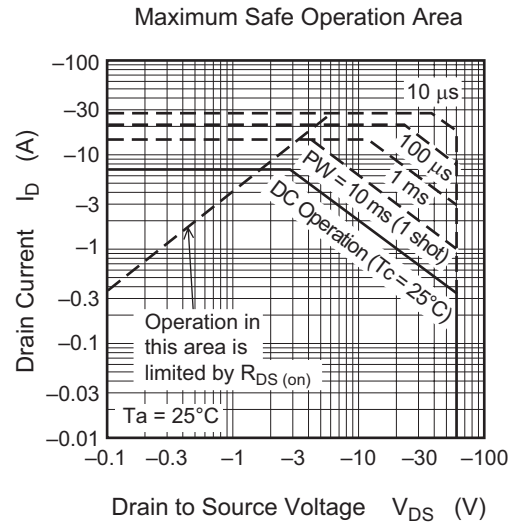
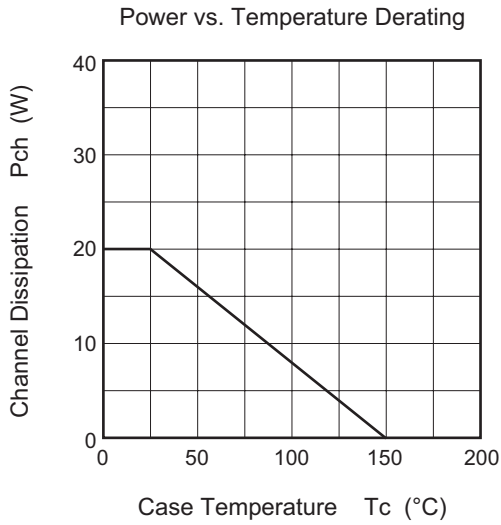
Electrical Characteristics

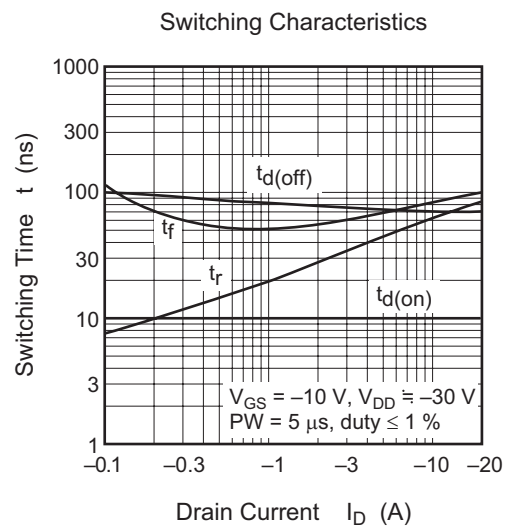
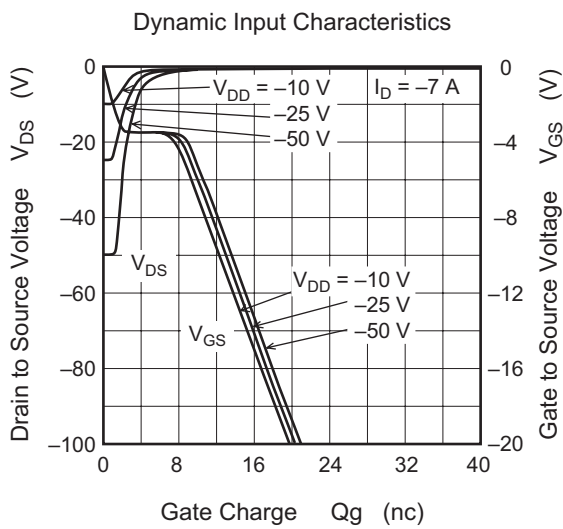
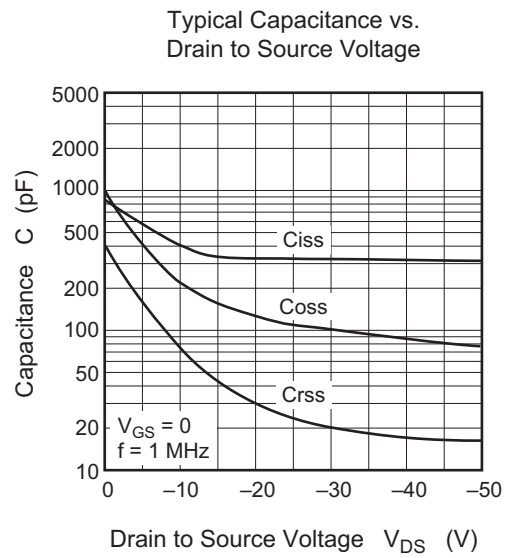
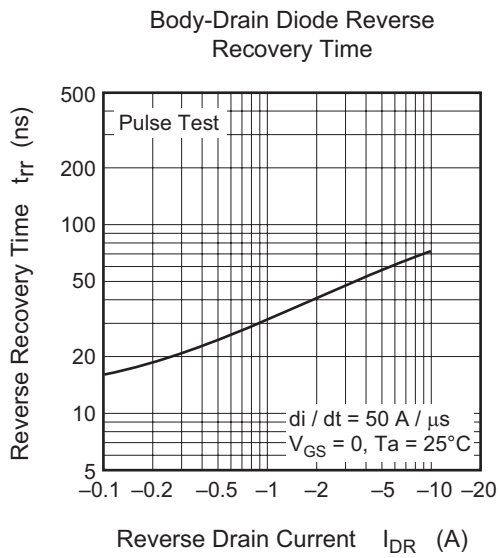
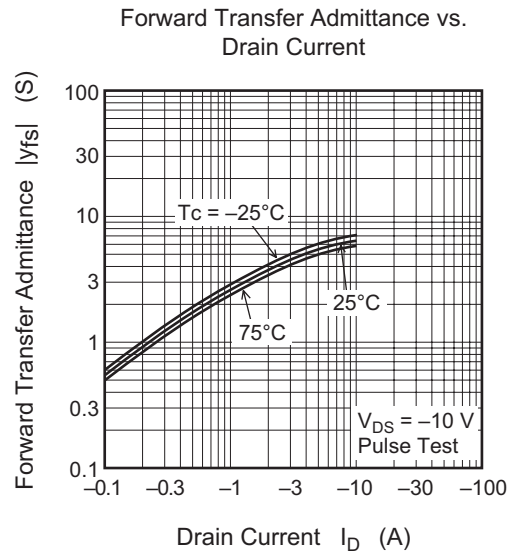
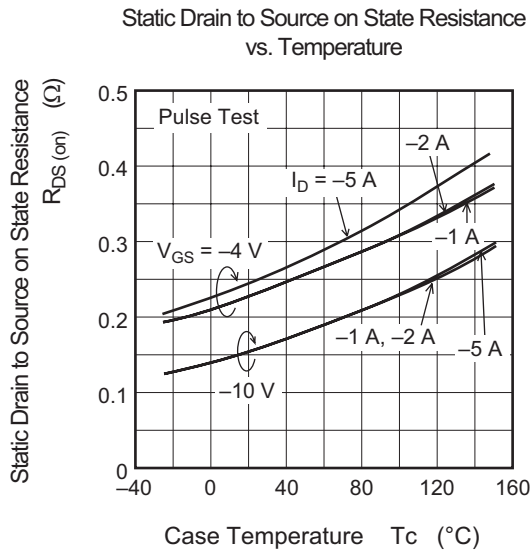
(Ta = 25°C)

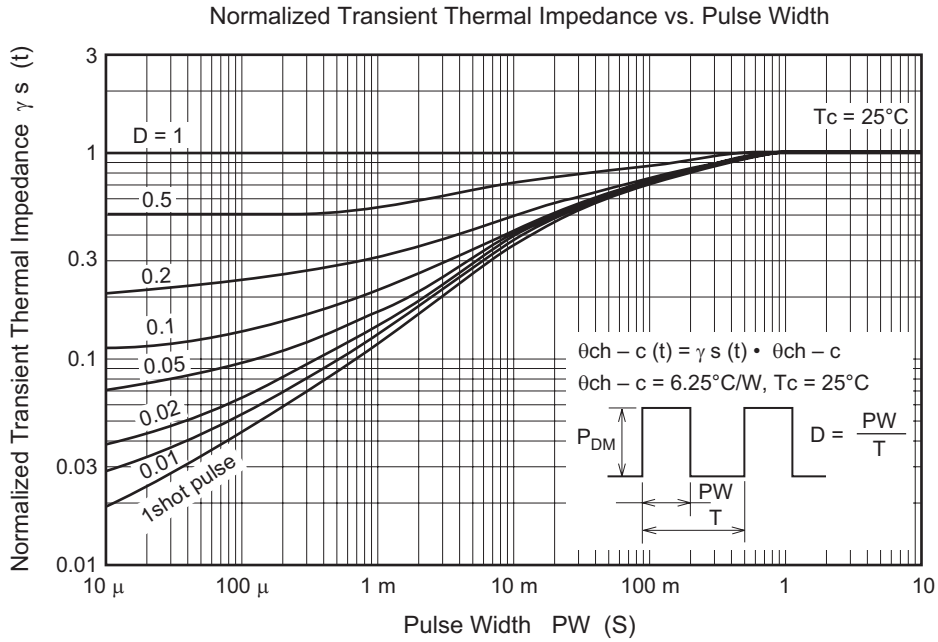
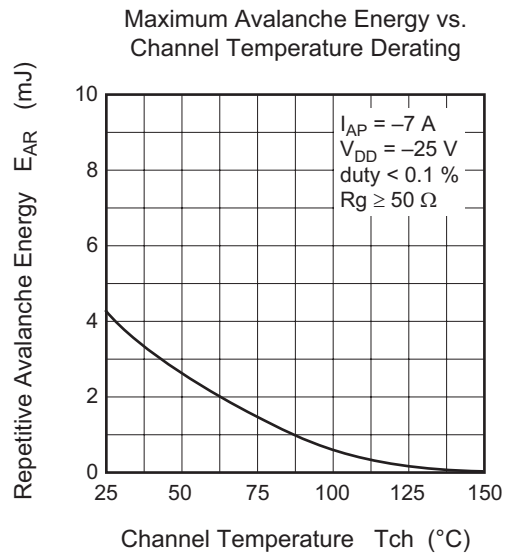
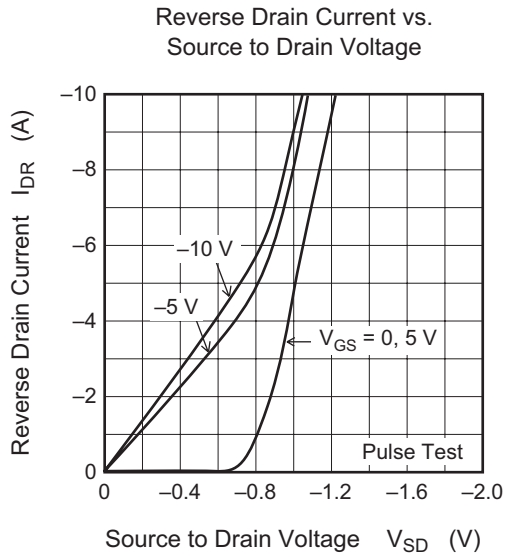
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.17	0.22	Ω	$I_D = -4 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note 4}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.24	0.37	Ω	$I_D = -4 \text{ A}$, $V_{GS} = -4 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	3.0	5.0	—	S	$I_D = -4 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	400	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	220	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	75	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10 \text{ V}$
Rise time	t_r	—	40	—	ns	$I_D = -4 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	75	—	ns	$R_L = 7.5 \Omega$
Fall time	t_f	—	65	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -7 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	65	—	ns	$I_F = -7 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

- Note: 4. Pulse test

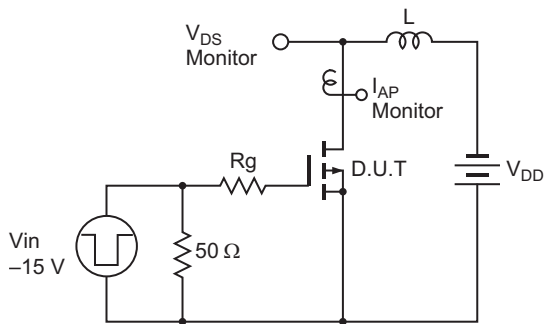
Main Characteristics





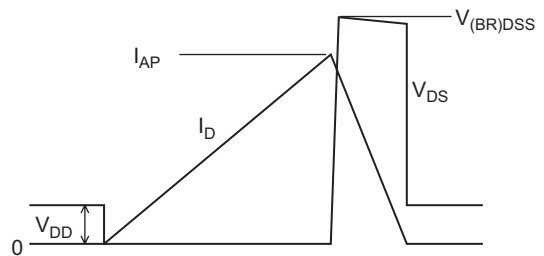


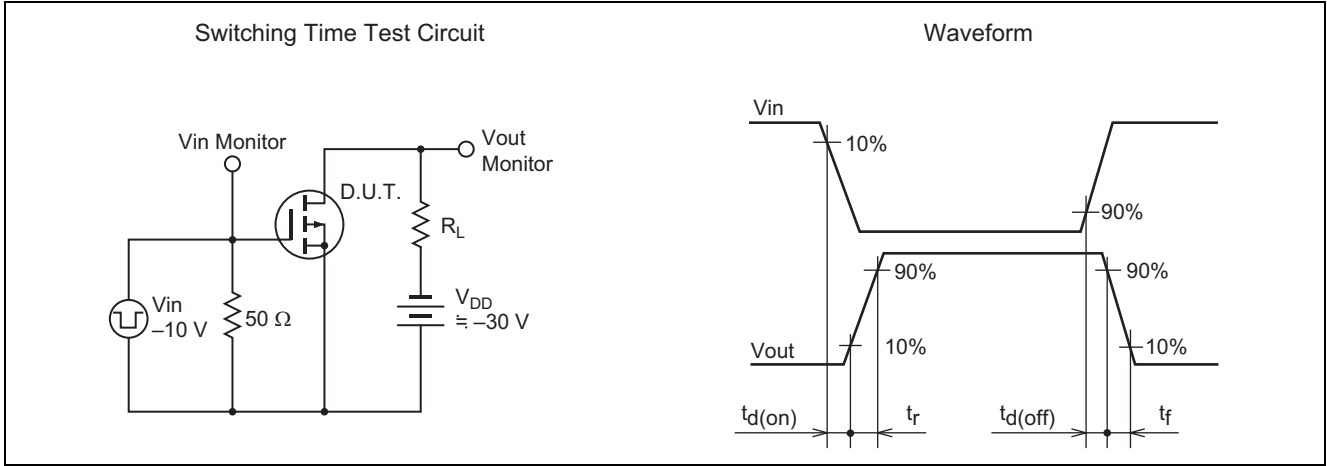
Avalanche Test Circuit



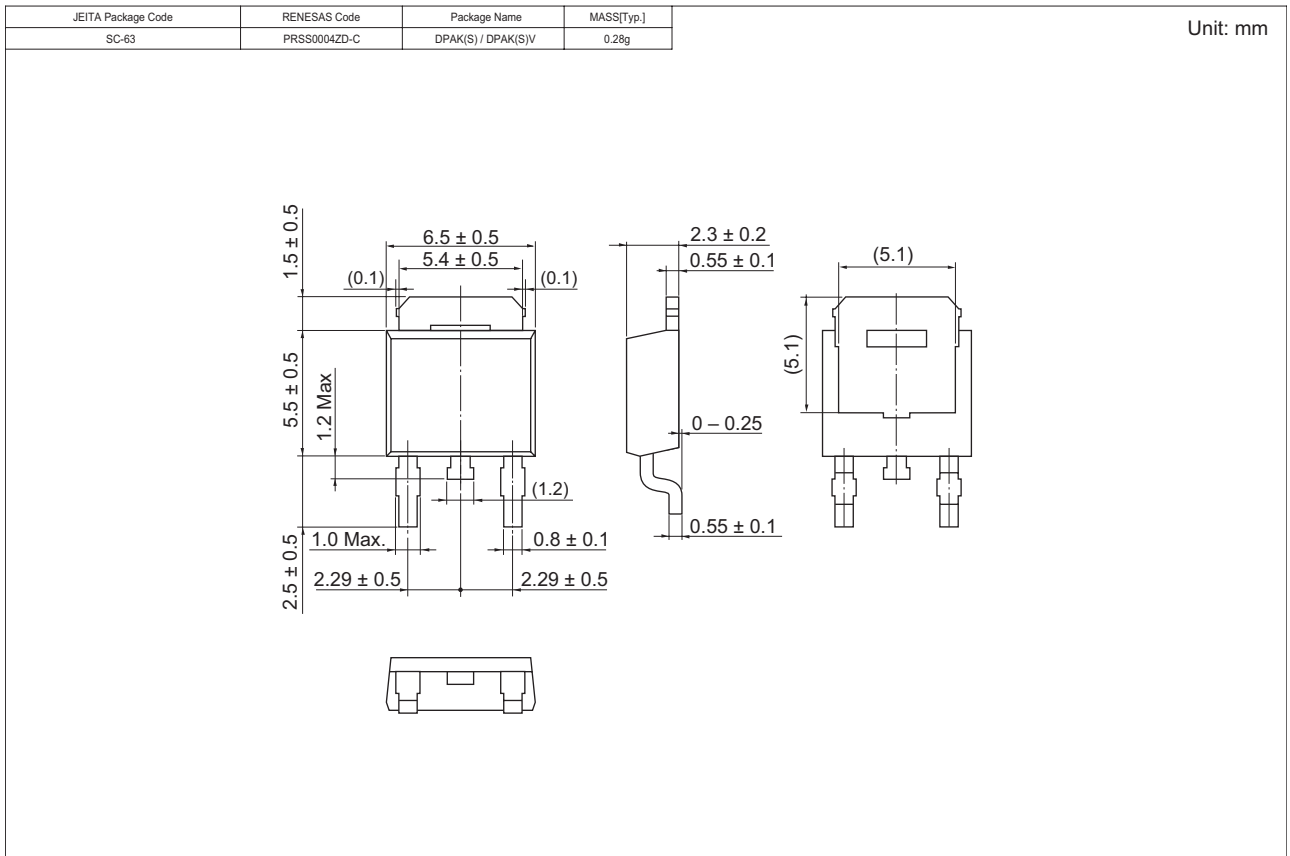
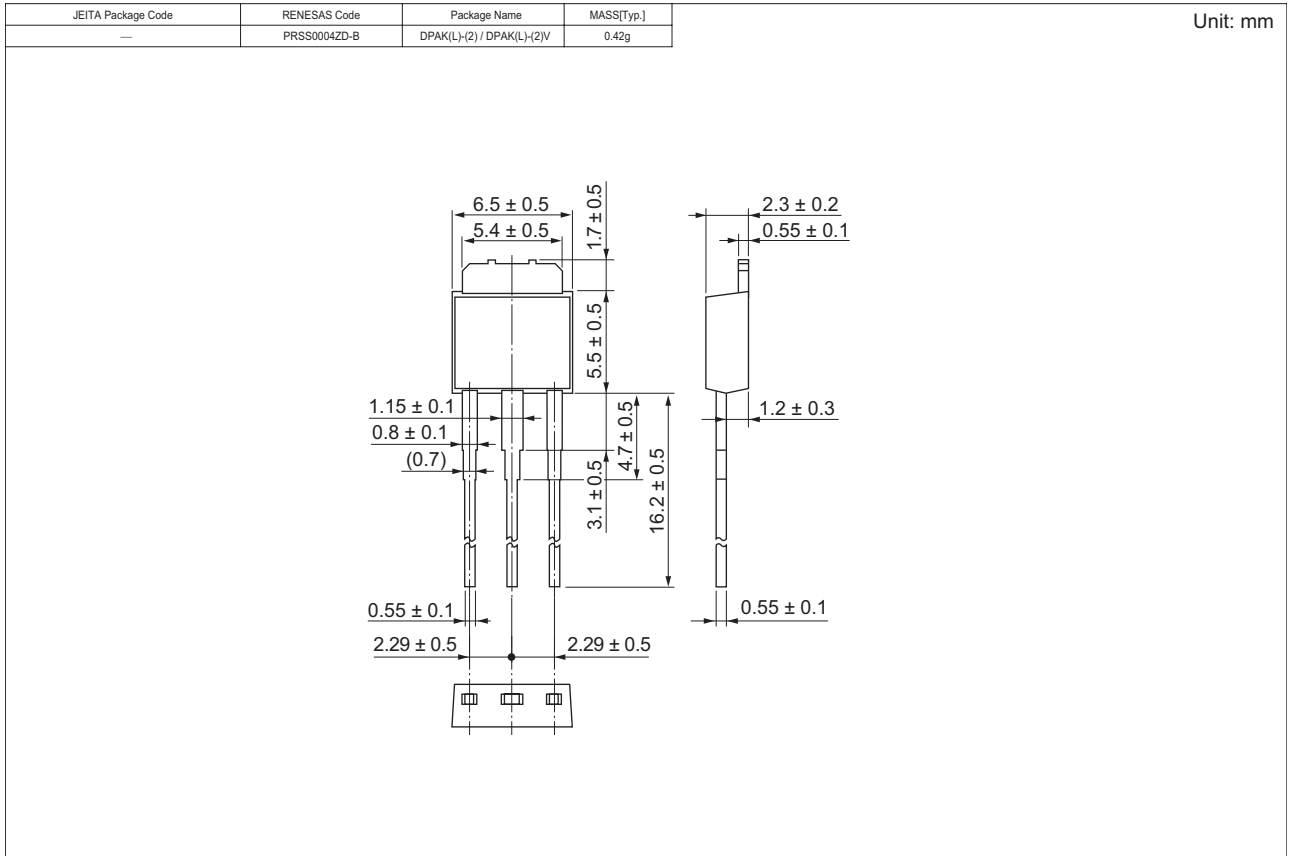
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ528L-E	3200 pcs	Box (Sack)
2SJ528STL-E	3000 pcs	Taping

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