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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR **2SJ600**

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ600 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

· Low on-state resistance:

 $R_{DS(on)1} = 50 \text{ m}\Omega \text{ MAX.}$ (Vgs = -10 V, ID = -13 A)

 $R_{DS(on)2} = 79 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.0 \text{ V, ID} = -13 \text{ A)}$

• Low input capacitance:

 $C_{iss} = 1900 \text{ pF TYP.} (V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V})$

- · Built-in gate protection diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE			
2SJ600	TO-251 (MP-3)			
2SJ600-Z	TO-252 (MP-3Z)			

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-60	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V	
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	∓25	Α	
Drain Current (pulse) Note1	ID(pulse)	∓70	Α	
Total Power Dissipation (Tc = 25°C)	Рт	45	W	
Total Power Dissipation (T _A = 25°C)	Рт	1.0	W	
Channel Temperature	Tch	150	°C	
Storage Temperature	T _{stg}	-55 to +150	°C	
Single Avalanche Current Note2	las	-25	Α	
Single Avalanche Energy Note2	Eas	62.5	mJ	

(TO-251)



(TO-252)



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

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ELECTRICAL CHARACTERISTICS (TA = 25°C)

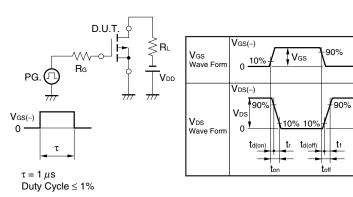
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μА
Gate Leakage Current	lgss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μА
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance Note	yfs	$V_{DS} = -10 \text{ V}, I_{D} = -13 \text{ A}$	10	20		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = -10 V, I _D = -13 A		41	50	mΩ
	R _{DS(on)2}	V _{GS} = -4.0 V, I _D = -13 A		55	79	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		1900		pF
Output Capacitance	Coss	V _G S = 0 V,		350		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		140		pF
Turn-on Delay Time	td(on)	I _D = −13 A,		9		ns
Rise Time	tr	V _{GS} = -10 V,		10		ns
Turn-off Delay Time	td(off)	$V_{DD} = -30 \text{ V},$		67		ns
Fall Time	tf	$R_G = 0 \Omega$		19		ns
Total Gate Charge	Q _G	lo = −25 A,		38		nC
Gate to Source Charge	Qgs	VDD= -48 V,		7		nC
Gate to Drain Charge	Q _{GD}	Vcs = -10 V		10		nC
Body Diode Forward Voltage Note	V _F (S-D)	IF = 25 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 25 A, VGS = 0 V		49		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		100		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

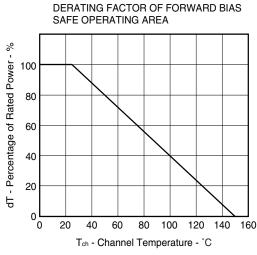
$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

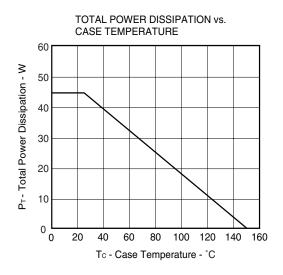
TEST CIRCUIT 2 SWITCHING TIME



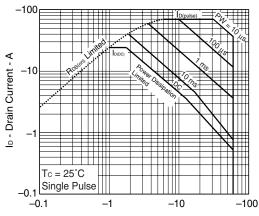
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

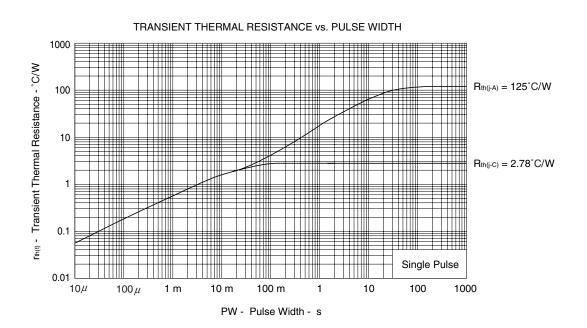








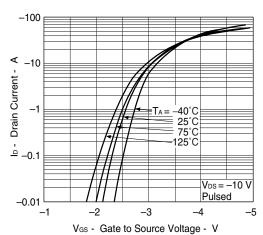
V_{DS} - Drain to Source Voltage - V



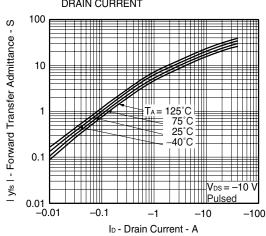
3

NEC 2SJ600

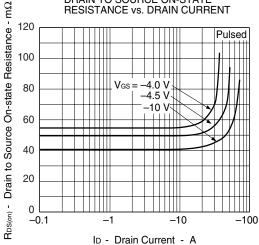
FORWARD TRANSFER CHARACTERISTICS



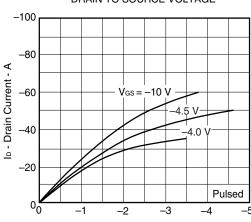
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

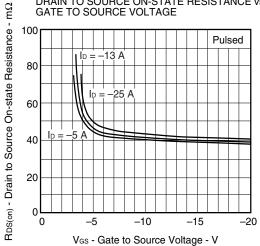


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

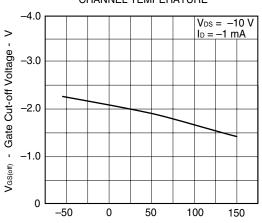


VDS - Drain to Source Voltage - V

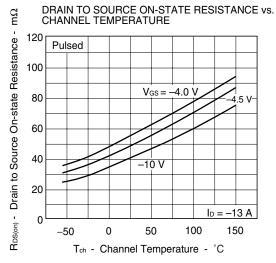
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

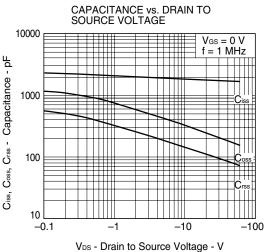


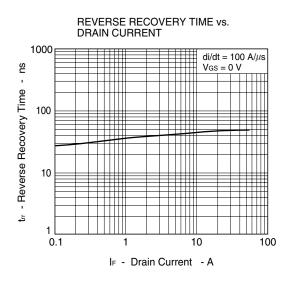
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

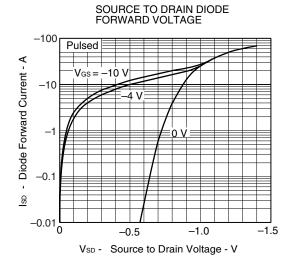


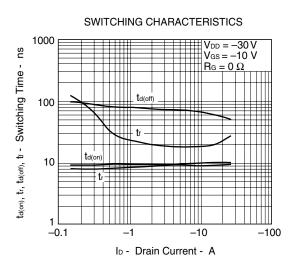
Tch - Channel Temperature - °C

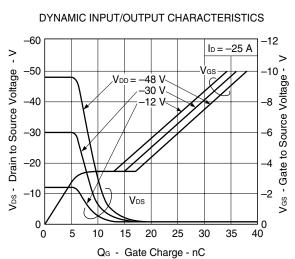




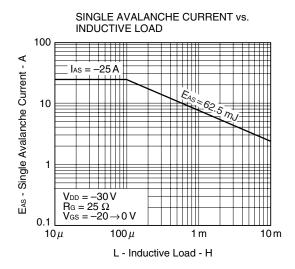


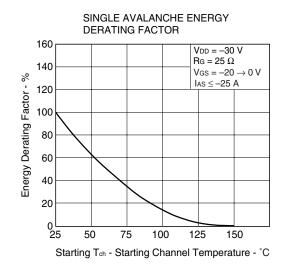




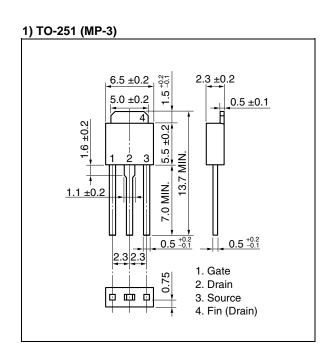


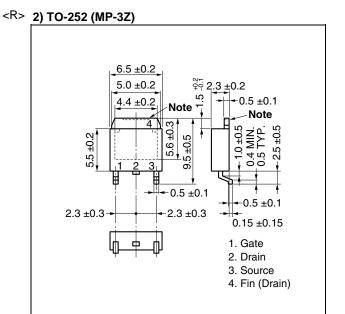
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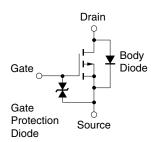
PACKAGE DRAWINGS (Unit: mm)





Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

NEC 2SJ600

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