

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# 2SK3147(L), 2SK3147(S)

Silicon N Channel MOS FET  
High Speed Power Switching

REJ03G1072-0300

Rev.3.00

Aug 17, 2009

## Features

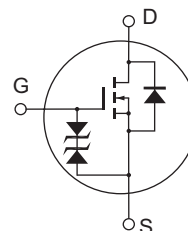
- Low on-resistance  
 $R_{DS} = 0.1 \Omega$  typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

## Outline

RENESAS Package code: PRSS0004ZD-B  
(Package name: DPAK(L)-(2))



RENESAS Package code: PRSS0004ZD-C  
(Package name: DPAK(S))



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	100	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	20	A
Body-drain diode reverse drain current	$I_{DR}$	5	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	5	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	2.5	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	20	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_c = 25^\circ\text{C}$   
 3. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$

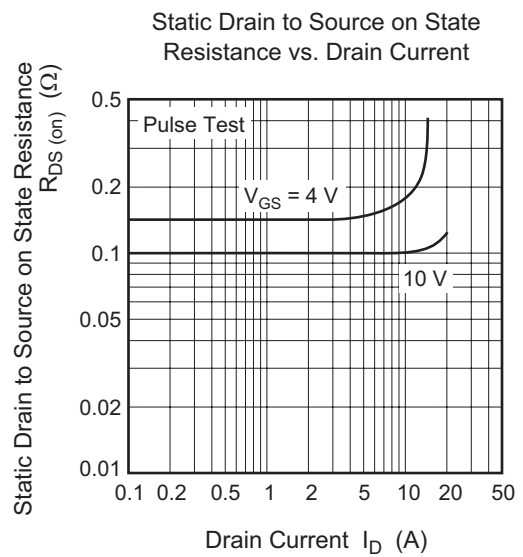
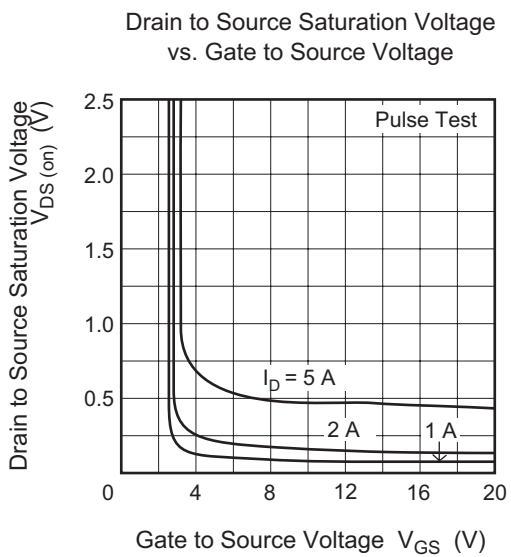
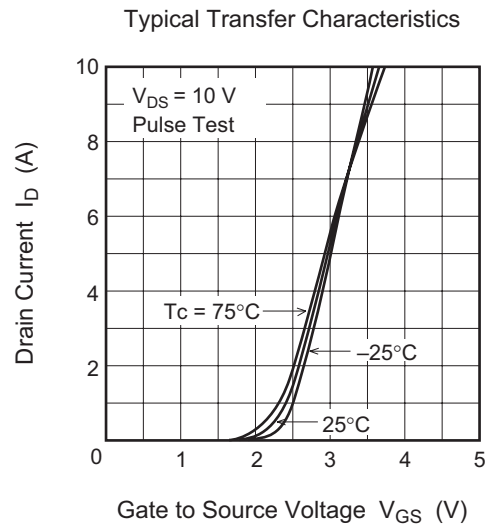
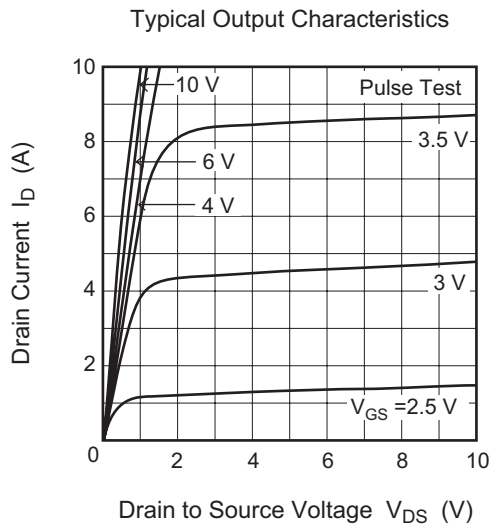
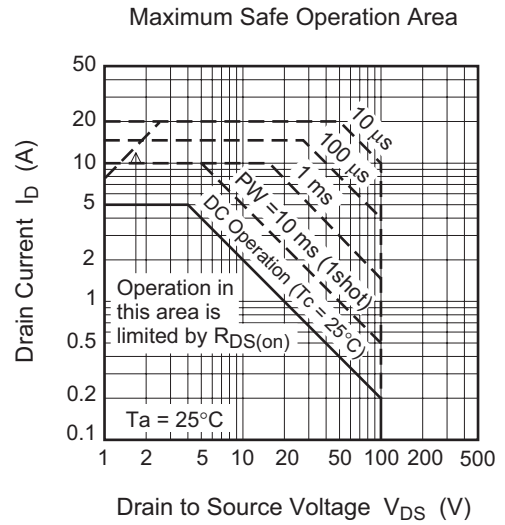
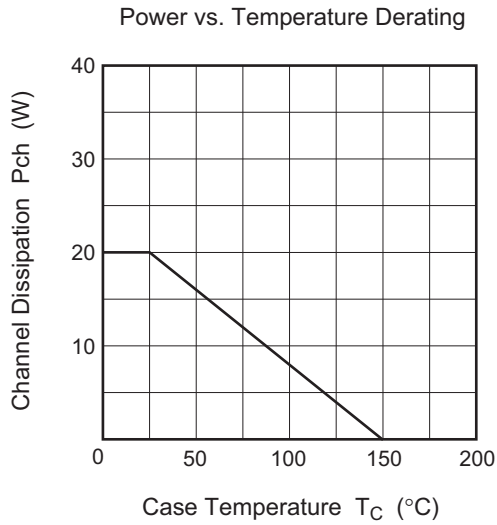
## Electrical Characteristics

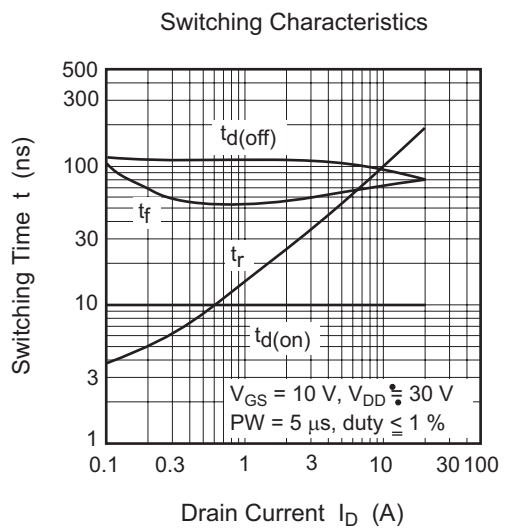
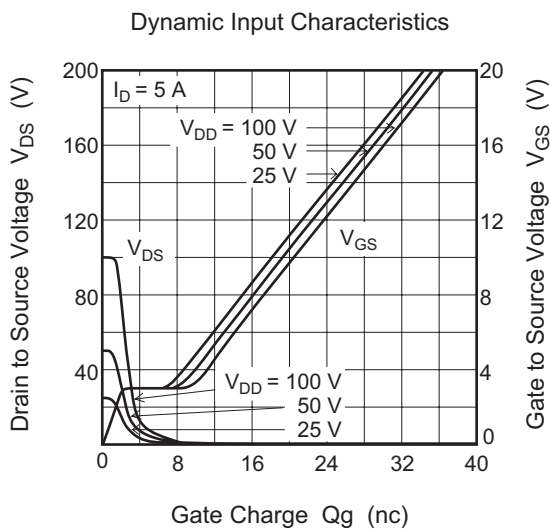
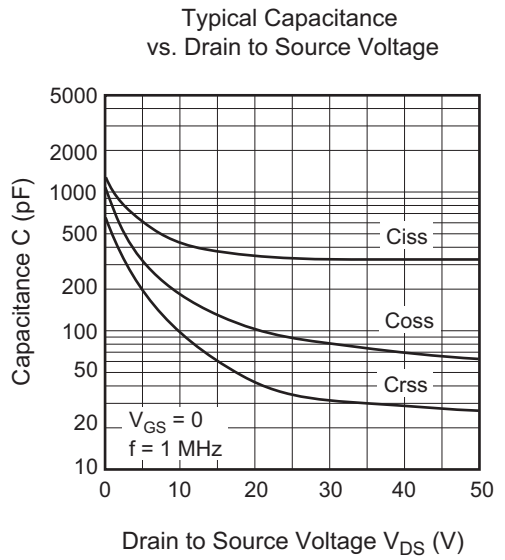
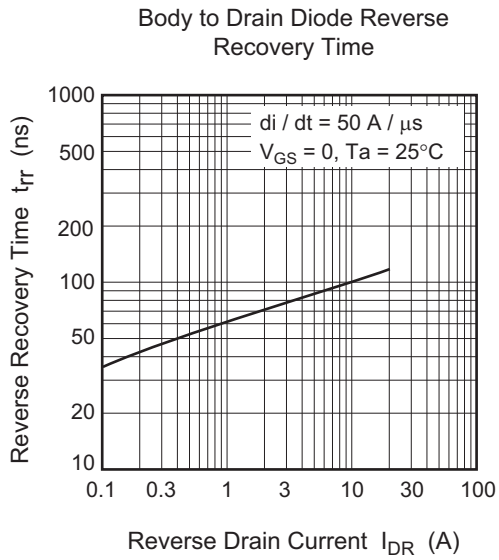
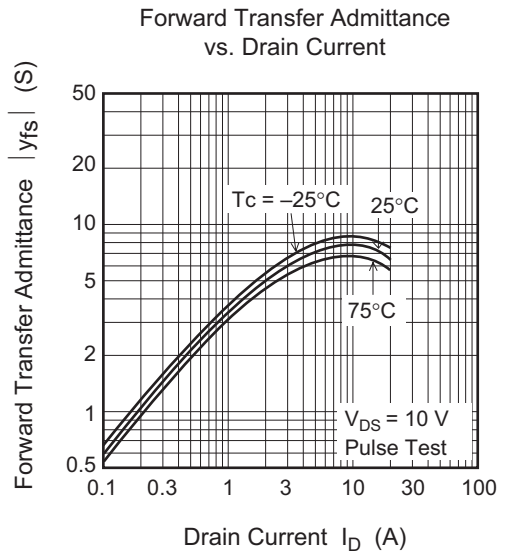
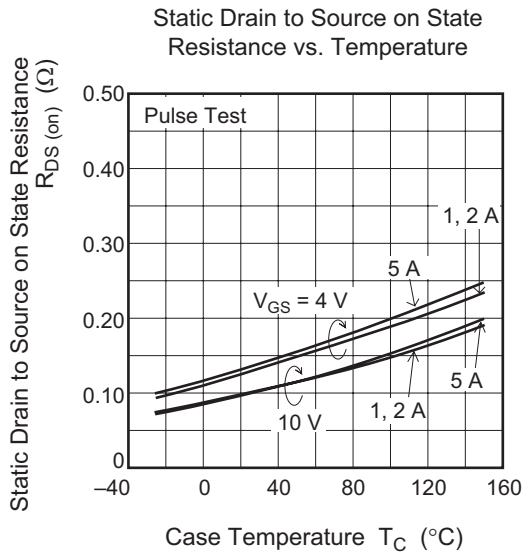
(Ta = 25°C)

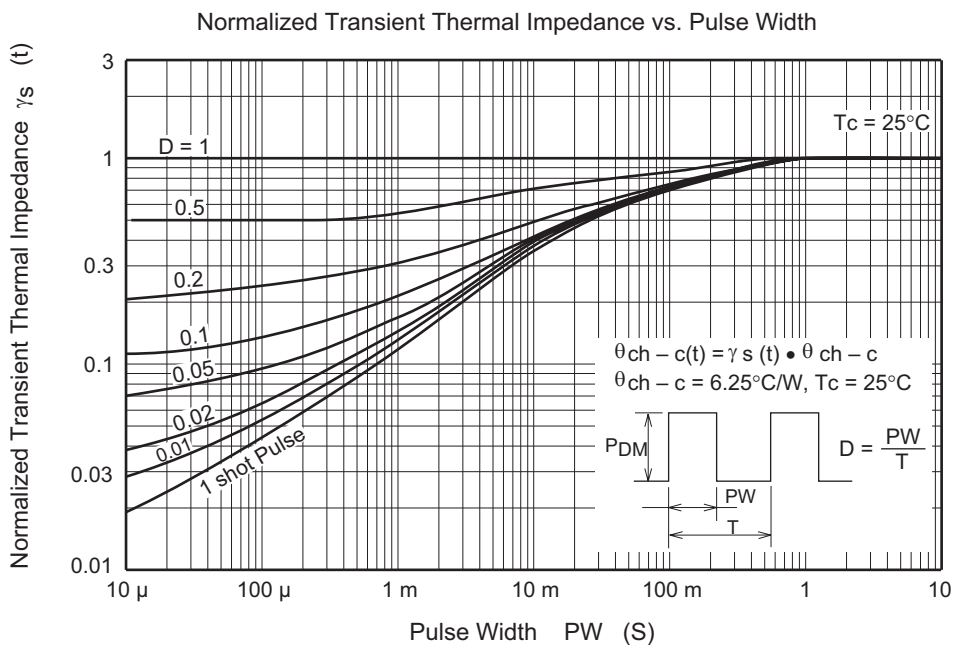
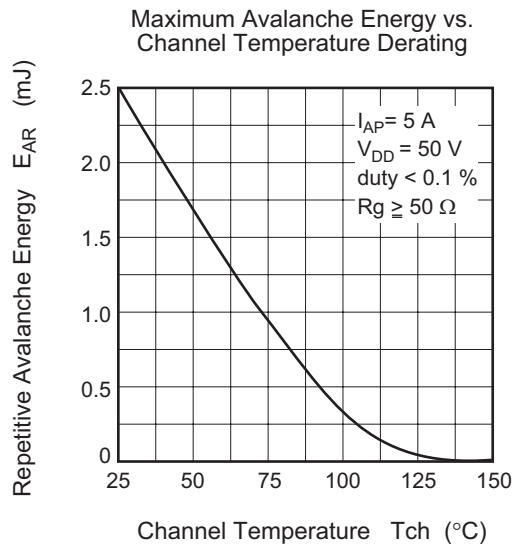
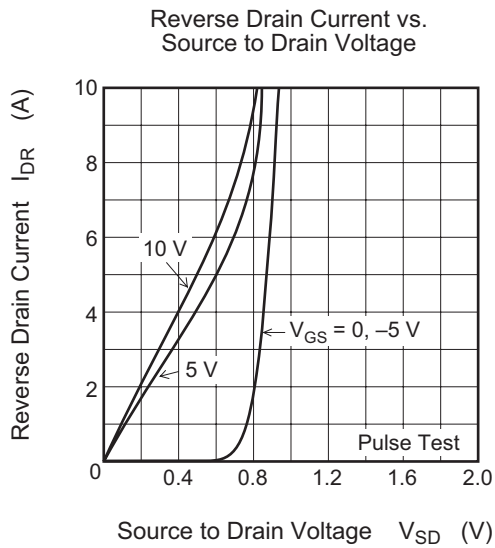
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 100 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.13	$\Omega$	$I_D = 3 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.13	0.17	$\Omega$	$I_D = 3 \text{ A}, V_{GS} = 4 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	3.5	6	—	S	$I_D = 3 \text{ A}, V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	420	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	185	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	100	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = 3 \text{ A}, V_{GS} = 10 \text{ V},$ $R_L = 10 \text{ }\Omega$
Rise time	$t_r$	—	35	—	ns	
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	$t_f$	—	60	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.85	—	V	$I_F = 5 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	85	—	ns	$I_F = 5 \text{ A}, V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

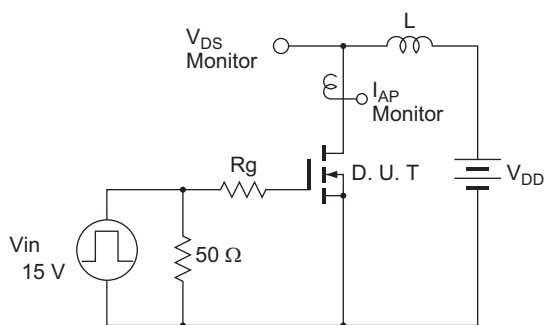
### Main Characteristics



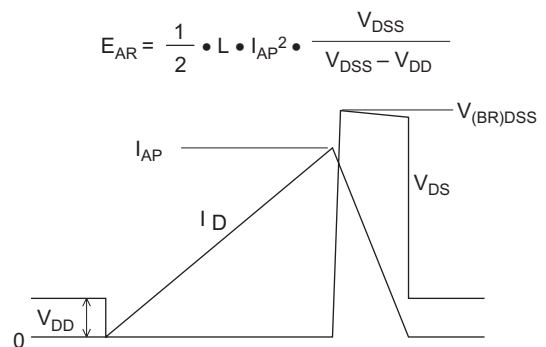


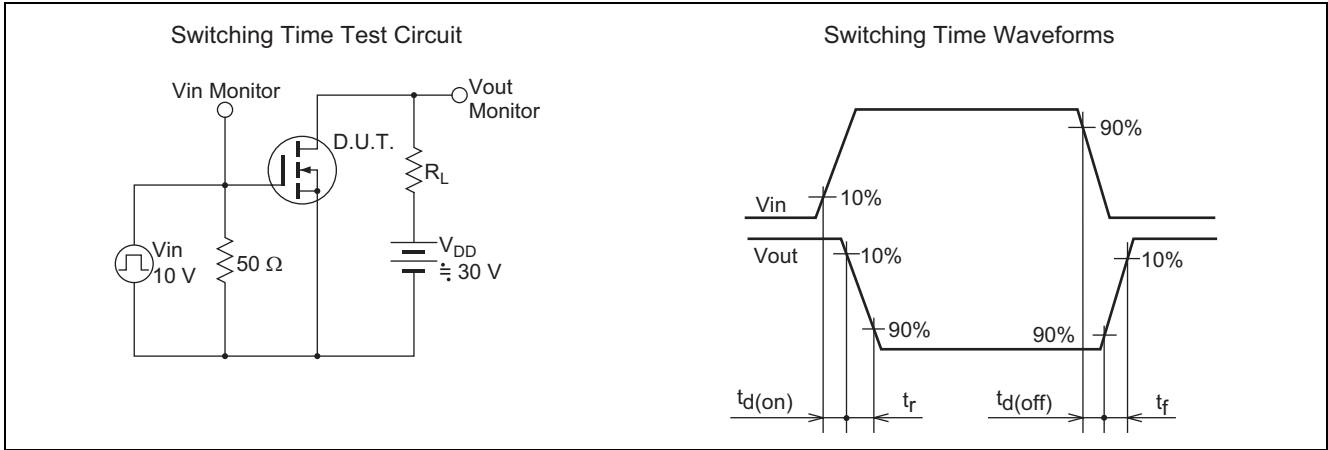


Avalanche Test Circuit



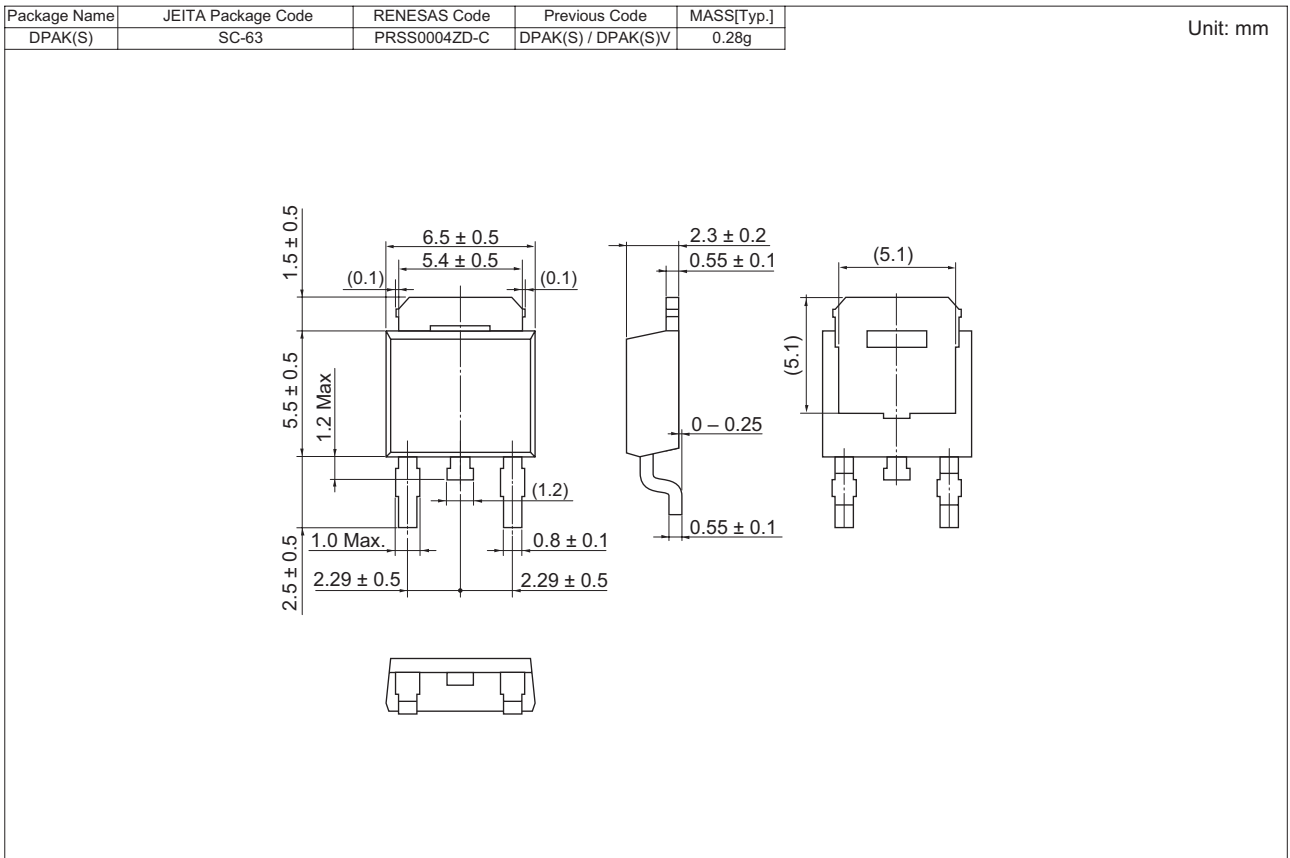
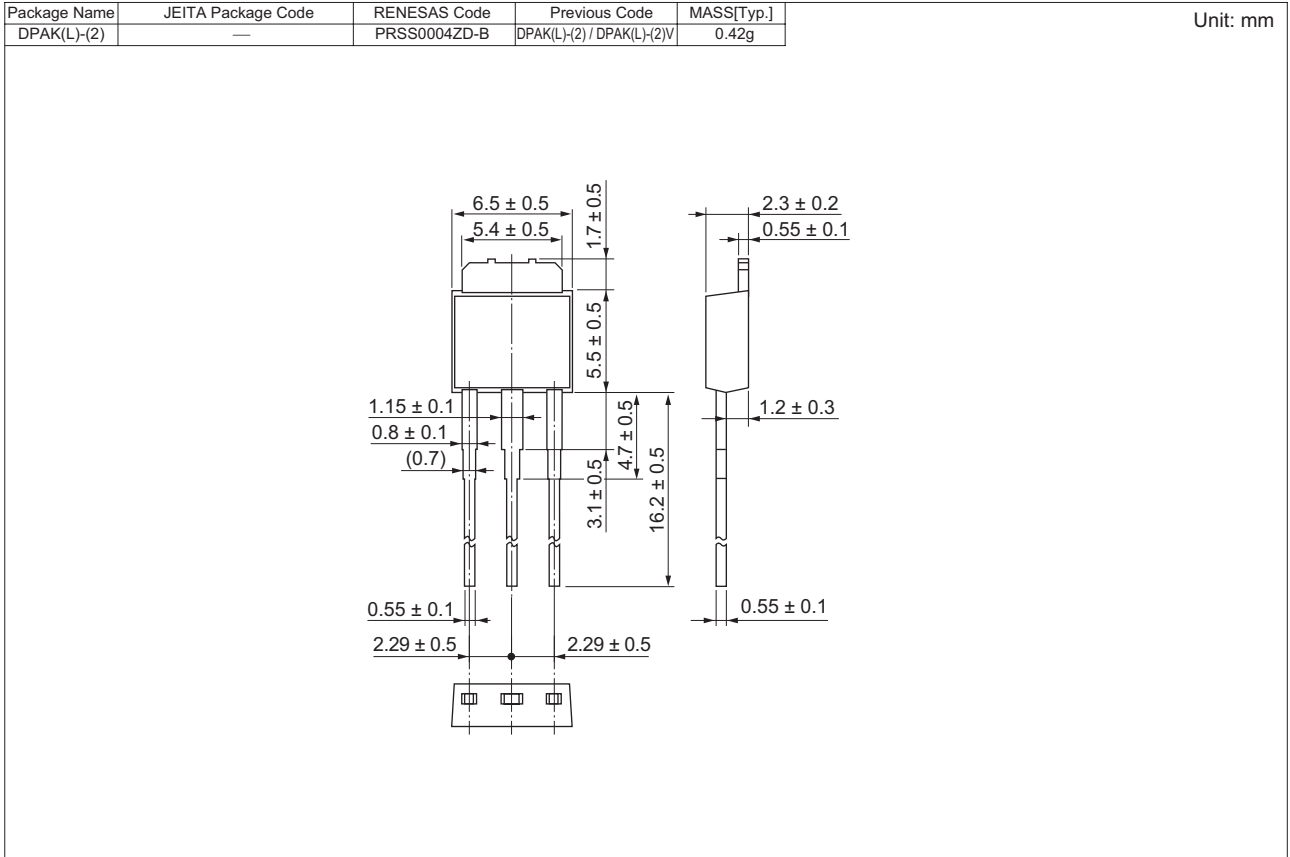
Avalanche Waveform







Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
2SK3147L-E	3200 pcs	Box (Sack)
2SK3147STL-E	3000 pcs	Taping

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