SemiSouth

Preliminary

Demo Board

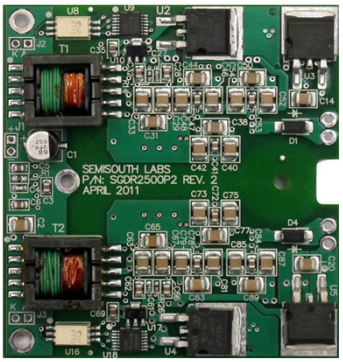
SGDR2500P2

Two-stage, dual-output, opto-coupled gate driver evaluation board

The SGDR2500P2 is an opto-isolated, two-stage gate driver optimized for high-speed hard switching of Microsemi's APTJC120AM13VCT1AG SiC JFET half-bridge power module. The SGDR2500P2 gate driver provides isolated high-side & low-side drivers with peak output currents of +20/-10 A for fast turn-on transients, yielding record-low switching energy losses.

Product Summary		
V_{DD}	+12	V
I_{PK}	+20/-10	A
$F_{SW(MAX)}$	100	kHz
Duty Cycle	0-100	%

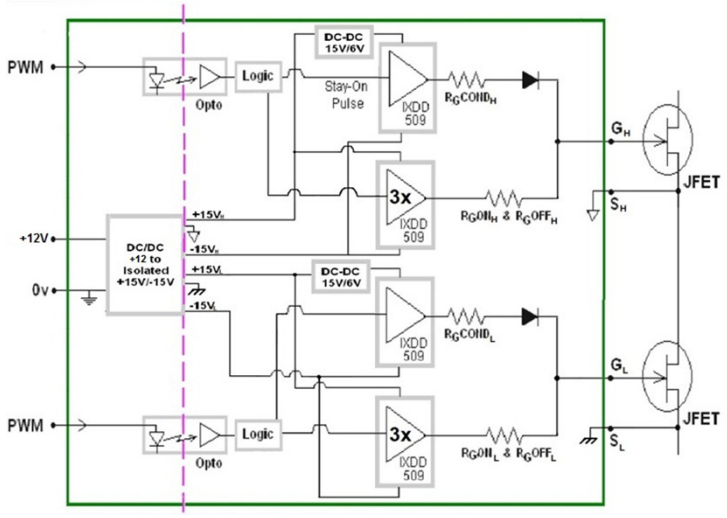
SGDR2500P2



Features:

- Suitable for driving Microsemi APTJC120AM13VCT1AG
- Isolated high-side and low-side outputs
- On-board derivation of isolated +/- 15 V supply voltages
- Two-stage driver - switching & conduction
- Peak gate current of +20/-10 A
- Switching frequency up to 100 kHz
- Duty cycle: 0 to 100%

Schematic Overview



Applications:

- Hard Switched Bridge Topologies
- Inverters/Converters
- Product Evaluation
- Research

- For operation principles and intended use, refer to Application note AN-SS5.

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Positive supply voltage	V_{CC}	to GND	+ 12	V
Input current logic HIGH	$I_{F(ON)}$	(high and low side inputs)	10	mA
Peak Output Current	I_O	Not connected to the JFET, output shorted to GND or pure capacitive load	+ 27	A
			- 27	
Operating temperature	T_{OP}		+ 85	℃
Storage temperature	T_{ST}		+ 100	℃

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
External Power Supplies						
Positive supply voltage	V_{CC}	to GND	+ 11.5		+12.5	V
Positive supply current	I_{CC}	without load		0.2		mA
		V_{CC} = +12 V, f = 100 kHz, D = 50%		1400		
Input (characteristics same for both inputs)						
Input forward voltage	V_F	I_F = 5 mA, T_A = 25 °C	1.4	1.60	1.70	V
Input voltage, OFF	$V_{F(OFF)}$		0	-	0.8	V
Input current, ON	$I_{F(ON)}$		4.5	-	10	mA
Input capacitance	C_{in}	V = 0V, f = 1 MHz, T_A = 25 °C	-	45	-	pF
Timing Characteristics						
Delay time input to output	$t_{d(ON)}$		-	130	-	ns
	$t_{d(OFF)}$		-	130	-	ns
Output (characteristics same for both outputs)						
Output voltage	V_O	Peak positive voltage clamped by JFET gate-source diode	- 15	-	+ 5V	V
Peak output current (1)	I_O	R_{GON} = 0.17 Ω	-	+ 20		A
		R_{GOFF} = 0.17 Ω		- 10	-	
Steady-state output current	I_{ODC}	limited by R_{GCOND}	-	500		mA
Output voltage rise time	t_{ro}		-	-	20	ns
Output voltage fall time	t_{fo}		-	-	20	ns
Electrical Isolation						
Creep path input-output			7.6	-	-	mm
Max ΔV/Δt at ΔV = TBD		10 kV used at 1000 Vp-p		TBD		kV/µs
Operating Conditions						
Operating Temperature	T_{OP}		0	-	+ 85	°C
Storage Temperature	T_{ST}		0	-	+ 100	°C

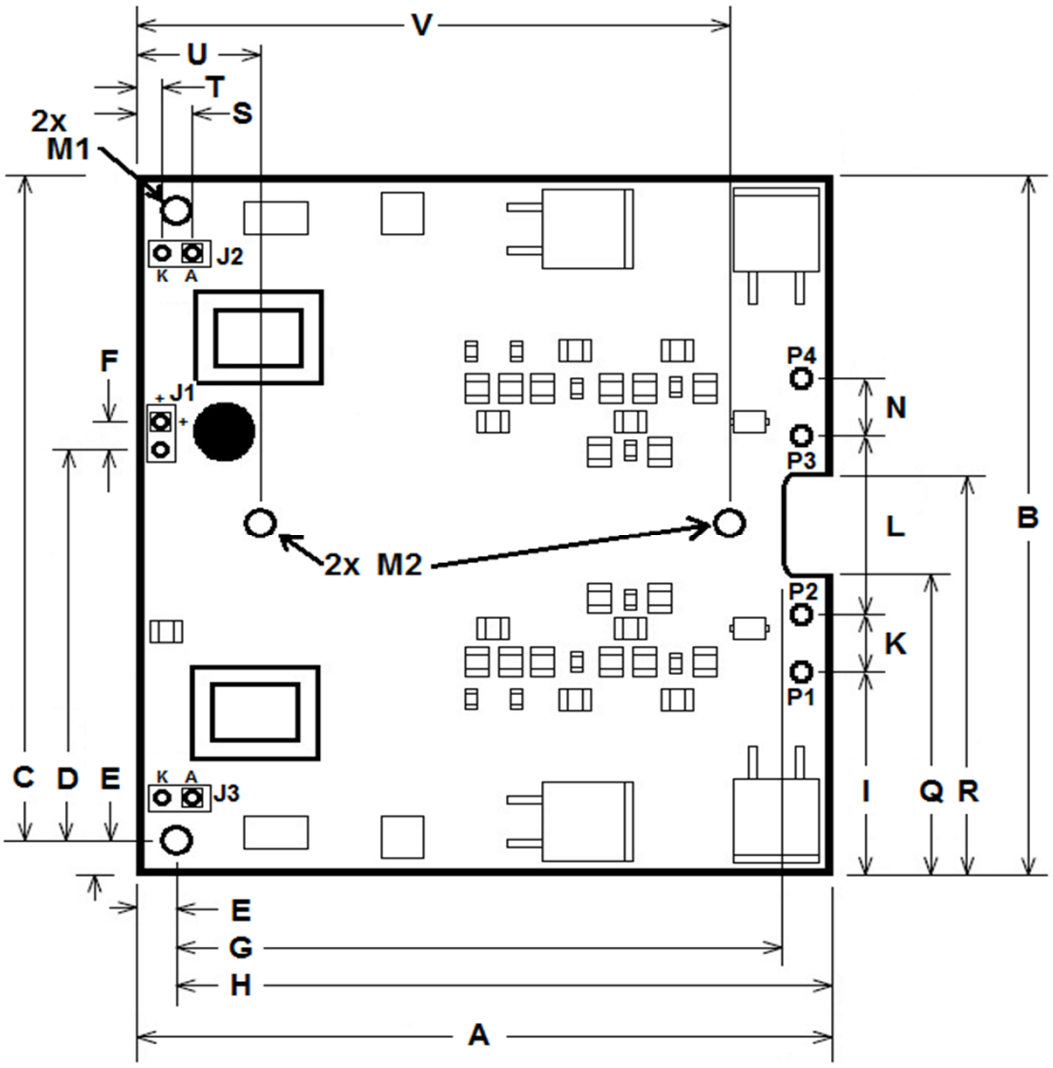
Notes:

(1) I_{PK} is limited by the JFET gate-source voltage (V_{GS}) and gate resistor (R_G). Pulse width is fixed at 100 ns. Connected to APTJC120AM13VCT1AG.

Package Pinout

Pin Descriptions						
J1	VCC	Voltage supply		**P1**	S_L	Low side source connection
J2	V_H	High side PWM (opto-coupler input)		**P2**	G_L	Low side gate connection
J3	V_L	Low side PWM (opto-coupler input)		**P3**	G_H	High side gate connection
				P4	S_H	High side source connection

Package Dimensions



Top View

	in.	mm
A	2.70	68.58
B	3.00	76.20
C	2.85	72.39
D	1.75	44.51
E	0.15	3.81
F	0.10	2.54
G	2.36	59.94
H	2.55	64.77
I	0.98	24.82
J1	0.04	1.09
J2	0.04	1.09
J3	0.04	1.09
K	0.15	3.81
L	0.75	19.05
M1	0.12	2.95
M2	0.12	2.95
N	0.15	3.81
P1	0.07	1.70
P2	0.07	1.70
P3	0.07	1.70
P4	0.07	1.70
Q	1.16	29.51
R	1.54	39.07
S	0.20	5.08
T	0.10	2.54
U	0.52	13.13
V	2.24	56.78

Published by
SemiSouth Laboratories, Inc.
201 Research Boulevard
Starkville, MS 39759 USA

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