CY2XF32

High Performance CMOS Oscillator with Frequency Margining – Pin Control

Features

- Crystal oscillator with CMOS output
- Output frequency from 8 MHz to 200 MHz
- Two frequency margining control pins (FS0, FS1)
- Output enable or power-down function
- Factory configured or field programmable
- Integrated phase-locked loop (PLL)
- Supply voltage: 3.3 V or 2.5 V
- Pb-free package: 5.0 × 3.2 mm LCC
- Commercial and industrial temperature ranges

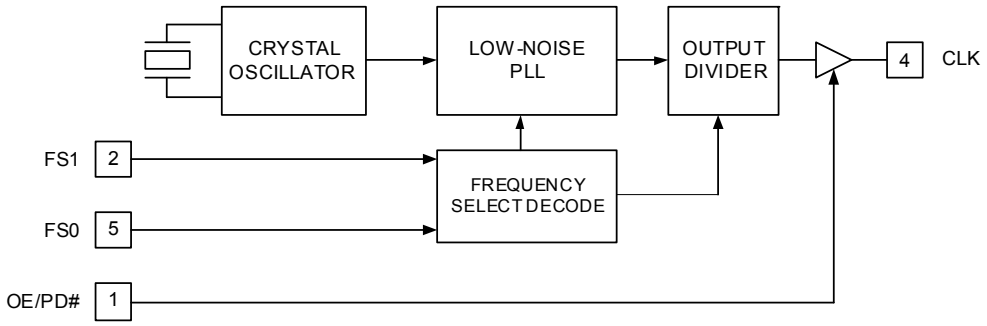
Functional Description

The CY2XF32 is a high performance and high frequency crystal oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed via two select pins, allowing easy frequency margin testing in applications.

The CY2XF32 is available as a factory configured device or as a field programmable device.

For a complete list of related documentation, click here.

Logic Block Diagram



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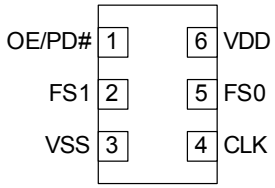
Pinouts

Figure 1. 6-pin Ceramic LCC pinout



Pin Definitions

6-pin Ceramic LCC

Pin No.	Pin Name	I/O Type	Description
1	OE/PD#	CMOS Input	Output Enable or Power-down: Functionality is a programming option; see Table 2 and Table 3 for details.
2, 5	FS1, FS0	CMOS Input	Frequency Select.
4	CLK	CMOS Output	Clock Output.
6	VDD	Power	Supply Voltage: 2.5 V or 3.3 V.
3	VSS	Power	Ground.

Functional Overview

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 1. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

Table 1. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

Pin 1 is programmed to function as either OE (output enable) or PD# (power-down, active low). The OE function is used to enable or disable the CLK output very quickly, but it does not reduce core power consumption. The PD# function puts the device into a low power state, but the wake up takes longer because the PLL must reacquire lock. Details are shown in Table 2 and Table 3.

Table 2. Output Enable Operation

OE	PLL & Xtal Oscillator	Output Buffer
0	Active	Off
1	Active	On

Table 3. Power-down Operation

PD#	PLL & Xtal Oscillator	Output Buffer
0	Off	Off
1	Active	On

Programming Description

The CY2XF32 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described below.

Field Programmable CY2XF32F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks™ Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF32 is one time programmable (OTP).

The software is located at www.cyberclocksonline.com.

Factory Configured CY2XF32

For ready-to-use devices, the CY2XF32 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Programming Variables

Output Frequencies

The CY2XF32 is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

Pin 1: Output Enable or Power-down (OE/PD#)

Pin 1 is programmed as either Output Enable (OE) or Power-down (PD#).

Supply Voltage

A programming option optimizes the CY2XF32 for either 2.5 V or 3.3 V supply voltage. A device programmed for a particular supply voltage is not guaranteed to meet specifications when operated at the other voltage.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Table 4. Device Programming Variables

Variable
Output Frequency 0 (Power on default)
Output Frequency 1
Output Frequency 2
Output Frequency 3
Pin 1 Functionality (OE or PD#)
Supply Voltage (2.5 V or 3.3 V)
Temperature Range (Commercial or Industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–55	135	°C
T_J	Temperature, Junction		–40	135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3 V Supply Voltage Range	3.135	3.3	3.465	V
	2.5 V Supply Voltage Range	2.375	2.5	2.625	V
T_{PU}	Power-up Time for V_{DD} to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	–	500	ms
T_A	Ambient Temperature, Commercial	0	–	70	°C
	Ambient Temperature, Industrial	–40	–	85	°C
C_{LOAD}	Load Capacitance at CLK (>100 MHz)	–	–	10	pF
	Load Capacitance at CLK (≤100 MHz)	–	–	15	pF

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has four layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	V_{DD} = 3.465 V, OE/PD# = V_{DD}, output unloaded	–	–	110	mA
I_{SB}	Standby Supply Current	PD# = V_{SS}	–	–	200	µA
V_{OH}	Output High Voltage	V_{DD} = min, I_{OH} = –4 mA	0.9 × V_{DD}	–	–	V
V_{OL}	Output Low Voltage	V_{DD} = max, I_{OL} = 4 mA	–	–	0.1 × V_{DD}	V
I_{OZ}	Output Leakage Current	OE/PD# = V_{SS}	–35	–	35	µA
V_{IH}	Input High Voltage		0.7 × V_{DD}	–	–	V
V_{IL}	Input Low Voltage		–	–	0.3 × V_{DD}	V
I_{IH0}	Input High Current, OE/PD# Pin	Input = V_{DD}	–	–	115	µA
I_{IH1}	Input High Current, FS0 & FS1 Pins	Input = V_{DD}	–	–	10	µA
I_{IL0}	Input Low Current, OE/PD# Pin	Input = V_{SS}	–50	–	–	µA
I_{IL1}	Input Low Current, FS0 & FS1 Pin	Input = V_{SS}	–20	–	–	µA
C_{IN0}[3]	Input Capacitance, OE/PD# Pin		–	15	–	pF
C_{IN1}[3]	Input Capacitance, FS0 & FS1 Pin		–	4	–	pF

Note
3. Not 100% tested, guaranteed by design and characterization.

AC Electrical Characteristics

Parameter [4]	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output Frequency[5]		8	–	200	MHz
FSC	Frequency Stability, Commercial Devices[6]	T_A = 0 °C to 70 °C	–	–	±35	ppm
FSI	Frequency Stability, Industrial Devices[6]	T_A = –40 °C to 85 °C	–	–	±55	ppm
AG	Aging, 10 Years		–	–	±15	ppm
T_{DC}	Output Duty Cycle	Measured at $V_{DD}/2$; see Figure 2	45	50	55	%
T_R	Output Rise Time	20% to 80% of V_{DD}, C_{LOAD} = 15 pF	–	0.7	1.5	ns
T_F	Output Fall Time	80% to 20% of V_{DD}, C_{LOAD} = 15 pF	–	0.8	1.5	ns
T_{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.) or from PD# rising edge	–	–	5	ms
T_{LFS}	Relock Time	Time for CLK to reach valid frequency from FS0 or FS1 pin change	–	–	1	ms

Notes
4. Not 100% tested, guaranteed by design and characterization.
5. This parameter is specified in CyberClocks Online software.
6. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, plus variation from temperature and supply voltage.

Switching Waveforms

Figure 2. Duty Cycle Timing

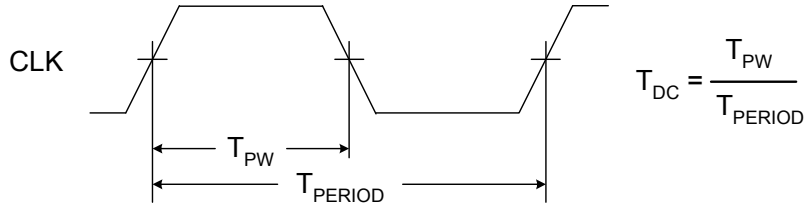


Figure 3. Output Rise and Fall Time

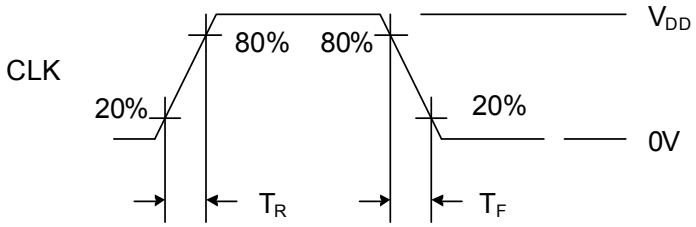
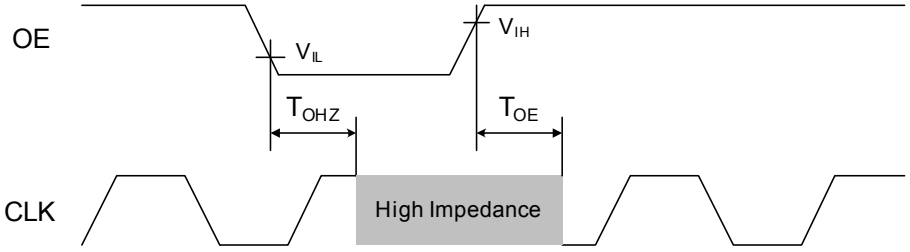


Figure 4. Output Enable and Disable Timing



Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

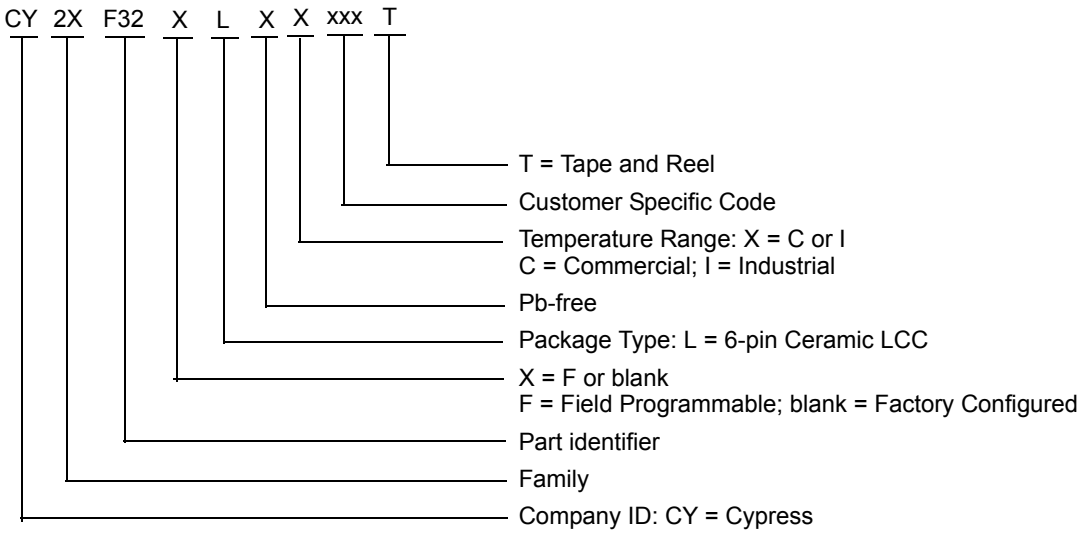
Part Number [7]	Configuration	Package Description	Product Flow
Pb-free			
CY2XF32FLXIT	Field Programmable	6-pin Ceramic LCC – Tape and Reel	Industrial, –40 °C to 85 °C

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE of Sales Representative for more information.

Possible Configurations

Part Number [7]	Configuration	Package Description	Product Flow
Pb-free			
CY2XF32LXCxxxT	Factory Configured	6-pin Ceramic LCC – Tape and Reel	Commercial, 0 °C to 70 °C
CY2XF32LXIxxxT	Factory Configured	6-pin Ceramic LCC – Tape and Reel	Industrial, –40 °C to 85 °C

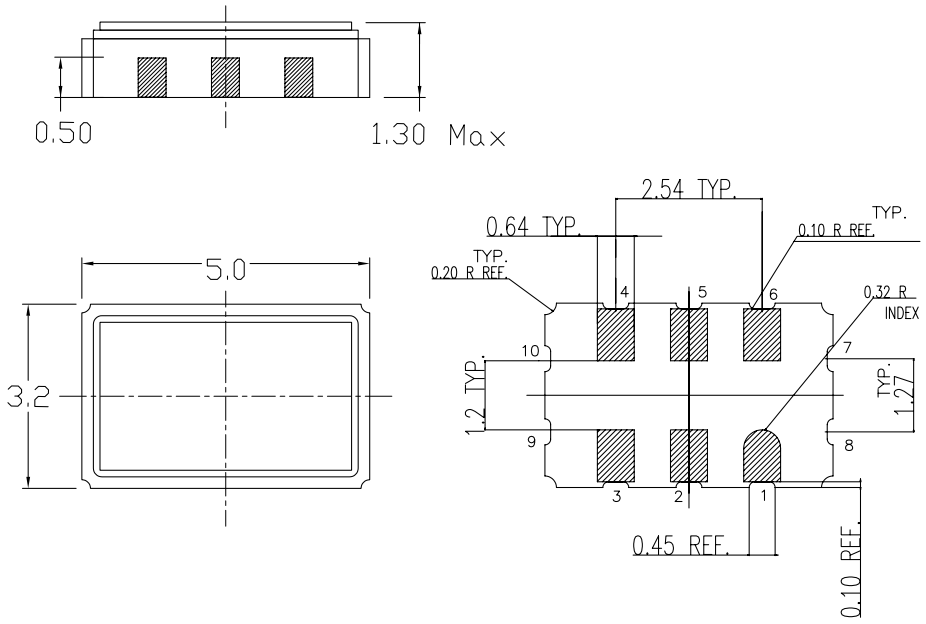
Ordering Code Definitions



Note
7. "xxx" is a factory assigned code that identifies the programming option.

Package Diagram

Figure 5. 6-pin Ceramic LCC (5.0 × 3.2 × 1.3 mm) LZ06A Package Outline, 001-10044



Dimensions in mm
Kyocera dwg ref KD-VA6432-A
Package Weight ~ 0.12 grams

001-10044 *C

Acronyms

Acronym	Description
CLKOUT	Clock Output
CMOS	Complementary Metal Oxide Semiconductor
DPM	Die Pick Map
EPROM	Erasable Programmable Read Only Memory
LVDS	Low-Voltage Differential Signaling
NTSC	National Television System Committee
OE	Output Enable
PAL	Phase Alternate Line
PD	Power-Down
PLL	Phase Locked Loop
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
ppm	parts per million
W	watt

Document History Page

Document Title: CY2XF32, High Performance CMOS Oscillator with Frequency Margining – Pin Control Document Number: 001-53147				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2705753	05/13/09	KVM / PYRS	New data sheet.
*A	2734005	07/09/2009	WWZ	Post to external web.
*B	2764787	09/19/2009	KVM	Change I_{SB} max from 250 µA to 200 µA Add max limit for T_R, T_F: 1.5 ns Change T_{LOCK} max from 10 ms to 5 ms Change T_{LFS} max from 10 ms to 1 ms
*C	2958629	06/22/10	KVM	Updated Ordering Information. Updated Package Diagram.
*D	3169028	05/06/10	BASH	Changed status from Preliminary to Final. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated template as per current Cypress standards.
*E	4398514	06/04/2014	AJU	Updated Package Diagram: spec 001-10044 – Changed revision from *A to *B. Updated in new template. Completing Sunset Review.
*F	4570063	11/14/2014	AJU	Added related documentation hyperlink in page 1. Removed the prune part number CY2XF32FLXCT in Ordering Information. Updated Figure 5 in Package Diagram (spec 001-10044 *B to *C).

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