

Features

- Pin- and function-compatible with CY7C1046CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 100 \text{ MHz}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in lead-free 400-mil-wide 32-pin SOJ package

Functional Description

The CY7C1046DV33 is a high-performance CMOS static RAM organized as 1M words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{19}).

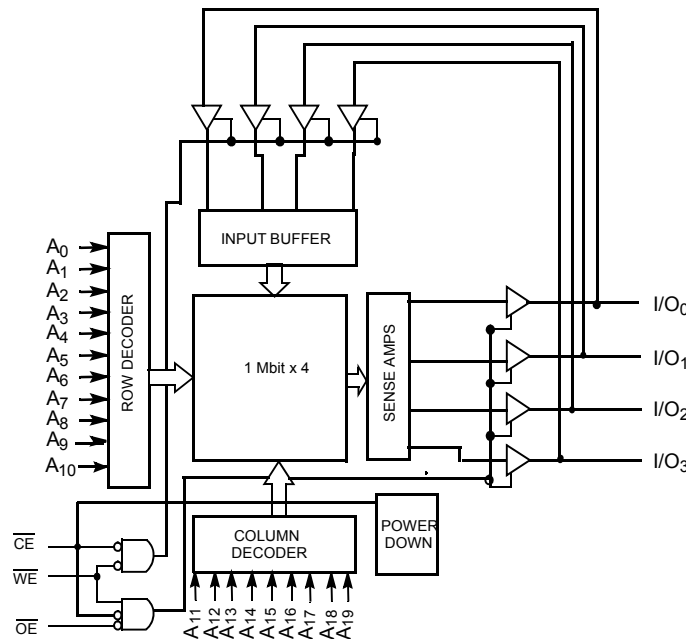
Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1046DV33 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

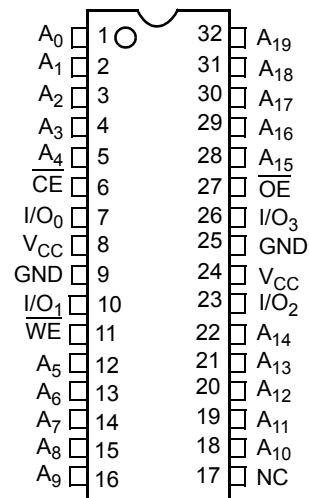
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Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	90	mA
Maximum CMOS standby current	10	mA

Pin Configuration

Figure 1. 32-pin SOJ (Top View)



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage on V _{CC} to relative GND ^[1]	-0.3 to +4.6 V
DC voltage applied to outputs in high Z State ^[1]	-0.3 V to V _{CC} + 0.3 V

DC input voltage ^[1]	-0.3 V to V _{CC} + 0.3 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
V _{OH}	Output HIGH voltage	Min V _{CC} , I _{OH} = -4.0 mA	2.4	-	V	
V _{OL}	Output LOW voltage	Min V _{CC} , I _{OL} = 8.0 mA	-	0.4	V	
V _{IH}	Input HIGH voltage		2.0	V _{CC} + 0.3	V	
V _{IL}	Input LOW voltage ^[1]		-0.3	0.8	V	
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	-1	+1	μA	
I _{OZ}	Output leakage current	GND ≤ V _{OUT} ≤ V _{CC} , output disabled	-1	+1	μA	
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, f = f _{MAX} = 1/t _{RC}	100 MHz	-	90	mA
			83 MHz	-	80	mA
			66 MHz	-	70	mA
			40 MHz	-	60	mA
I _{SB1}	Automatic CE power-down Current – TTL inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	-	20	mA	
I _{SB2}	Automatic CE power-down Current – CMOS inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V, f = 0	-	10	mA	

Capacitance

Parameter ^[2]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	I/O capacitance		8	pF

Thermal Resistance

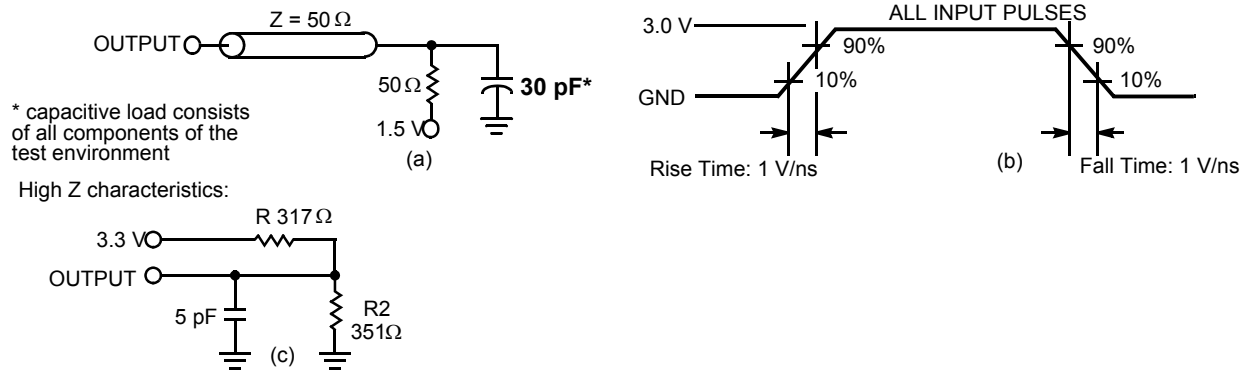
Parameter ^[2]	Description	Test Conditions	32-pin SOJ Package	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	53.44	°C/W
θ _{JC}	Thermal resistance (junction to case)		38.25	°C/W

Notes

- V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [3]



Note

3. AC characteristics (except high Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

AC Switching Characteristics

Over the Operating Range

Parameter ^[4]	Description	-10		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[5]}$	V_{CC} (typical) to the first access	100	–	μ s
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	10	ns
t_{DOE}	\overline{OE} LOW to data valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[6]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[6, 7]	–	5	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[6]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[6, 7]	–	5	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	10	ns
Write Cycle ^[8, 9]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	\overline{CE} LOW to write end	7	–	ns
t_{AW}	Address set-up to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	ns
t_{SD}	Data set-up to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[6]	3	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[6, 7]	–	5	ns

Notes

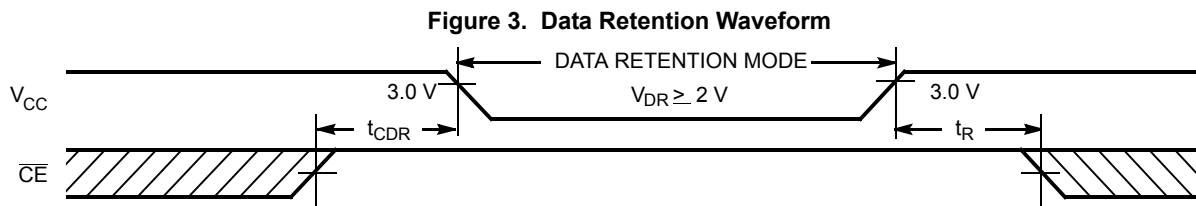
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of [Figure 2 on page 5](#). Transition is measured when the outputs enter a high impedance state.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics

Over the Operating Range

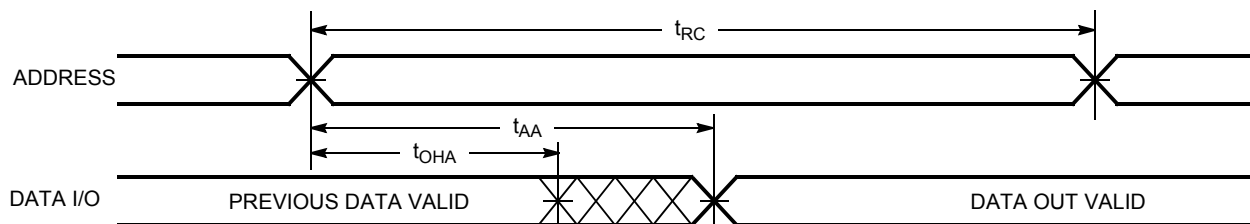
Parameter	Description	Conditions ^[10]	Min	Max	Unit
V _{DR}	V _{CC} for data retention	–	2.0	–	V
I _{CCDR}	Data retention current	V _{CC} = V _{DR} = 2.0 V, $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V	–	10	mA
t _{CDR} ^[11]	Chip deselect to data retention time	–	0	–	ns
t _R ^[12]	Operation recovery time	–	t _{RC}	–	ns

Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) ^[13, 14]



Notes

- 10. No inputs may exceed V_{CC} + 0.3 V.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 50 μs or stable at V_{CC(min.)} ≥ 50 μs.
- 13. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 14. WE is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]

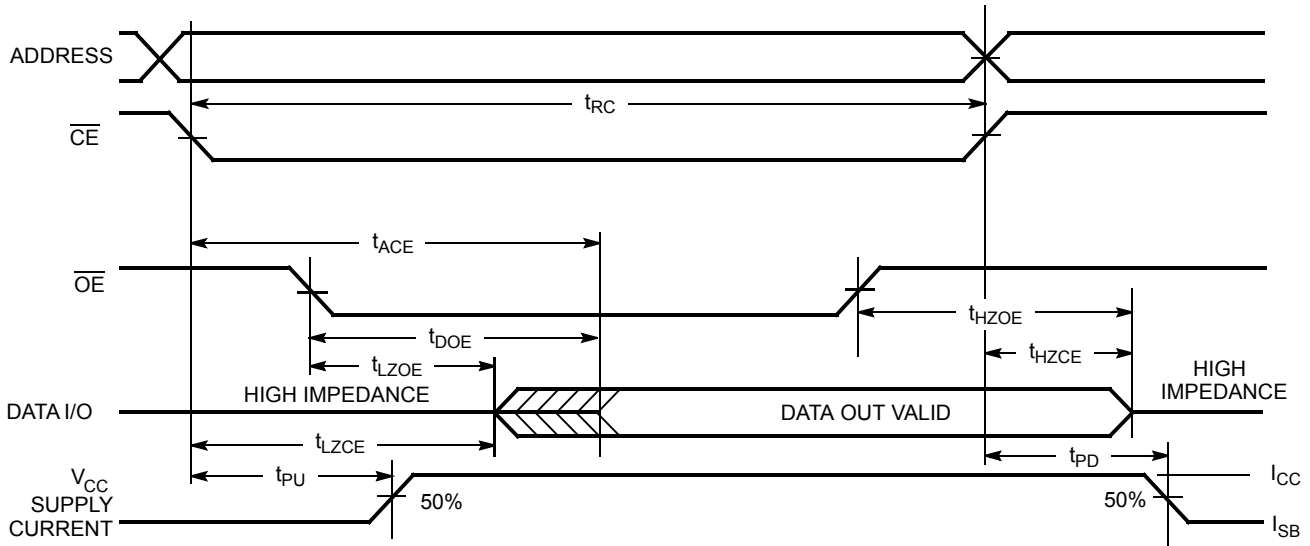
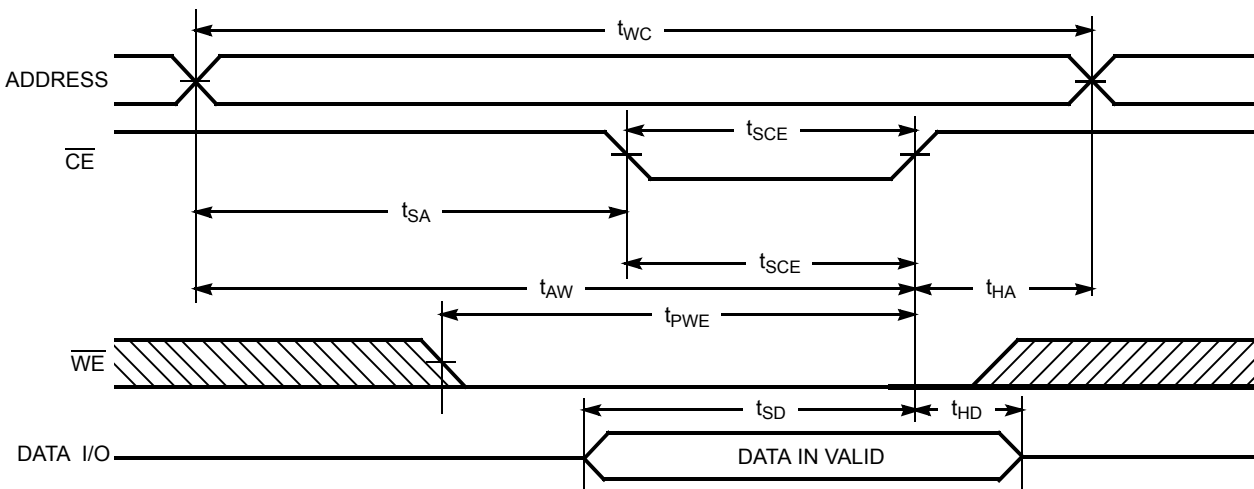


Figure 6. Write Cycle No. 1 (\overline{CE} Controlled) [17, 18]



Notes

- 15. \overline{WE} is HIGH for Read cycle.
- 16. Address valid prior to or coincident with \overline{CE} transition LOW.
- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [19, 20]

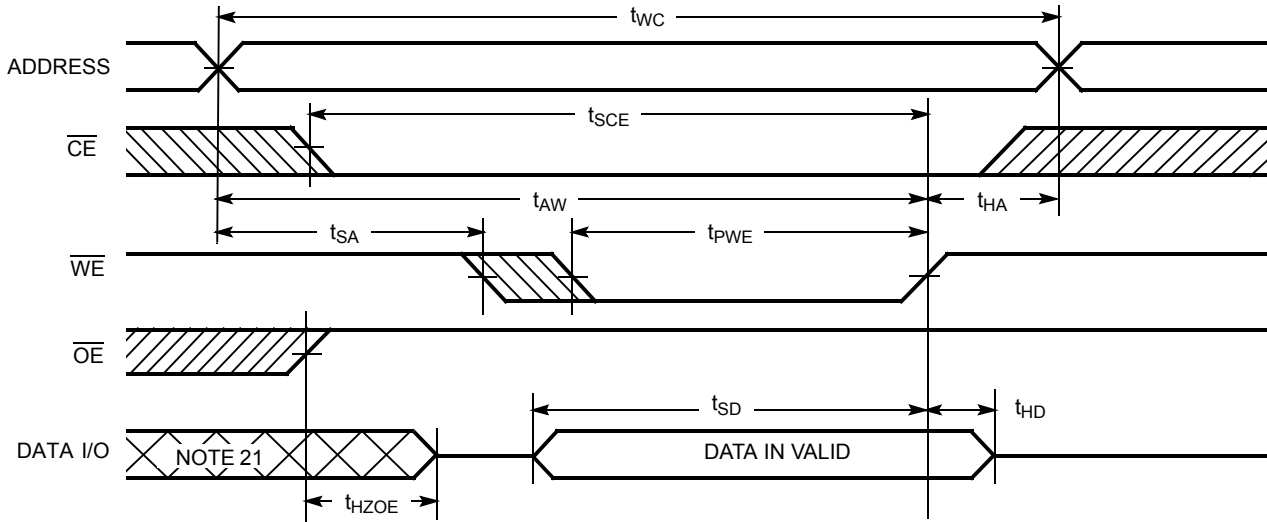
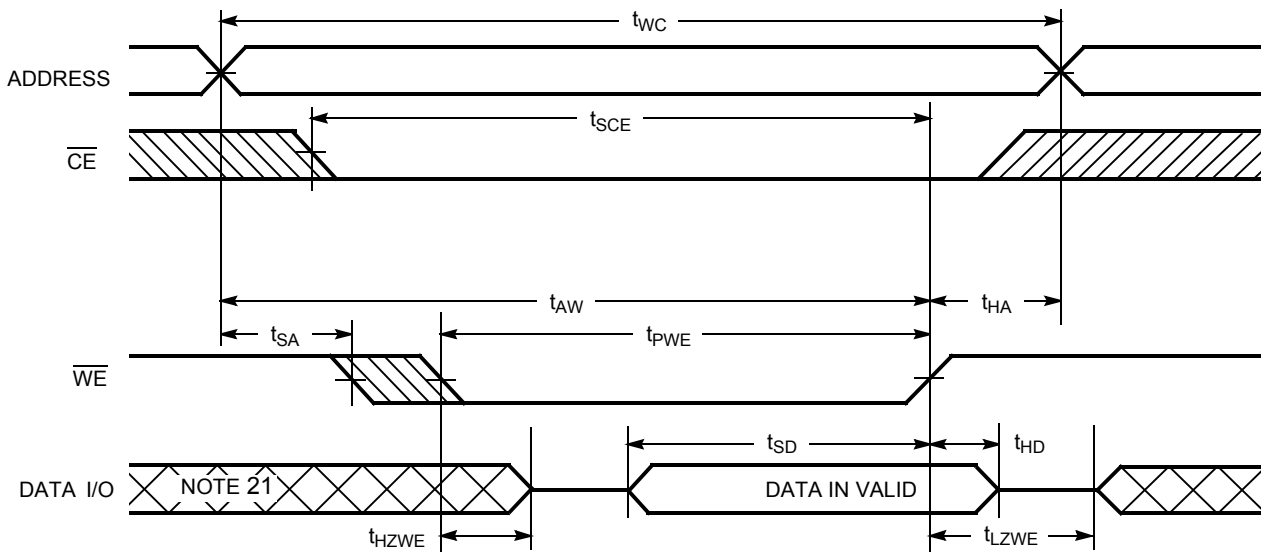


Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [20]



Notes

- 19. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 20. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 21. During this period the I/Os are in the output state and input signals should not be applied.

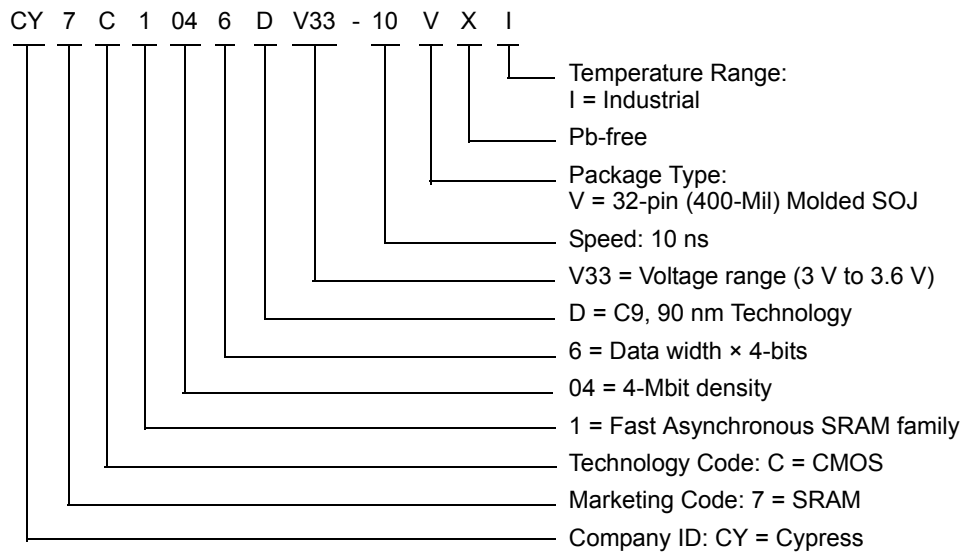
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ –I/O ₃	Mode	Power
H	X	X	High Z	Power-down	Standby (I _{SB})
L	L	H	Data out	Read	Active (I _{CC})
L	X	L	Data in	Write	Active (I _{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1046DV33-10VXI	51-85033	32-lead (400-mil) Molded SOJ (Pb-free)	Industrial

Ordering Code Definitions

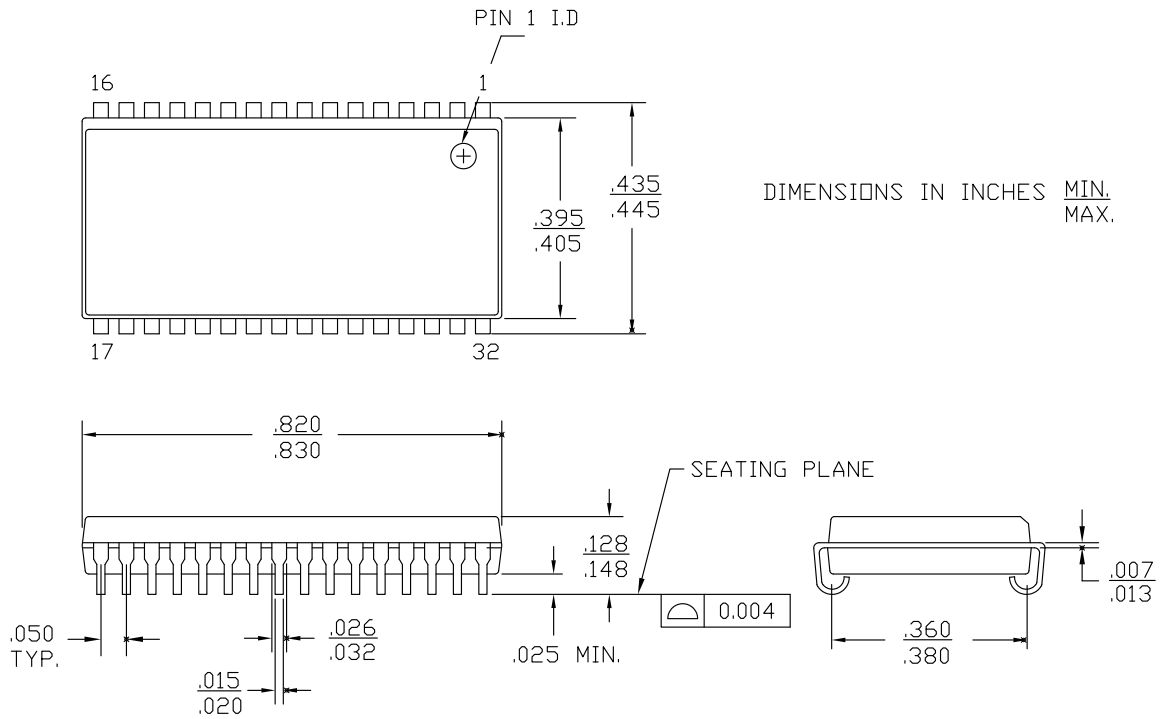


Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

Figure 9. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033

32 Lead (400 MIL) Molded SOJ V33



51-85033 *E

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1046DV33, 4-Mbit (1 M × 4) Static RAM Document Number: 38-05611				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	307613	See ECN	RKF	New data sheet
*A	397134	See ECN	R XU	<p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed -15 Speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from -0.5 to -0.3 V and $V_{CC} + 0.5 V$ to $V_{CC} + 0.3 V$</p> <p>Redefined I_{CC} values for Com'l and Ind'l temperature ranges</p> <p>I_{CC} (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12 ns speed bins respectively</p> <p>I_{CC} (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12 ns speed bins respectively</p> <p>Removed footnote on rise time and added footnote on Operation Recovery Time (t_R)</p> <p>Corrected Typo in Truth Table from (I/O₀ - I/O₇) to (I/O₀ to I/O₃)</p> <p>Changed part names from V33 to V32 in the Ordering Information Table</p> <p>Removed L-Version</p> <p>Added Lead-Free Product Information</p> <p>Shaded Ordering Information Table</p>
*B	459072	See ECN	NXR	<p>Converted from Preliminary to Final</p> <p>Removed -8 and -12 speed bins</p> <p>Removed Commercial Operating Range product information</p> <p>Removed the PIn Definition table</p> <p>Changed the Capacitance value of input pins and I/O pins from 6 pF to 8 pF</p> <p>Updated the Thermal Resistance table</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #11</p> <p>Replaced Package Name column with Package Diagram in the Ordering Information table</p>
*C	3059211	10/14/2010	PRAS	<p>Added Ordering Code Definitions.</p> <p>Updated Package Diagram.</p>
*D	3100106	12/02/2010	PRAS	<p>Added Acronyms and Units of Measure.</p> <p>Minor edits and updated in new template.</p>
*E	3432847	11/08/2011	TAVA	<p>Updated Features.</p> <p>Updated Functional Description.</p> <p>Updated DC Electrical Characteristics.</p> <p>Updated Switching Waveforms.</p> <p>Updated Package Diagram.</p>
*F	4574311	11/19/2014	TAVA	<p>Added related documentation hyperlink in page 1.</p> <p>Updated Figure 9 in Package Diagram (spec 51-85033 *D to *E).</p>

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