

DELKIN DEVICES®

SLC Commercial and Industrial PC/PCMCIA ATA Card

Engineering Specification

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General Description

PCMCIA ATA or PC Card is a high capacity storage solution for laptops and an array of industrial hosts. It's easy to store and virtually indestructible. The PC Card is roughly the dimensions of a credit card, and has a standardized 68-pin connector at one end. It's easy to use; just plug it into a PCMCIA slot in your laptop or industrial host. The PC Card's low-power consumption, small size and ruggedness make it a great storage solution.

Applications

- Industrial Computer
- Embedded Systems
- Data Acquisition
- Automotive
- Flight Systems
- Also, hundreds of other industries looking for a more robust and rugged digital storage option.
- Agriculture
- Manufacturing
- Military
- Gaming
- Telecommunications

Features

PC Card ATA specification standard 68-pin interface in a type I (3.3mm) package
3.3V / 5V single power supply operation
ISA standard Read/Write unit of 512 bytes (sector), sequential access
Maximum Density: 4 GB
Operations Modes:
 Memory mode
 I/O mode
 True IDE mode
Internal Power on Self Test (POST)
High Reliability ECC (Error Correction Code)
Data Reliability / 1 error in 10^{14} bits read
Auto Sleep Mode

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1.0 General PC/PCMCIA ATA Card Specifications

1.1 Recommended Temperature Conditions (Celsius)

Parameter	Min.	Max.
Storage Temp.	-50°	100°
SLC Industrial Operating Temp.	-40°	85°

1.2 Performance

Parameter	Value
*Data Transfer Rate	up to 16.6 Mb/sec
*Sustained Read	up to 10 Mb/sec
*Sustained Write	up to 9 Mb/sec

* Dependent on configuration and testing environment

1.3 Reliability

Parameter	Value
Program/Erase Cycle Endurance	Raw flash is rated for 60,000 P/E cycles
MTBF	>2,000,000 hours @ 0° C
Data Retention	10 Yrs

1.4 Environmental Characteristics

Parameter	Value
Shock	40g's at 11ms, MIL-STD-810, Method 516.5
Vibration	15Hz to 2000Hz, MIL-STD-810, Method 514.5
Humidity	95% R-H, MIL-STD-810, Method 507.4
Altitude	80,000 ft

1.5 Ordering Information

Capacity	SLC Industrial (-40 to 85° C) Removable/DMA Enabled	SLC Industrial (-40 to 85° C) Removable/DMA Disabled
128MB	AE12TFJHG-XX000-D	AE12TFJHG-X1000-D
256MB	AE25TFKHG-XX000-D	AE25TFKHG-X1000-D
512MB	AE51TFLHG-XX000-D	AE51TFLHG-X1000-D
1GB	AE0GTFLHG-XX000-D	AE0GTFLHG-X1000-D
2GB	AE02TFLHG-XX000-D	AE02TFLHG-X1000-D
4GB	AE04TFLHG-XX000-D	AE04TFLHG-X1000-D

1.6 CHS Parameters

Card Density	Capacity**	# Cylinders	# Heads	Sectors/Track	Total Sectors
128 MB	128,188,416	03 D2	08	20	03 D2 00
256 MB	256,327,680	04 13	0F	20	07 A3 A0
512 MB	512,386,560	04 23	0F	3F	0F 45 33
1 GB	1,025,480,752	07 C3	10	3F	1E 8F D0
2 GB	2,147,483,648	0F B2	10	3F	3D 0F E0
4 GB	4,294,967,296	1F 04	10	3F	7A 1F C0

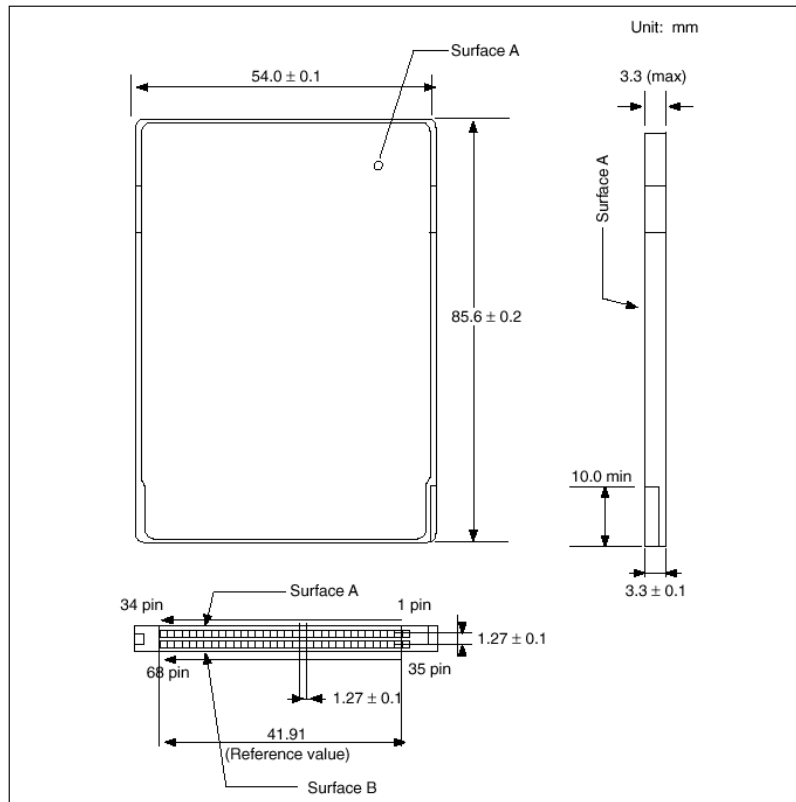
NOTE: All CIS information is shown in HEX format.

** The logical address space (including system area).

1.7 Card Dimensions

Delkin Devices Industrial and Extended Temperature cards are PC/PCMCIA type I cards.

Length:	85.6 ± 0.2 mm (3.370 ± .008 in.)
Width:	54.0 ± 0.1 mm (2.126 ± .004 in.)
Thickness Including Label Area:	3.3 mm ± 0.1 mm (.130 ± .004 in.)
Weight:	12.0 g typical



2.0 PC/PCMCIA ATA Card Interface

2.1 Card Pin Assignment

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE1	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	—	—	—	—	—	—
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	—	—	—	—	—	—
14	—	—	—	—	—	—
15	-WE	I	-WE	I	-WE	I
16	RDY/-BSY	O	-IREQ	O	INTRQ	O
17	VCC	—	VCC	—	VCC	—
18	—	—	—	—	—	—
19	—	—	—	—	—	—
20	—	—	—	—	—	—
21	—	—	—	—	—	—
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	-IOIS16	O	-IOIS16	O
34	GND	—	GND	—	GND	—
35	GND	—	GND	—	GND	—
36	-CD1	O	-CD1	O	-CD1	O

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I/O	D15	I/O	D15	I/O
42	-CE2	I	-CE2	I	-CE2	I
43	-VS1	O	-VS1	O	-VS1	O
44	-IORD	I	-IORD	I	-IORD	I
45	-IOWR	I	-IOWR	I	-IOWR	I
46	—	—	—	—	—	—
47	—	—	—	—	—	—
48	—	—	—	—	—	—
49	—	—	—	—	—	—
50	—	—	—	—	—	—
51	VCC	—	VCC	—	VCC	—
52	—	—	—	—	—	—
53	—	—	—	—	—	—
54	—	—	—	—	—	—
55	—	—	—	—	—	—
56	-CSEL	I	-CSEL	I	-CSEL	I
57	-VS2	O	-VS2	O	-VS2	O
58	RESET	I	RESET	I	-RESET	I
59	-WAIT	O	-WAIT	O	IORDY	O
60	-INPACK	O	-INPACK	O	-INPACK	O
61	-REG	I	-REG	I	-REG	I
62	BVD2	I/O	-SPKR	I/O	-DASP	I/O
63	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	I/O	D10	I/O	D10	I/O
67	-CD2	O	-CD2	O	-CD2	O
68	GND	—	GND	—	GND	—

2.2 Card Pin Explanation

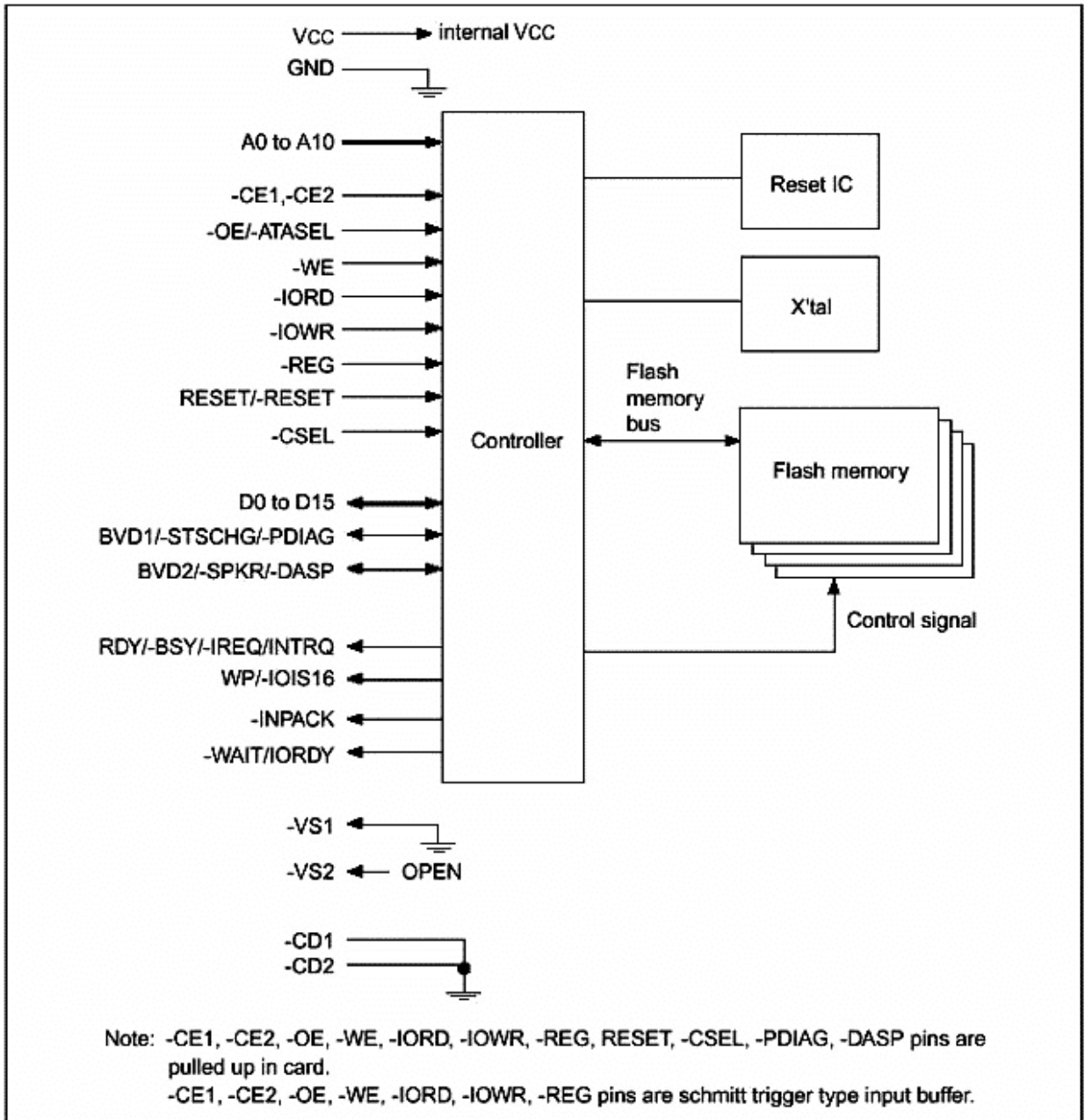
Signal name	Direction	Pin No.	Description
A[10..0] (PC Card Memory mode)	1	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	A[10..0], Address bus. A10 = MSB
A[10..0] (PC Card I/O mode)			
A[2..0] (True IDE mode)			
BVD1 (PC Card Memory mode)	I/O	63	Not supported. Output = 1.
-STSCHG (PC Card I/O mode)			-STSCHG, used to notify the host of changes in the RDY/-BSY and write protect status.
-PDIAG (True IDE mode)			-PDIAG, Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory mode)	I/O	62	Not supported. Output = 1.
-SPKR (PC Card I/O mode)			Not supported. Output = 1.
-DASP (True IDE mode)			-DASP, Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory mode)	O	36, 67	-CD1 and -CD2, card detection signals. -CD1 and -CD2 are connected to ground.
-CD1, -CD2 (PC Card I/O mode)			
-CD1, -CD2 (True IDE mode)			
-CE1, -CE2 (PC Card Memory mode) Card Enable	I	7, 42	-CE1 and -CE2, active low card selects. Byte/Word/Odd byte mode are defined by combination of -CE1, -CE2 and A0.
-CE1, -CE2 (PC Card I/O mode) Card Enable			
-CE1, -CE2 (True IDE mode)			-CE2 selects the Alternate Status Register and the Device Control Register -CE1 selects the task file registers.

Signal name	Direction	Pin No.	Description
-CSEL (PC Card Memory mode)	I	56	This signal is not used.
-CSEL (PC Card I/O mode)			
-CSEL (True IDE mode)			-CSEL, configures the device as a Master or Slave. When grounded, the device is configured as a Master. When open, the device is configured as a Slave.
D[15..0] (PC Card Memory mode)	I/O	41, 40, 39, 38, 37, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	D[15..0]. Bi-Directional data lines.
D[15..0] (PC Card I/O mode)			16bit: D15 = MSB 8bit: D15 = MSB (odd byte), D7 = MSB (even byte)
D[15..0] (True IDE mode)			
GND (PC Card Memory mode)	—	1, 34, 35, 68	Ground
GND (PC Card I/O mode)			
GND (True IDE mode)			
-INPACK (PC Card Memory mode)	O	60	This signal is not used and should not be connected at the host.
-INPACK (PC Card I/O mode) Input Acknowledge			-INPACK, asserted low when the card is selected and responding to an I/O read cycle at the address that is on the address bus while -CE and -IORD are low. -INPACK is also used for the input data buffer control.
-INPACK (True IDE mode)			This signal is not used and should not be connected at the host.
-IORD (PC Card Memory mode)	I	44	This signal is not used.
-IORD (PC Card I/O mode)			-IORD is used to control of read the I/O task file area. This signal also gates I/O data onto the bus.
-IORD (True IDE mode)			

Signal name	Direction	Pin No.	Description
-IOWR (PC Card Memory mode)	I	45	This signal is not used.
-IOWR (PC Card I/O mode)			-IOWR, control signal used to write to the Task File Register. This signal also clocks I/O data in of the card.
-IOWR (True IDE mode)			(Clocking occurs on the rising edge)
-OE (PC Card Memory mode)	I	9	-OE, controls the reading of Attribute and Task File data.
-OE (PC Card I/O mode)			-OE, controls the reading of Attribute data.
-ATASEL (True IDE mode)			-OE, grounded by the host.
RDY/-BSY (PC Card Memory mode)	O	16	RDY/-BSY, asserted low while the card is busy.
-IREQ (PC Card I/O mode)			-IREQ, Active low Interrupt Request.
INTRQ (True IDE mode)			INTRQ, active high Interrupt Request.
-REG (PC Card Memory mode)	I	61	-REG, distinguishes between task file and attribute memory accesses. Hi = Task file Lo = Attribute
-REG (PC Card I/O mode)			This input signal is not used and should be connected to VCC.
-REG (True IDE mode)			
RESET (PC Card Memory mode)	I	58	RESET, active high RESET pin.
RESET (PC Card I/O mode)			-RESET active low -RESET pin.
-RESET (True IDE mode)			

Signal name	Direction	Pin No.	Description
VCC (PC Card Memory mode)	—	17, 51	+5 V, +3.3 V power.
VCC (PC Card I/O mode)			
VCC (True IDE mode)			
-VS1, -VS2 (PC Card Memory mode)	O	43, 57	-VS1, -VS2, identifies VCC requirements.
-VS1, -VS2 (PC Card I/O mode)			-VS1 = GND
-VS1, -VS2 (True IDE mode)			-VS2 = Reserved by PCMCIA
-WAIT (PC Card Memory mode)	O	59	-WAIT, signals the host to delay completion of a memory or I/O cycle in progress.
-WAIT (PC Card I/O mode)			
IORDY (True IDE mode)			IORDY, I/O ready signal.
-WE (PC Card Memory mode)	I	15	-WE, controls the writing of data to the attribute or task file areas.
-WE (PC Card I/O mode)			-WE, controls the writing of data to the attribute memory area.
-WE (True IDE mode)			This input signal is not used.
WP (PC Card Memory mode) Write Protect	O	33	This input signal is not used.
-IOIS16 (PC Card I/O mode)			-IOIS16, asserted low when task file registers are accessed in 16-bit mode.
-IOIS16 (True IDE mode)			-IOIS16, asserted low when the device is expecting a word data transfer cycle

2.3 Card Block Diagram



2.4 Card Function Explanation

Register construction

- Attribute region
 - Configuration register
 - Configuration Option register
 - Configuration and Status register
 - Pin Replacement register
 - Socket and Copy register
 - CIS (Card Information Structure)
- Task File region
 - Data register
 - Error register
 - Feature register
 - Sector Count register
 - Sector Number register
 - Cylinder Low register
 - Cylinder High register
 - Drive Head register
 - Status register
 - Alternate Status register
 - Command register
 - Device Control register
 - Drive Address register

3.0 Electrical Specification

3.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
All input/output voltages	Vin, Vout	-0.3 to Vcc + 0.3	V	1
Vcc voltage	Vcc	-0.3 to +6.5	V	

Note: 1. Vin, Vout min = -2.0 V for pulse width \leq 20 ns.

3.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating temperature	Ta	0	25	85	°C	
Vcc voltage	Vcc	4.75	5.0	5.25	V	
		3	3.3	3.6	V	

3.3 Capacitance (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	35	pF	Vin = 0 V
Output capacitance	Cout	—	—	35	pF	Vout = 0 V

3.4 System Performance

Item	Performance
Start up times (Reset to ready)	100 ms (max)
Start up times (Sleep to idle)	2 ms (max)
Controller overhead (Command to DRQ)	2 ms (max)
Data transfer cycle end to ready (Sector write)	2 ms (typ)

3.5 DC Characteristics-1 (Ta = 0 to +85°C, VCC = 5.0 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input leakage current	ILI	—	—	±1	μA	Vin = GND to VCC	1
Input voltage (CMOS)	VIL	—	—	0.8	V		
	VIH	4.0	—	—	V		
Input voltage (schmitt trigger)	VIL	—	2.0	—	V		
	VIH	—	2.8	—	V		
Output voltage	VOL	—	—	0.4	V	IOL = 8 mA	
	VOH	VCC – 0.8	—	—	V	IOH = –8 mA	

Note: 1. Except pulled up input pin.

3.6 DC Characteristics-2 (Ta = 0 to +85°C, VCC = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input leakage current	ILI	—	—	±1	A	Vin = GND to VCC	1
Input voltage (CMOS)	VIL	—	—	0.6	V		
	VIH	2.4	—	—	V		
Input voltage (schmitt trigger)	VIL	—	1.0	—	V		
	VIH	—	1.8	—	V		
Output voltage	VOL	—	—	0.4	V	IOL = 8 mA	
	VOH	VCC – 0.8	—	—	V	IOH = –8 mA	

Note: 1. Except pulled up input pin.

3.7 DC Characteristics-3 ($T_a = 0$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$)

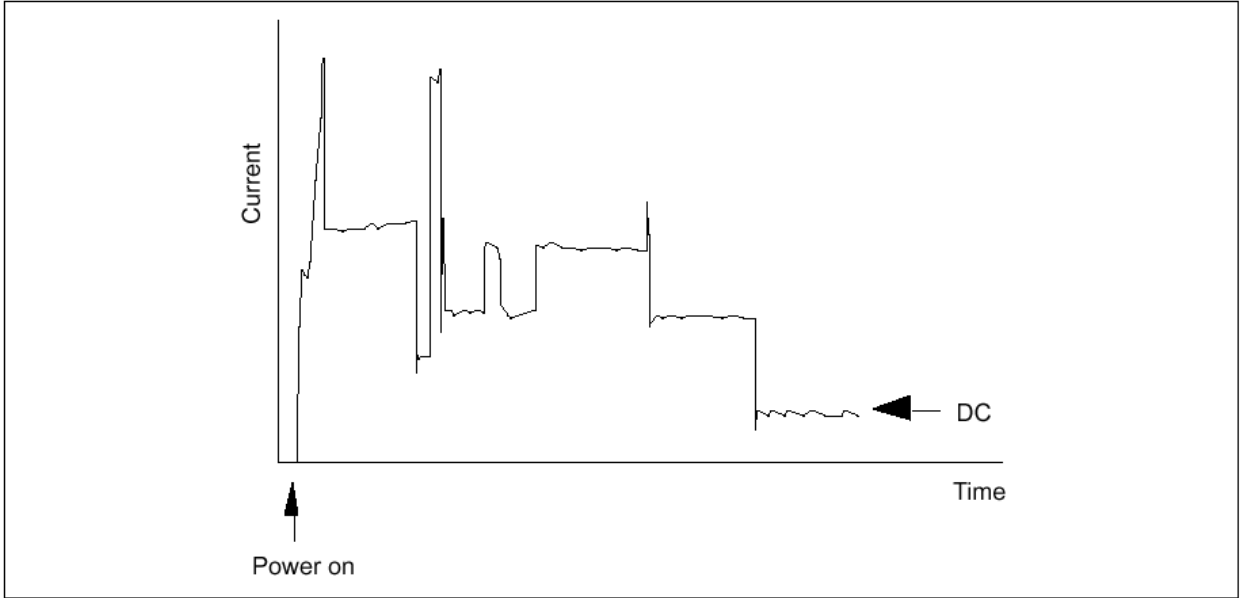
Parameter	Symbol	$\leq 128\text{MB}$		$> 128\text{MB}$		Unit	Test conditions
		Typ	Max	Typ	Max		
Sleep/standby = current	ISP1	0.5		1.0	0.7	1.5 mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) (In Memory card mode and I/O card mode)
Sector read = current	ICCR (DC)	40	75	40	75	mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) during sector read transfer
	ICCR (Peak)	80	120	80	120		
Sector write = current	ICCW (DC)	45	75	45	75	mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) during sector write transfer
	ICCW (Peak)	80	120	80	120		

3.8 DC Characteristics-4 ($T_a = 0$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 5\%$)

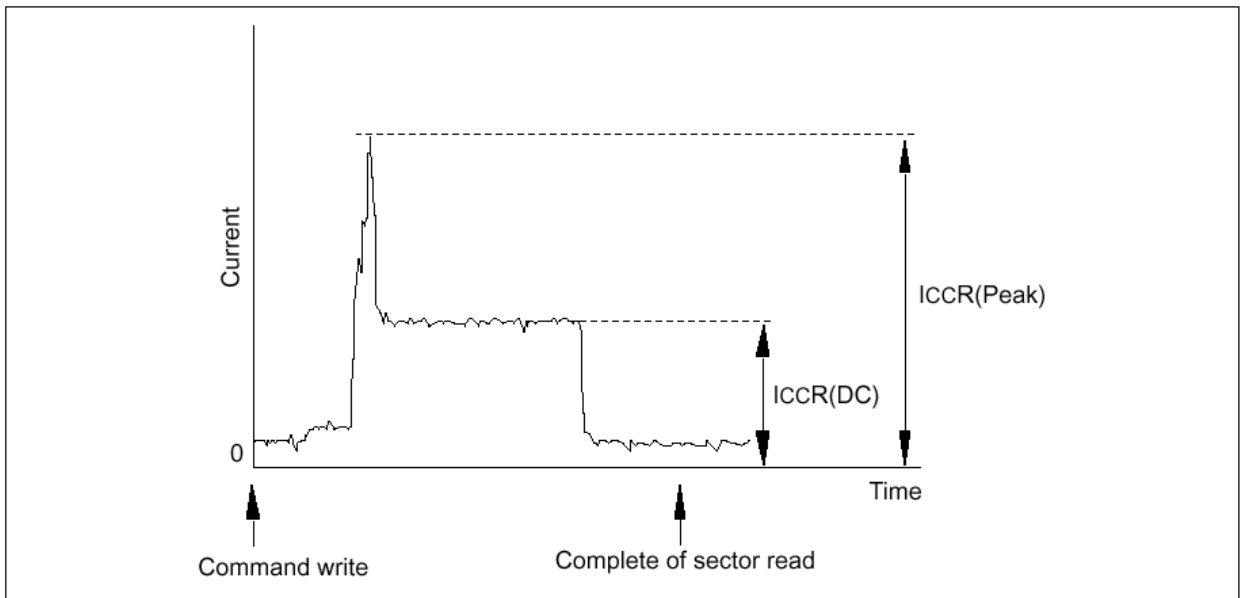
Parameter	Symbol	$\leq 128\text{MB}$		$> 128\text{MB}$		Unit	Test conditions
		Typ	Max	Typ	Max		
Sleep/standby current	ISP1	0.3	1.0	0.4	1.5	mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) (In Memory card mode and I/O card mode)
Sector read current	ICCR (DC)	25	50	25	50		
	ICCR (Peak)	50	80	50	80	mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) during sector read transfer
Sector write current	ICCW (DC)	25	50	25	50		
	ICCW (Peak)	50	100	50	100	mA	CMOS level (control signal = $V_{CC} - 0.2\text{ V}$) during sector write transfer

3.9 DC Current Waveform (VCC = 5 V, Ta = 25°C)

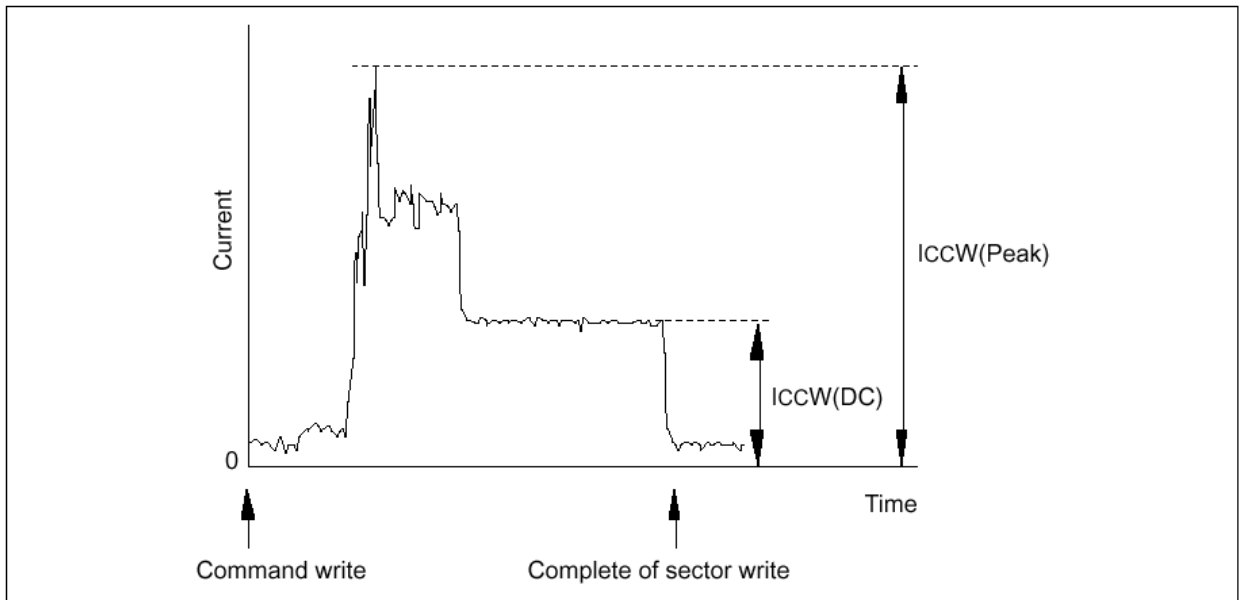
3.9.1 Power on Operation (Reference only)



3.9.2 Sector Read (Reference only)



3.9.3 Sector Write (Reference only)

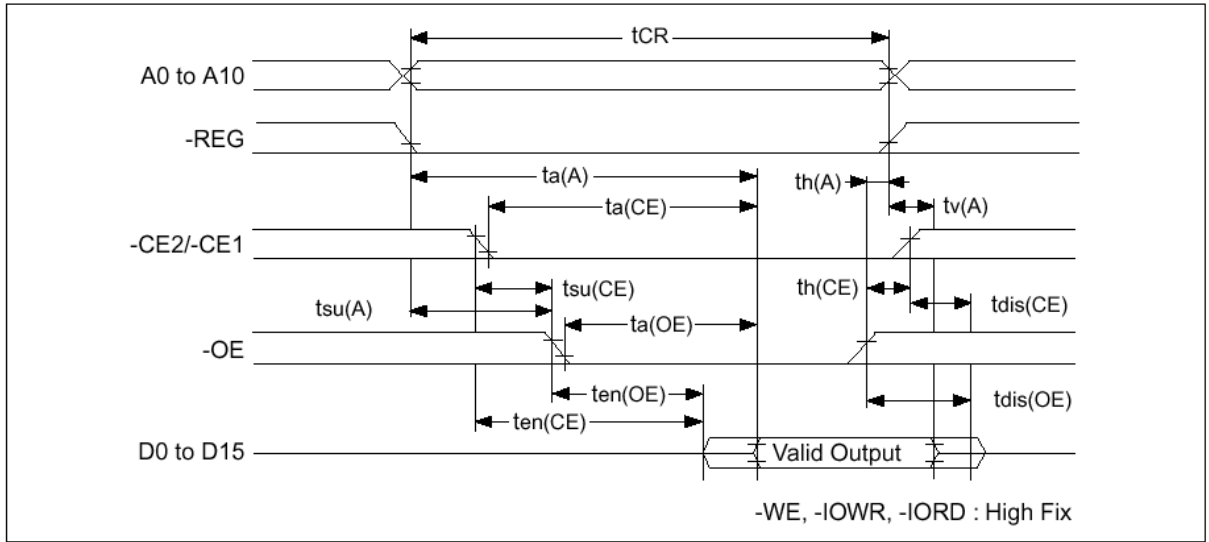


3.10 AC Characteristics ($T_a = 0$ to $+85^\circ\text{C}$, $V_{CC} = 5 \pm 10\%$, $V_{CC} = 3.3 \text{ V} \pm 5\%$)

3.10.1 Attribute Memory Read AC Characteristics

Parameter	Symbol	250 ns			Unit
		Min	Typ	Max	
Read cycle time	tCR	250	—	—	ns
Address access time	ta(A)	—	—	250	ns
-CE access time	ta(CE)	—	—	250	ns
-OE access time	ta(OE)	—	—	125	ns
Output disable time (-CE)	t _{dis} (CE)	—	—	100	ns
Output disable time (-OE)	t _{dis} (OE)	—	—	100	ns
Output enable time (-CE)	t _{en} (CE)	5	—	—	ns
Output enable time (-OE)	t _{en} (OE)	5	—	—	ns
Data valid time (A)	t _v (A)	0	—	—	ns
Address setup time	t _{su} (A)	30	—	—	ns
Address hold time	t _h (A)	20	—	—	ns
-CE setup time	t _{su} (CE)	0	—	—	ns
-CE hold time	t _h (CE)	20	—	—	ns

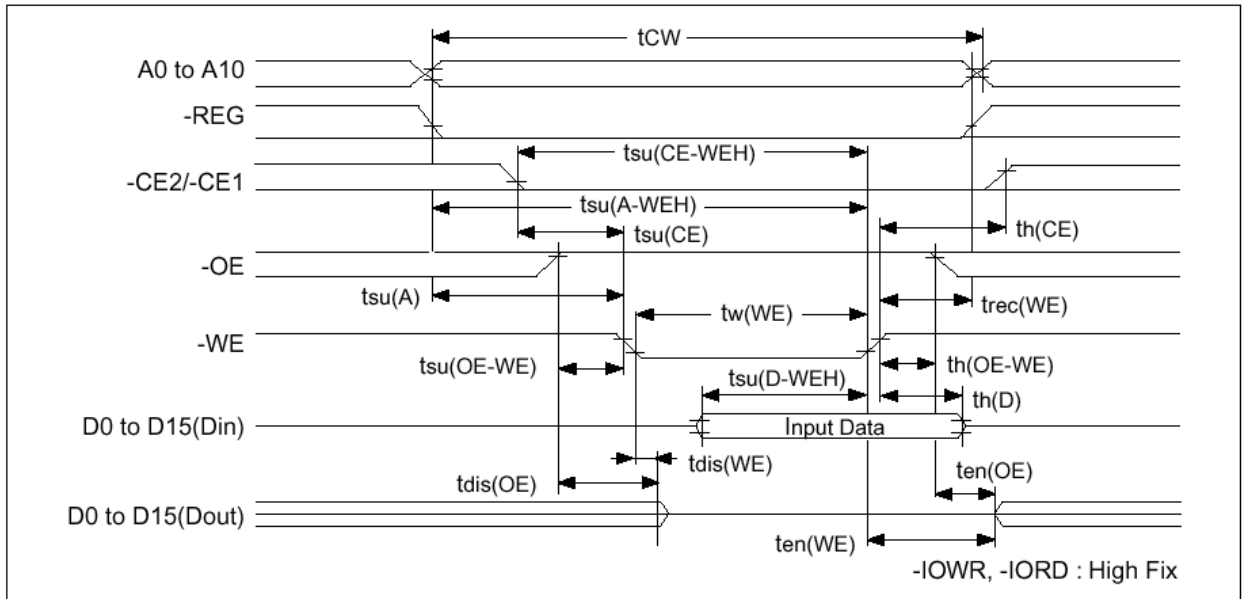
3.10.2 Attribute Memory Read Timing



3.10.3 Attribute Memory Write AC Characteristics

Parameter	Symbol	250 ns			Unit
		Min	Typ	Max	
Write cycle time	t_{CW}	250	—	—	ns
Write pulse time	$t_{w(WE)}$	150	—	—	ns
Address setup time	$t_{su(A)}$	30	—	—	ns
Address setup time (-WE)	$t_{su(A-WEH)}$	180	—	—	ns
-CE setup time (-WE)	$t_{su(CE-WEH)}$	180	—	—	ns
Data setup time (-WE)	$t_{su(D-WEH)}$	80	—	—	ns
Data hold time	$t_{h(D)}$	30	—	—	ns
Write recover time	$t_{rec(WE)}$	30	—	—	ns
Output disable time (-WE)	$t_{dis(WE)}$	—	—	100	ns
Output disable time (-OE)	$t_{dis(OE)}$	—	—	100	ns
Output enable time (-WE)	$t_{en(WE)}$	5	—	—	ns
Output enable time (-OE)	$t_{en(OE)}$	5	—	—	ns
Output enable setup time (-WE)	$t_{su(OE-WE)}$	10	—	—	ns
Output enable hold time (-WE)	$t_{h(OE-WE)}$	10	—	—	ns
-CE setup time	$t_{su(CE)}$	0	—	—	ns
-CE hold time	$t_{h(CE)}$	20	—	—	ns

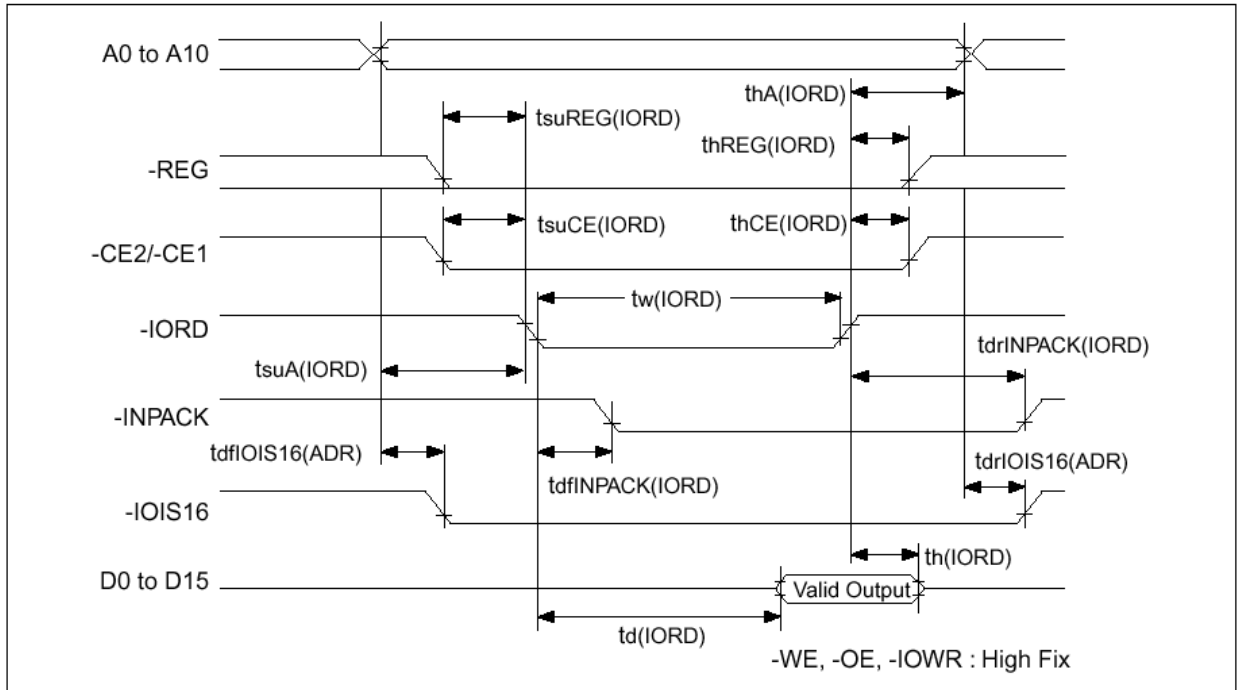
3.10.4 Attribute Memory Write Timing



3.10.5 I/O Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after -IORD	td(IORD)	—	—	100	ns
Data hold following -IORD	th(IORD)	0	—	—	ns
-IORD pulse width	tw(IORD)	165	—	—	ns
Address setup before -IORD	tsuA(IORD)	70	—	—	ns
Address hold following -IORD	thA(IORD)	20	—	—	ns
-CE setup before -IORD	tsuCE(IORD)	5	—	—	ns
-CE hold following -IORD	thCE(IORD)	20	—	—	ns
-REG setup before -IORD	tsuREG(IORD)	5	—	—	ns
-REG hold following -IORD	thREG(IORD)	0	—	—	ns
-INPACK delay falling from -IORD	tdfINPACK(IORD)	0	—	45	ns
-INPACK delay rising from -IORD	tdrINPACK(IORD)	—	—	45	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

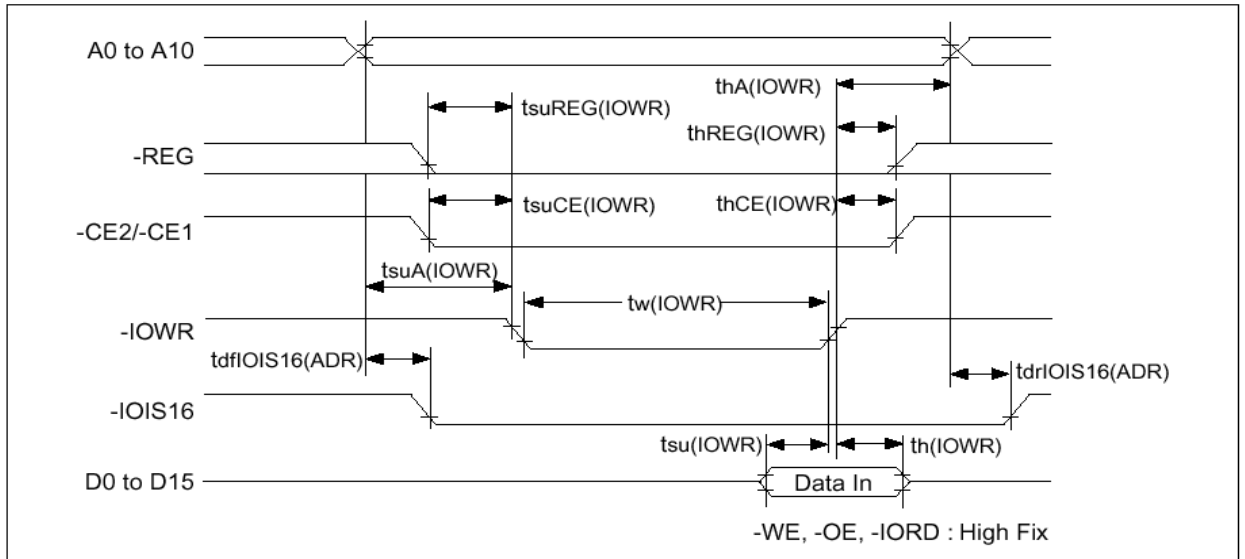
3.10.6 I/O Access Read Timing



3.10.7 I/O Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before $-IOWR$	$tsu(IOWR)$	60	—	—	ns
Data hold following $-IOWR$	$th(IOWR)$	30	—	—	ns
$-IOWR$ pulse width	$tw(IOWR)$	165	—	—	ns
Address setup before $-IOWR$	$tsuA(IOWR)$	70	—	—	ns
Address hold following $-IOWR$	$thA(IOWR)$	20	—	—	ns
$-CE$ setup before $-IOWR$	$tsuCE(IOWR)$	5	—	—	ns
$-CE$ hold following $-IOWR$	$thCE(IOWR)$	20	—	—	ns
$-REG$ setup before $-IOWR$	$tsuREG(IOWR)$	5	—	—	ns
$-REG$ hold following $-IOWR$	$thREG(IOWR)$	0	—	—	ns
$-IOIS16$ delay falling from address	$tdfIOIS16(ADR)$	—	—	35	ns
$-IOIS16$ delay rising from address	$tdrIOIS16(ADR)$	—	—	35	ns

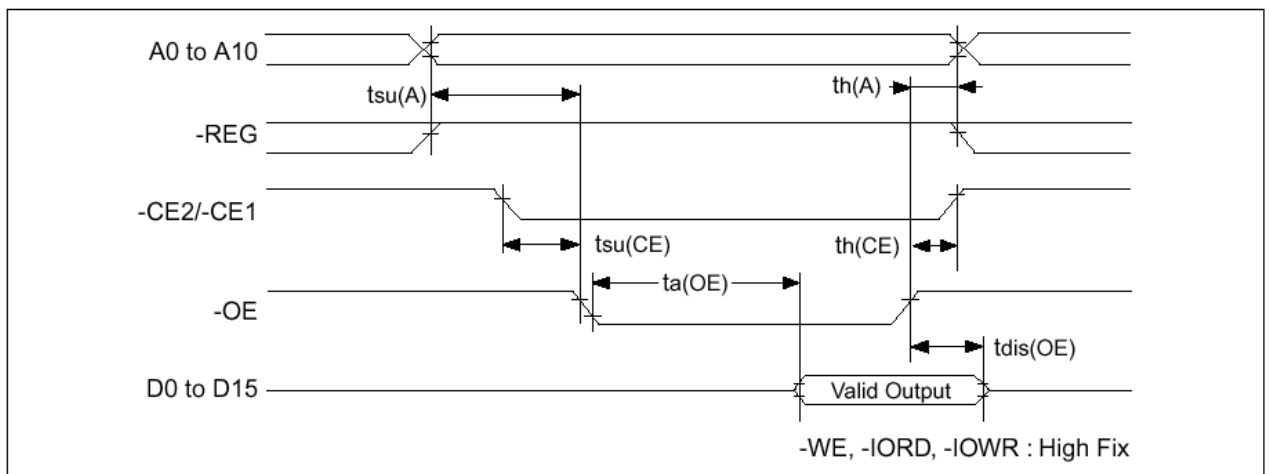
3.10.8 I/O Access Write Timing



3.10.9 Common Memory Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
-OE access time	$t_{a(OE)}$	—	—	125	ns
Output disable time (-OE)	$t_{dis(OE)}$	—	—	100	ns
Address setup time	$t_{su(A)}$	30	—	—	ns
Address hold time	$t_{h(A)}$	20	—	—	ns
-CE setup time	$t_{su(CE)}$	0	—	—	ns
-CE hold time	$t_{h(CE)}$	20	—	—	ns

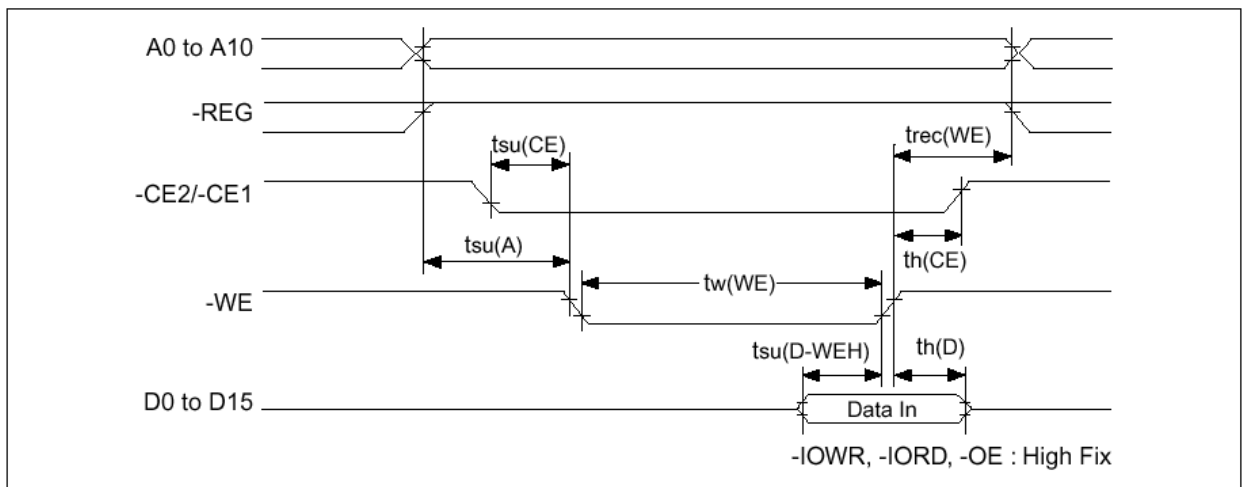
3.10.10 Common Access Read Timing



3.10.11 Common Memory Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
-CE hold following -WE	th(CE)	20	—	—	ns

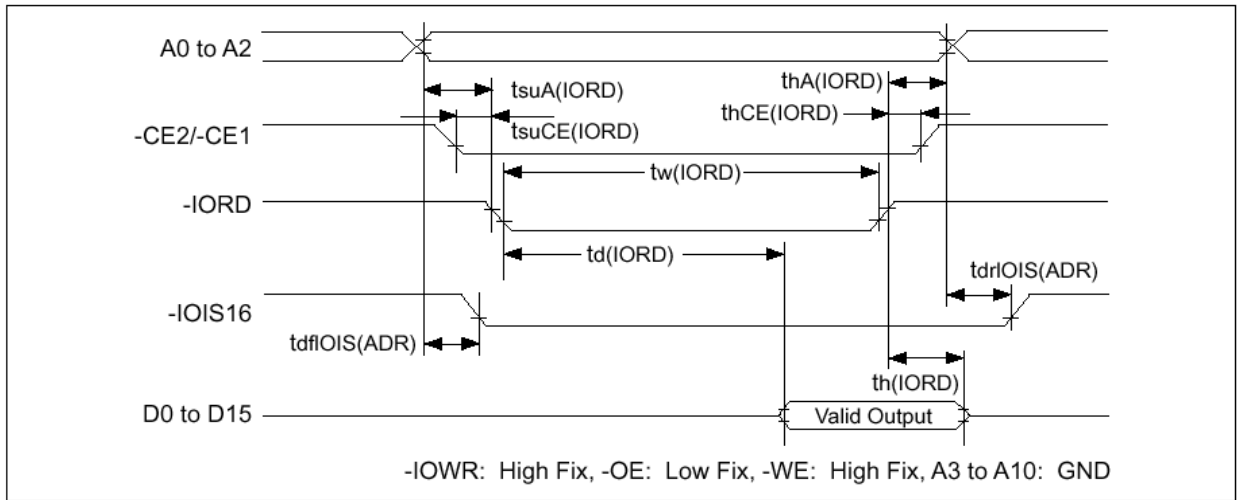
3.10.12 Common Access Write Timing



3.10.13 True IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after IORD	td(IORD)	—	—	100	ns
Data hold following IORD	th(IORD)	0	—	—	ns
IORD width time	tw(IORD)	165	—	—	ns
Address setup before IORD	tsuA(IORD)	70	—	—	ns
Address hold following IORD	thA(IORD)	20	—	—	ns
CE setup before IORD	tsuCE(IORD)	5	—	—	ns
CE hold following IORD	thCE(IORD)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

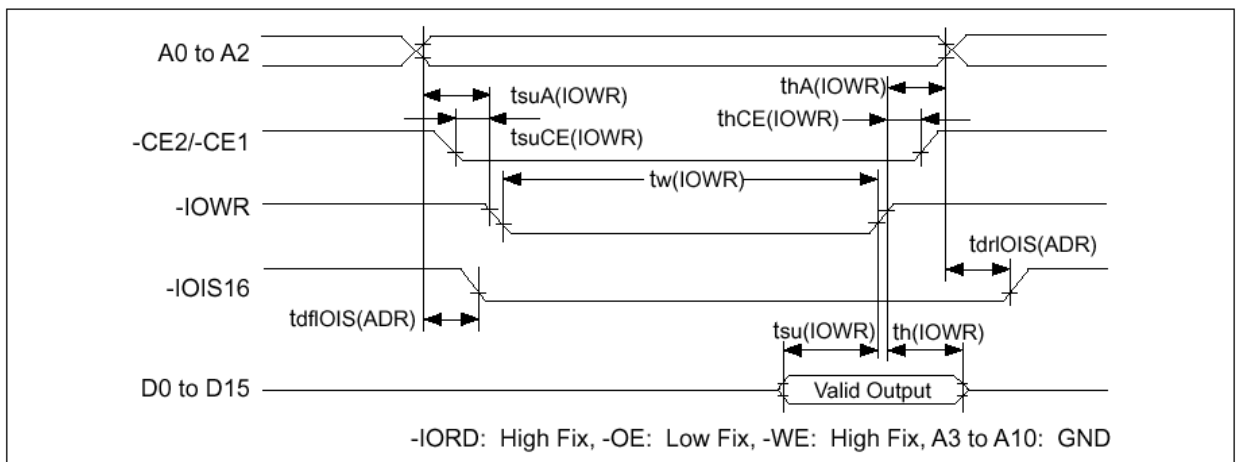
3.10.14 True IDE Mode Access Read Timing



3.10.15 True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	60	—	—	ns
Data hold following IOWR	th(IOWR)	30	—	—	ns
IORD width time	tw(IOWR)	165	—	—	ns
Address setup before IOWR	tsuA(IOWR)	70	—	—	ns
Address hold following IOWR	thA(IOWR)	20	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	5	—	—	ns
CE hold following IOWR	thCE(IOWR)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

3.10.16 True IDE Mode Access Write Timing

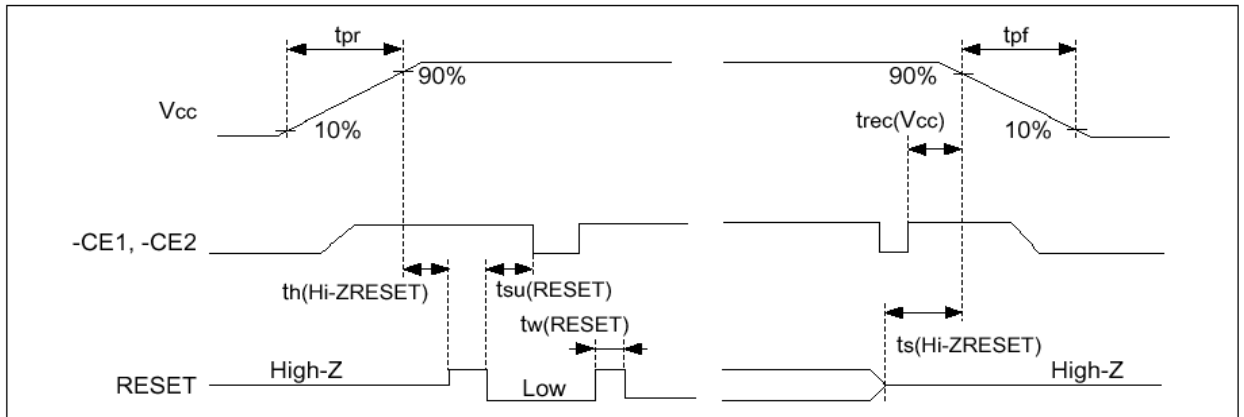


3.11 Reset Characteristics (Memory Card Mode or I/O Card Mode only)

3.11.1 Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	μs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	μs	
	th(Hi-ZRESET)	1	—	—	ms	
	ts(Hi-ZRESET)	0	—	—	ms	

3.11.2 Hard Reset Timing

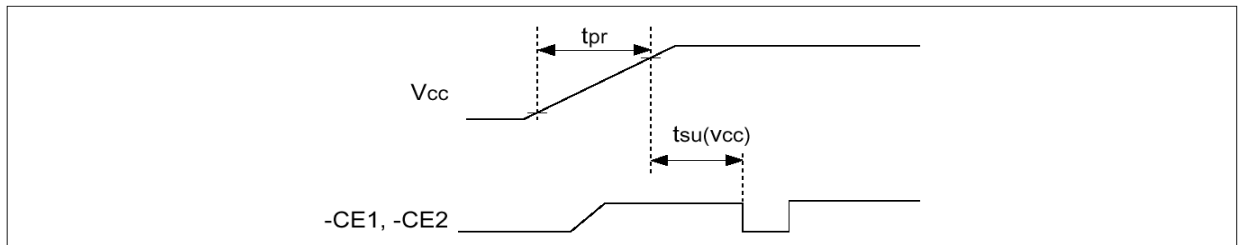


3.11.3 Power on Reset Characteristics

Card status is reset automatically when VCC voltage goes over about 2.3 V.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
-CE setup time	tsu(VCC)	100	—	—	ms	
VCC rising up time	tpr	0.1	—	100	ms	

3.11.4 Power on Reset Timing



Attention for Card Use

- In the reset or power off, all register information is cleared.
- Card status is cleared automatically when VCC voltage turns below about 2.5V.
- Notice: the card insertion/removal should not be executed while host is active if the card is used in True IDE mode.
- After a hard reset, soft reset power on reset, or ATA reset, if a command applied the card while +RDY/-BSY pin is "low", the Flash card will ignore the command.
- Notice that while card removal should be executed after card internal operations are completed.
- Before card insertion VCC cannot be supplied to the card until confirmation that -CD1, -CD2 pins are inserted.
- -OE must be kept at VCC during a power on reset in memory card mode and I/O card mode. -OE must be kept at the GND in True IDE mode.

4.0 Host access specifications**4.1 Attribute access specifications**

When CIS or Configuration registers are accessed, read and write operations are executed under the condition of -REG = "L" as follows: (the region may be accessed by Byte/Word/Odd-byte modes).

4.1.1 Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access (16-bit)	L	L	L	x	L	H	invalid	even byte
Odd byte access (8-bit)	L	L	H	x	L	H	invalid	High-Z

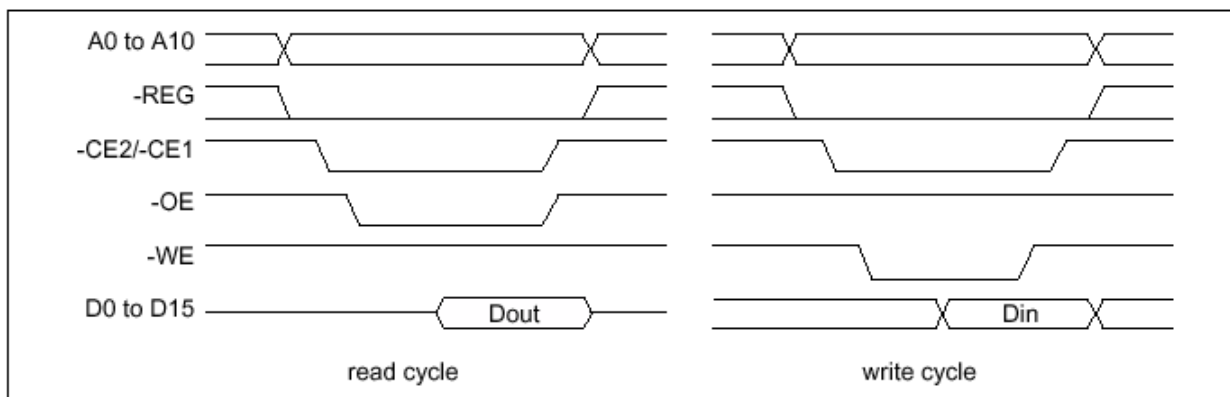
Note: x: L or H

4.1.2 Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	don't care	don't care
Byte access (8-bit)	L	H	L	L	H	L	don't care	even byte
	L	H	L	H	H	L	don't care	don't care
Word access (16-bit)	L	L	L	x	H	L	don't care	even byte
Odd byte access (8-bit)	L	L	H	x	H	L	don't care	don't care

Note: x: L or H

4.1.3 Attribute Access Timing Example



4.2 Task File register access specifications

The Task is accessed via one of two modes, I/O mapped, and Memory mapped. Each Task File register read and write operation is executed under the condition as follows: (the area may be accessed in Byte/Word/Odd Byte mode).

4.2.1 I/O address map

4.2.1.1 Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	High-Z	High-Z
Byte access (8-bit) byte	L	H	L	L	L	H	H	H	High-Z	even
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16-bit) byte	L	L	L	x	L	H	H	H	odd byte	even
Odd byte access (8-bit)	L	L	H	x	L	H	H	H	odd byte	High-Z

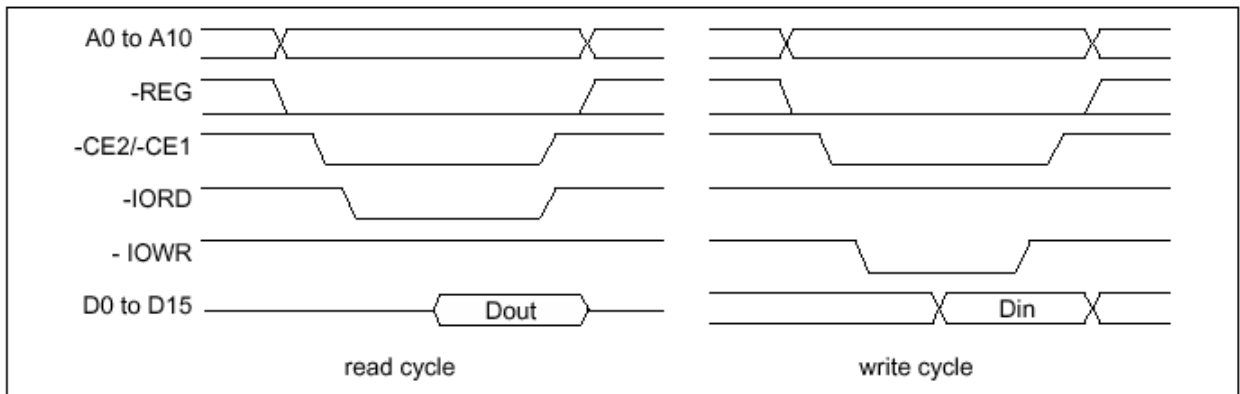
Note: x: L or H

4.2.1.2 Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode care	x	H	H	x	x	x	x	x	don't care	don't care
Byte access (8-bit) byte	L	H	L	L	H	L	H	H	don't care	even
	L	H	L	H	H	L	H	H	don't care	odd byte
Word access (16-bit) byte	L	L	L	x	H	L	H	H	odd byte	even
Odd byte access (8-bit)	L	L	H	x	H	L	H	H	odd byte	don't care

Note: x: L or H

4.2.1.3 Task File Register Access Timing Example (1)



4.2.2 I/O address map

4.2.2.1 Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	x	H	H	x	x	x	x	x	High-Z	High-Z
Byte access (8-bit) byte	H	H	L	L	L	H	H	H	High-Z	even
	H	H	L	H	L	H	H	H	High-Z	odd
Word access (16-bit) byte	H	L	L	x	L	H	H	H	odd byte	even
Odd byte access (8-bit)	H	L	H	x	L	H	H	H	odd byte	High-Z

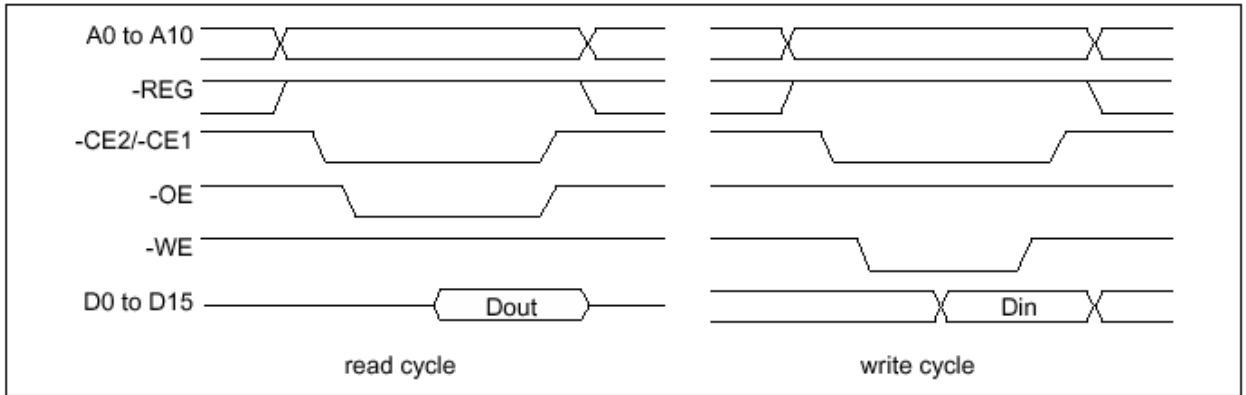
Note: x: L or H

4.2.2.2 Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode care	x	H	H	x	x	x	x	x	don't care	don't care
Byte access (8-bit) byte	H	H	L	L	H	L	H	H	don't care	even
	H	H	L	H	H	L	H	H	don't care	odd
Word access (16-bit) byte	H	L	L	x	H	L	H	H	odd byte	even
Odd byte access (8-bit) care	H	L	H	x	H	L	H	H	odd byte	don't care

Note: x: L or H

4.2.2.3 Task File Register Access Timing Example (2)



4.3 True IDE Mode

The card may be configured in a True IDE mode of operation. This card is configured in True IDE mode when the -OE input signal is asserted GND by the host. In True IDE mode Attribute Registers are not accessible to the host, only I/O operations to the task file and data register are allowed. If the card is configured during a power on sequence, data registers are accessed in word (16-bit) mode. The card permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

4.3.1 True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	L	L	x	x	x	High-Z	High-Z
Data register access	H	H	x	x	x	High-Z	High-Z
Invalid mode	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

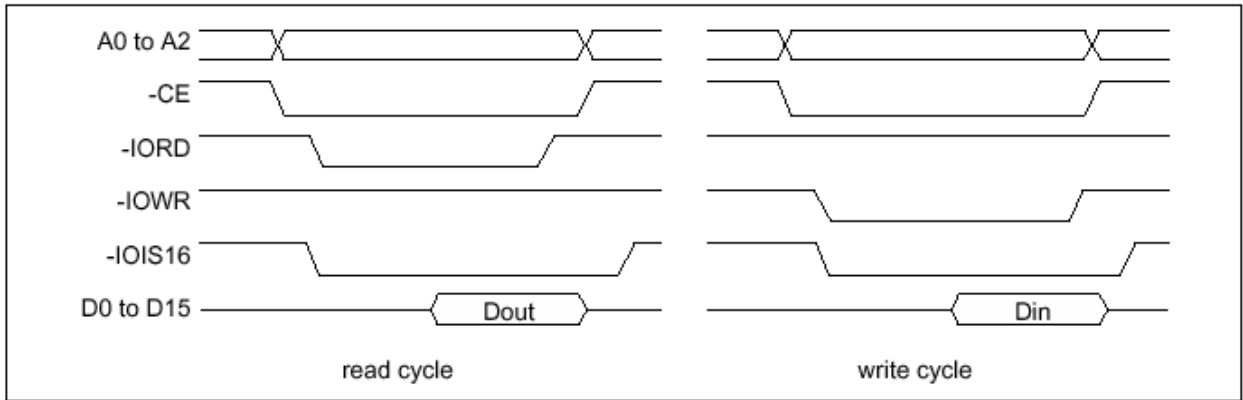
Note: x: L or H

4.3.2 True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode care	L	L	x	x	x	don't care	don't
Standby mode care	H	H	x	x	x	don't care	don't
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: x: L or H

4.3.3 True IDE Mode I/O Access Timing Example



5.0 Software Interface

5.1 Configuration register specifications

The card has four Configuration registers for the purpose of the configuration and observation of the card. These registers may be used in memory card and I/O card mode. In True IDE mode, these registers are inaccessible.

5.1.1 Configuration Option register (Address 200H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevIREQ	INDEX					

Note: initial value: 00H

Name	R/W	Function
SRESET	R/W	Setting this bit to '1', places the card in the reset state (Card Hard Reset). This (HOST->) operation is equal to a Hard Reset, except this bit is not cleared. Then this bit is set to '0', this places the card in the reset state of a Hard Reset (This bit is set to "0" by Hard Reset).
LevIREQ	R/W	This bit is set to '0' when pulse mode interrupt is selected, and '1' when level mode (HOST->) interrupt is selected.
INDEX	R/W	This bit is used to select the operating mode of the card. (HOST->) After Power on, Card Hard Reset and Soft Reset, these bits are "000000" for the purpose of Memory card recognition.

INDEX bit assignment

INDEX bit	5	4	3	2	1	0	Card mode Task	File register address	Mapping mode
	0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
	0	0	0	0	0	1	I/O card	xx0H to xxFH	contiguous I/O mapped
	0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	primary I/O mapped
	0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	secondary I/O mapped

5.1.2 Configuration and Status register (Address 202H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value: 00H

Name	R/W	Function
CHGED	R	This bit indicates that the CRDY/-BSY bit in the Pin Replacement register is set to "1". (CARD->) When the CHGED bit is set to "1", -STSCHG pin is held "L".
SIGCHG	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal. (HOST->) When the card is configured to I/O card interface and this bit is set to "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8	R/W	The host sets this field to "1" when it can provide I/O cycles on an 8 bit data bus (D7 to D0).
PWD	R/W	When this bit is set to "1", the card enters sleep mode (Power Down mode). When this bit is reset to "0", the card transfers to idle mode (active mode). RRDY/-BSY in the Pin Replacement Register becomes BUSY when this bit is changed.
RRDY/-BSY		BSY will not become Ready until the power state requested has been entered.
This		card automatically powers down when it is idle, and powers up when it receives a command.
INTR	R	This bit indicates the internal state of the interrupt request. The bit state is available (CARD->) whether I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a 0.

5.1.3 Pin Replacement register (Address 204H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

Note: initial value: 0CH

Name	R/W	Function
CRDY/-BSY	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be (HOST->) written to by the host.
RRDY/-BSY	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for (HOST->) CRDY/-BSY bit masking.

4. Socket and Copy register (Address 206H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

Note: initial value: 00H

Name	R/W	Function
------	-----	----------

DRV#	R/W	This field is used for the configuration of plural cards. When the host configures (HOST->) plural cards, the card's copy number is written in this field.
------	-----	--

5.2 Task File register specification

These registers are used to read and write data to the card. The decoded addresses are shown as follows.

5.2.1 Memory map (INDEX = 0)

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE = L	-WE = L
1	0	X	0	0	0	0	0H	Data register	Data register
1	0	X	0	0	0	1	1H	Error register	Feature register
1	0	X	0	0	1	0	2H	Sector count register	Sector count register
1	0	X	0	0	1	1	3H	Sector number register	Sector number register
1	0	X	0	1	0	0	4H	Cylinder low register	Cylinder low register
1	0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	X	0	1	1	0	6H	Drive head register	Drive head register
1	0	X	0	1	1	1	7H	Status register	Command register
1	0	X	1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0	X	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0	X	1	1	0	1	DH	Dup. error register	Dup. feature register
1	0	X	1	1	1	0	EH	Alt. status register	Device control register
1	0	X	1	1	1	1	FH	Drive address register	Reserved
1	1	X	X	X	X	0	8H	Even data register	Even data register
1	1	X	X	X	X	1	9H	Odd data register	Odd data register

5.2.2 Contiguous I/O map (INDEX = 1)

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD = L	-IOWR = L
0	X	0	0	0	0	0H	Data register	Data register
0	X	0	0	0	1	1H	Error register	Feature register
0	X	0	0	1	0	2H	Sector count register	Sector count register
0	X	0	0	1	1	3H	Sector number register	Sector number register
0	X	0	1	0	0	4H	Cylinder low register	Cylinder low register
0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	X	0	1	1	0	6H	Drive head register	Drive head register
0	X	0	1	1	1	7H	Status register	Command register
0	X	1	0	0	0	8H	Dup. even data register	Dup. even data register
0	X	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0	X	1	1	0	1	DH	Dup. error register	Dup. feature register
0	X	1	1	1	0	EH	Alt. status register	Device control register
0	X	1	1	1	1	FH	Drive address register	Reserved

5.2.3 Primary I/O map (INDEX = 2)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	-IOWR = L
0	X	1FH	0	0	0	0	Data register	Data register
0	X	1FH	0	0	0	1	Error register	Feature register
0	X	1FH	0	0	1	0	Sector count register	Sector count register
0	X	1FH	0	0	1	1	Sector number register	Sector number register
0	X	1FH	0	1	0	0	Cylinder low register	Cylinder low register
0	X	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	X	1FH	0	1	1	0	Drive head register	Drive head register
0	X	1FH	0	1	1	1	Status register	Command register
0	X	3FH	0	1	1	0	Alt. status register	Device control register
0	X	3FH	0	1	1	1	Drive address register	Reserved

5.2.4 Secondary I/O map (INDEX = 3)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	IOWR = L
0	X	17H	0	0	0	0	Data register	Data register
0	X	17H	0	0	0	1	Error register	Feature register
0	X	17H	0	0	1	0	Sector count register	Sector count register
0	X	17H	0	0	1	1	Sector number register	Sector number register
0	X	17H	0	1	0	0	Cylinder low register	Cylinder low register
0	X	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	X	17H	0	1	1	0	Drive head register	Drive head register
0	X	17H	0	1	1	1	Status register	Command register
0	X	37H	0	1	1	0	Alt. status register	Device control register

0	X	37H	0	1	1	1	Drive address register	Reserved
---	---	-----	---	---	---	---	------------------------	----------

5.2.5 True IDE Mode I/O map

-CE2	-CE1	A2	A1	A0	-IORD = L
1	0	0	0	0	Data register
1	0	0	0	1	Error register
1	0	0	1	0	Sector count register
1	0	0	1	1	Sector number register
1	0	1	0	0	Cylinder low register
1	0	1	0	1	Cylinder high register
1	0	1	1	0	Drive head register
1	0	1	1	1	Status register
0	1	1	1	0	Alt. status register
0	1	1	1	1	Drive address register

5.2.6 Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector of data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error and Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

5.2.7 Error register: This register is a read only register, it is used to analyze errors during accesses. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	"0"	IDNF	"0"	ABRT	"0"	AMNF

bit	Name	Function
7	BBK (Bad Block detected)	This bit is set when a Bad Block is detected in a requested ID field.
6	UNC (Data ECC error)	This bit is set when an Uncorrectable error has occurred While reading the card.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (ABoRTed command)	This bit is set if the command has been aborted due to the card status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

5.2.8 Feature register: This register is a write only register and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
------	------	------	------	------	------	------	------

 Feature byte

5.2.9 Sector count register: This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request. This register's initial value is "01H".

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5.2.10 Sector number register: This register contains the starting sector number.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number							

5.2.11 Cylinder low register: This register contains the low 8-bit of the starting cylinder.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low							

5.2.12 Cylinder high register: This register contains the upper 8-bits of the starting cylinder address.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high							

5.2.13 Drive head register: This register is used to select the Drive and Head.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head number			
bit	Name	Function					
7	1	This bit is set to "1".					
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00 : Sector Number Register D7-D0. LBA15-LBA08 : Cylinder Low Register D7-D0. LBA23-LBA16 : Cylinder High Register D7-D0. LBA27-LBA24 : Drive / Head Register bits HS3-HS0.					
5	1	This bit is set to "1".					
4	DRV (DRiVe select)	This bit is used to select Master (Card 0) or Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by DRV# of the Socket and Copy register.					
3 to 0	Head number	This bit is used to select the Head. (Bit 3 is MSB).					

5.2.14 Status register: This register is a read only register which indicates card status. This register should be accessed in byte mode

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7 this	BSY (BuSY)	This bit is set while the card is executing a command. When bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of Receiving read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates a write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seek complete.
3 the	DRQ (Data ReQuest)	This bit is set when information may be transferred between the host and Data register. This bit is cleared when the card receives another command.
2	CORR (CORReCted data)	This bit is set when a correctable data error has occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0 some	ERR (ERRor)	This bit is set when the previous command has ended in some Type of error.

5.2.15 Alternate status register: This register is physically the same as the Status register, however -IREQ is not negated when data is read.

5.2.16 Command register: This register is a write only register. The command register contains the command code being sent to the device. Command execution begins immediately after this register is written.

Command	Command code LBA	Used parameter						
		FR	SC	SN	CY	DR	HD	
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y

Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
 SC: Sector Count register
 SN: Sector Number register
 CY: Cylinder register
 DR: DRV bit of Drive Head register
 HD: Head Number of Drive Head register
 LBA: Logical Block Address Mode Supported
 Y: The register contains a valid parameter for this command.
 N: The register does not contain a valid parameter for this command.

5.2.17 Device control register: This register is write only register, and it is used to control interrupt requests and the issuing of an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X□	X	X	1	SRST	nIEN	0

bit	Name	Function
7 to 4	X	don't care
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling -IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.

6.0 ATA Command specifications

This table summarizes the ATA command set.

6.1 ATA Command Set

No.	Command set LBA	Code	FR	SC	SN	CY	DR	HD
1	Check power mode	E5H or 98H	—	—	—	—	Y	—
2	Execute drive diagnostic	90H	—	—	—	—	Y	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y
5	Identify Drive	ECH	—	—	—	—	Y	—
6	Idle	E3H or 97H	—	Y	—	—	Y	—
7	Idle immediate	E1H or 95H	—	—	—	—	Y	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y
9	Read buffer	E4H	—	—	—	—	Y	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y
11	Read long sector	22H, 23H	—	—	Y	Y	Y	Y
12	Read sector (s)	20H, 21H	—	Y	Y	Y	Y	Y
13	Read verify sector (s)	40H, 41H	—	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—
15	Request sense	03H	—	—	—	—	Y	—
16	Seek	7XH	—	—	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—
19	Set sleep mode	E6H or 99H	—	—	—	—	Y	—
20	Stand by	E2H or 96H	—	—	—	—	Y	—
21	Stand by immediate	E0H or 94H	—	—	—	—	Y	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y
24	Write buffer	E8H	—	—	—	—	Y	—
25	Write long sector	32H or 33H	—	—	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	—	Y	Y	Y	Y	Y
29	Write sector(s) w/o erase	38H	—	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y

Note: FR: Feature Register
 SC: Sector Count register (00H to FFH)
 SN: Sector Number register (01H to 20H)
 CY: Cylinder Low/High register (to)
 DR: Drive bit of Drive/Head register
 HD: Head No.(0 to 3) of Drive/Head register
 NH: No. of Heads
 Y: Set up
 —: Not set up

6.1.1 Check Power Mode (code: E5H or 98H): This command checks the power mode.

6.1.2 Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the Card.

6.1.3 Erase Sector(s) (code: C0H): This command is used to erase data sectors.

6.1.4 Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive. But selected sector data is not exchange. This card accepts a sector buffer of data from the host to follow the command with same protocol as the Write Sector Command.

6.1.5 Identify Drive (code: ECH): This command enables the host to receive parameter information from the Card.

6.1.6 Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0 848AH	2		General configuration bit-significant information
1 XXXX	2		Default number of cylinders
2 0000H	2		Reserved
3 00XXH	2		Default number of heads
4 0000H	2		Number of unformatted bytes per track
5 XXXX	2		Number of unformatted bytes per sector
6 XXXX	2		Default number of sectors per track
7 to 8	XXXX	4	Number of sectors per card (Word7 = MSW, Word8 = LSW)
9 0000H	2		Reserved
10 to 19	XXXX	20	Reserved
20	0002H	2	Buffer type (dual ported)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23 to 46	XXXX	48	Firmware revision in ASCII etc.
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit 8), LBA supported (bit9)
50	0000H	2	Reserved
51	0100H	2	PIO data transfer cycle timing mode 1
52	0000H	2	DMA data transfer cycle timing mode not Supported
53 to 58	XXXX	12	Reserved

59	010XH	2	Multiple sector setting is valid
60 to 61	XXXX	4	Total number of sectors addressable in LBA Mode
62 to 255	0000H	388	Reserved

6.1.7 Idle (code: E3H or 97H): This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

6.1.8 Idle Immediate (code: E1H or 95H): This command causes the Card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

6.1.9 Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cylinder.

6.1.10 Read Buffer (code: E4H): This command enables the host to read the current contents of the card's sector buffer.

6.1.11 Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

6.1.12 Read Long Sector (code: 22H or 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

6.1.13 Read Sector(s) (code: 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

6.1.14 Read Verify Sector(s) (code: 40H or 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host .

6.1.15 Recalibrate (code: 1XH): This command is effectively a NOP command to the Card and is provided for compatibility purposes.

6.1.16 Request Sense (code: 03H): This command requests an extended error code after command ends with an error.

6.1.17 Seek (code: 7XH): This command is effectively a NOP command to the Card although it does perform a range check.

6.1.18 Set Features (code: EFH): This command is used by the host to establish or select certain features.

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Disable 8-bit data transfers.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

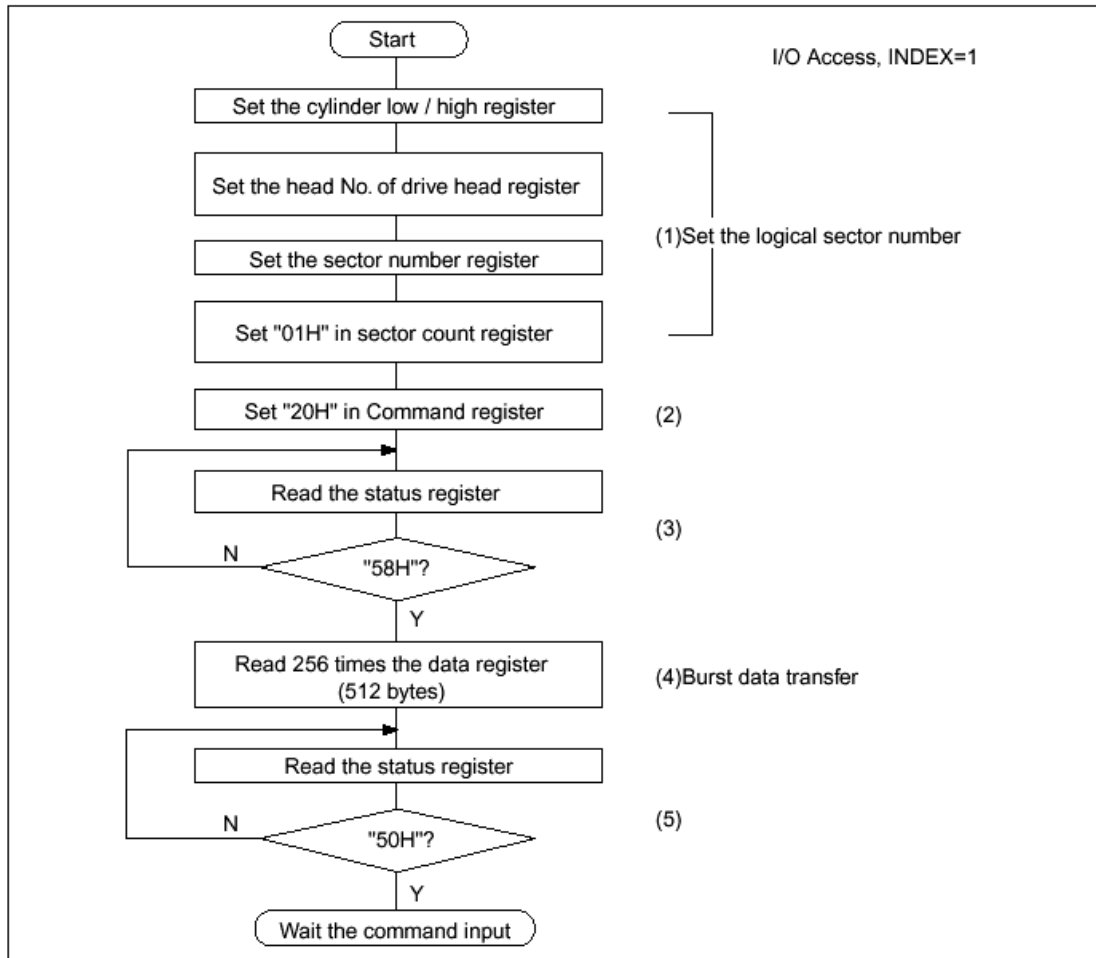
- 6.1.19 Set Multiple Mode (code: C6H):** This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.
- 6.1.20 Set Sleep Mode (code: E6H or 99H):** This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
- 6.1.21 Stand By (code: E2H or 96H):** This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
- 6.1.22 Stand By Immediate (code: E0H or 94H):** This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
- 6.1.23 Translate Sector (code: 87H):** This command allows the host a method of determining the exact number of times a user sector has been erased and programmed.
- 6.1.24 Wear Level (code: F5H):** This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00H indicating Wear Level is not needed.
- 6.1.25 Write Buffer (code: E8H):** This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.
- 6.1.26 Write Long Sector (code: 32H or 33H):** This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
- 6.1.27 Write Multiple (code: C5H):** This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
- 6.1.28 Write Multiple without Erase (code: CDH):** This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.
- 6.1.29 Write Sector(s) (code: 30H or 31H):** This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

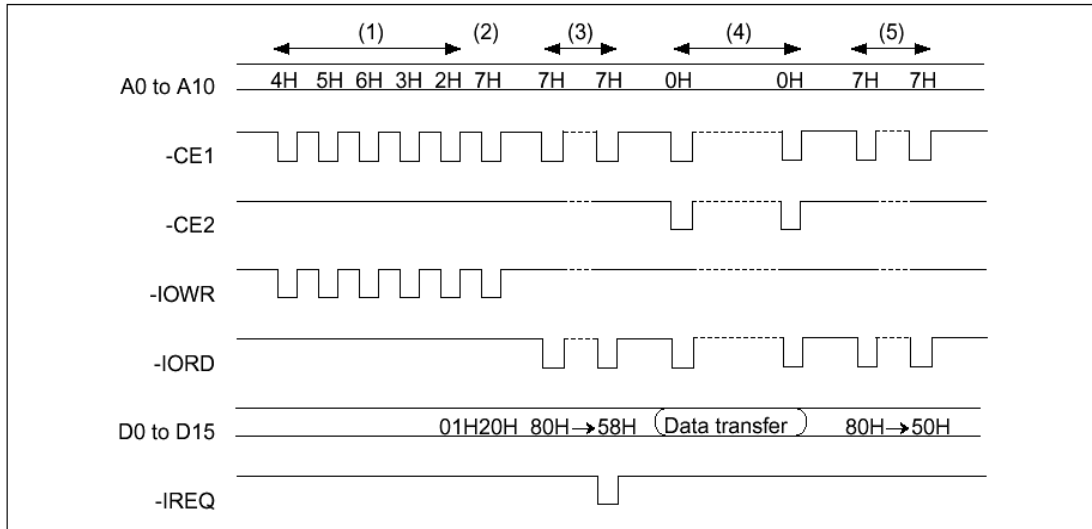
6.1.30 Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

6.1.31 Write Verify (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

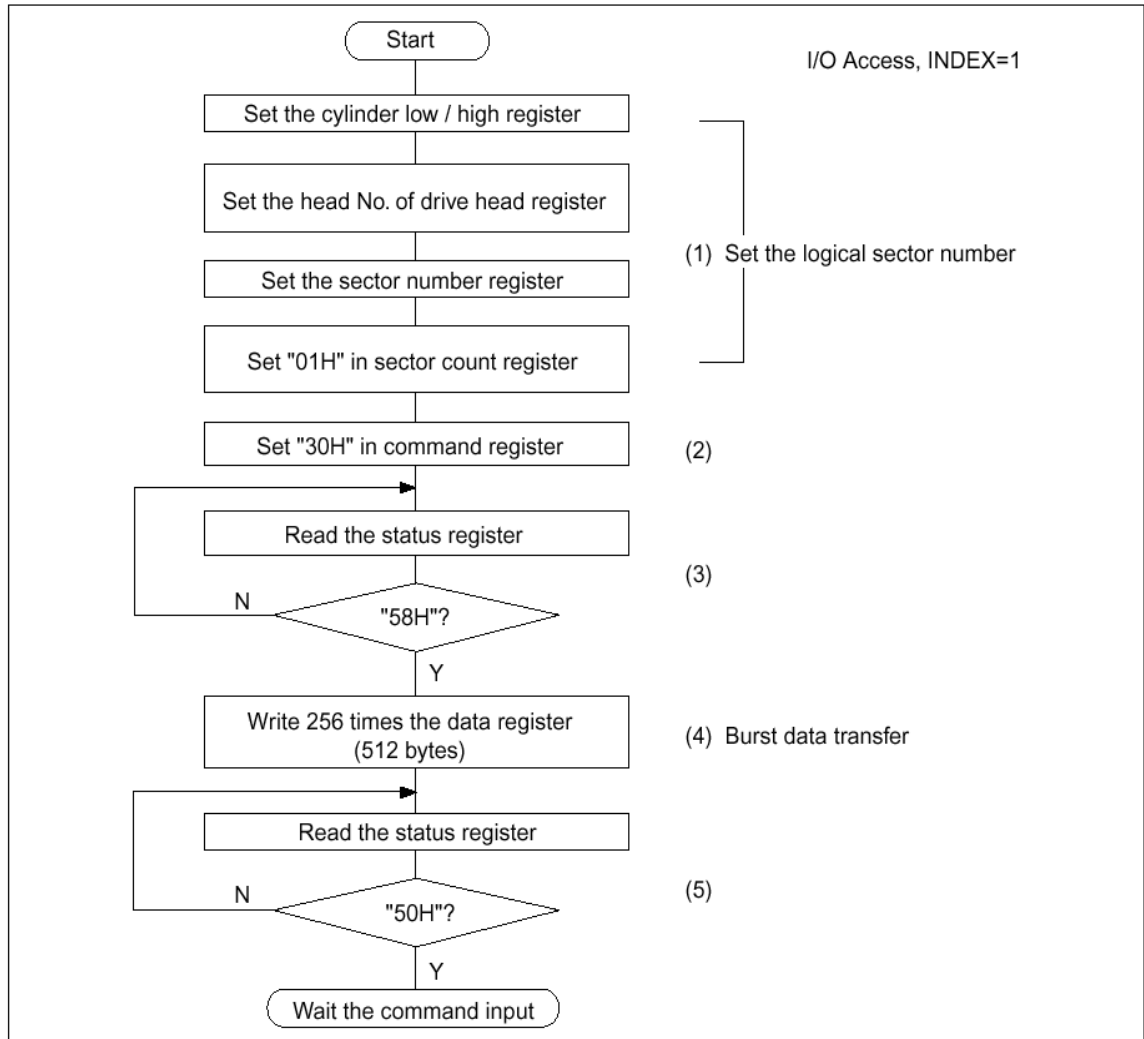
6.2 Sector Transfer Protocol

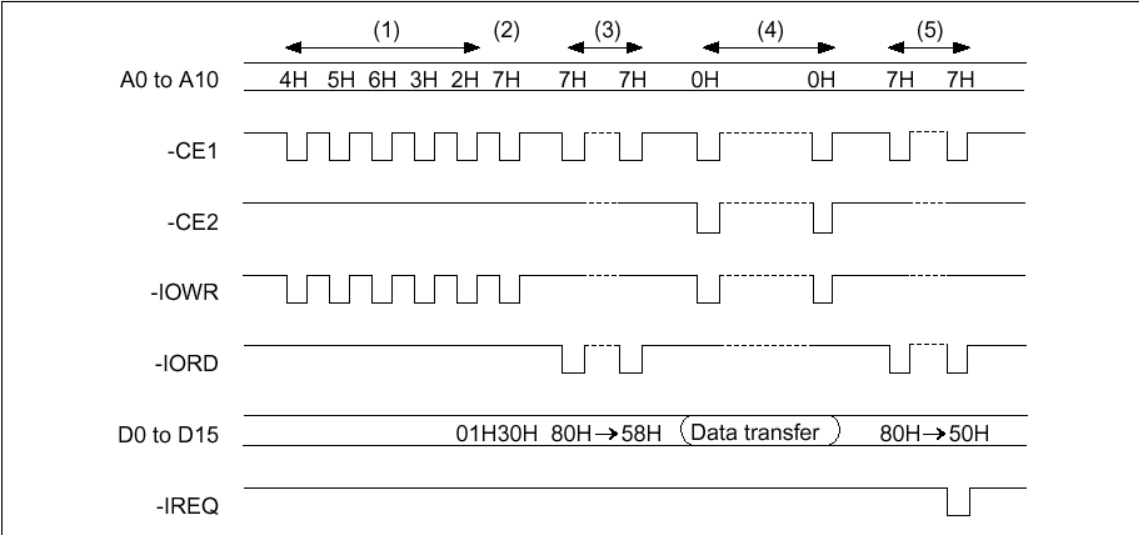
6.2.1 Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.





6.2.2 Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.





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