AN1703
APPLICATION NOTE

GUIDELINES FOR USING ST'S MOSFET SMD PACKAGES

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1. ABSTRACT

The trend from through-hole packages to low-cost SMD-applications is marked by the improvement of chip technologies. "Silicon instead of heatsink" is therefore possible in many cases. Many applications today use PCBs assembled with SMD-technologies, the emphasis being on Power ICs in SMD packages mounted on single-sided PCBs laminated on one side.

The printed circuit board (PCB) itself becomes the heatsink. In early fabrications a solid heatsink was either screwed or clamped to the power package. It was easy to calculate the thermal resistance from the geometry of the heatsink.

In SMD-technology, this calculation is much more difficult because the heat path must be evaluated: chip (junction) - lead frame - case or pin - footprint - PCB materials (basic material, thickness of the laminate) - PCB volume - surroundings.

As the layout of the PCB is a main contributor to the result, a new technique must be applied. Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package.

The power dissipation for a SMD device is a function of the drain pad size, which can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. The measurements achieved on SMD packages for different drain pad size show that by increasing the area of the drain pad the power dissipation can be increased.

Although one can achieve improvements in power dissipation with this method, the tradeoff is to use valuable board area.

Next we consider the common ST MOSFET SMD packages (D^2PAK, DPAK, SOT-223, SO-8, PowerSO-8™, PowerFLAT™ (5x5) and (6x5), TSSOP8 and PowerSO-10™) with their recommended footprints. For each of these packages we will show the power dissipation for the minimum footprint and for a large drain pad area ($1in^2$ or $600mm^2$) using the max measured $R_{THJ-PCB}$.

We will show the maximum allowable power dissipation versus drain pad area for different T_J-T_A values as well.

Finally we will make a thermal performance comparison for all SMD packages analysed.

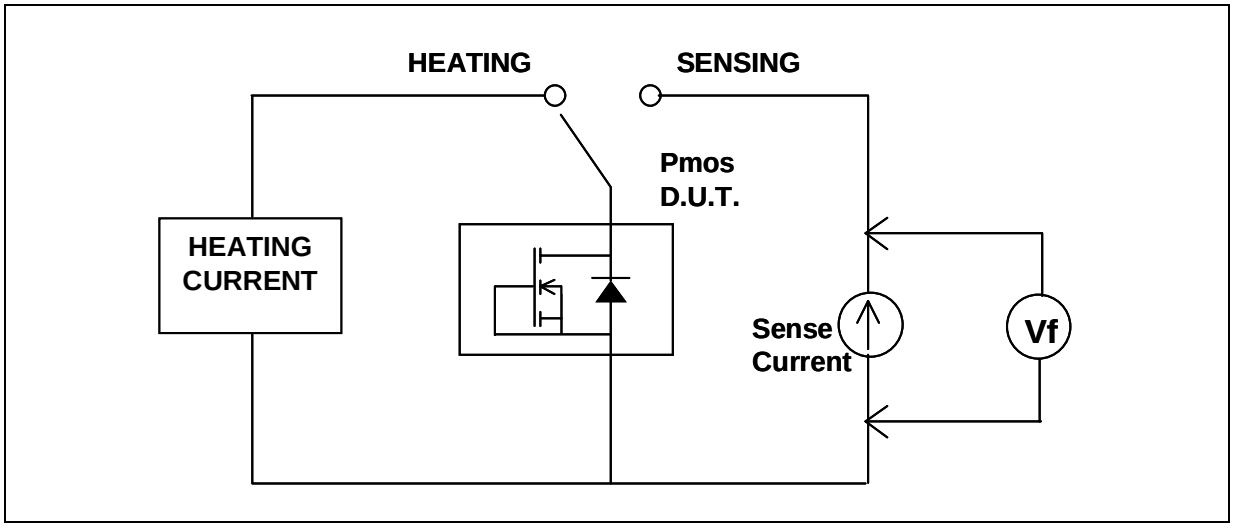
Information regarding the mechanical dimensions for each SMD package can be found on the related datasheets.

2. THERMAL MEASUREMENTS

The most practical method of optimizing thermal performance is to characterize the MOSFET on the PCB where it will be used. The basis of this method is to dissipate a known amount of power in the MOSFET, and to measure the amount of temperature rise this causes in the junction, given the data

required to calculate the junction to PCB thermal resistance (°C/W).
The procedure has two main steps. First is the characterization of the body diode. Second is the temperature rise measurements and calculation of the thermal resistance.
As an inherent part of the MOSFET structure, the body diode makes the ideal sensor to measure the junction temperature, since the forward voltage V_F varies with temperature, approximately -2.2mV/°C. For this the diode's temperature coefficient is needed to get an accurate representation of the junction temperature. The forward voltage is measured with a low level current flowing through it to ensure there is no self heating, which would make the junction temperature measurement inaccurate.
The MOSFET being characterized is soldered on to the thermal test PCB and has the gate shorted to the source, to insure the MOSFET cannot turn on. The copper mounting pad reaches the remote connection points through fine traces that do not contribute significant thermal dissipation but serve the purpose of electrical connections.
Figure 1 illustrate the schematic of R_{TH} measurements where the MOSFET 's drain and source are connected with two power supplies.

Figure 1: Schematic of temperature measurements



The first power supply forces current through the body diode to heat the junction with a fixed power level, when the switch is in the "heating" position. The second power supply provides the sensing current for measuring the junction temperature, through the V_F measurement, when the switch is in the "sensing" position.

The measure of $R_{THJ\text{-}PCB}$ is based on the well know relationship between the power being dissipated in the devices and the relevant arising junction temperature:

$$R_{THJ-PCB} = \frac{\Delta T}{P_D} = \frac{T_J - T_C}{P_D}$$

This computation is made from pulsed operation to steady state in order to achieve the whole thermal transient response of the device under test. The applied power P_D is fixed by the equipment in terms of magnitude and time duration, so it is an input data.

What we now have to compute is the T_J value since T_C is also an input data related to ambient or case temperature. To detect the arising junction temperature (T_J), we look at the variation of the forward drop of the drain-source diode, since this variation is proportional to the change in junction temperature.

3. D²PAK

The D²PAK is a surface mounting version of the standard TO-220 package, with the lead formed and the tab removed. It has been designed to achieve the high quality and reliability levels required by end users in the automotive industry.

Figure 2 shows D²PAK and its recommended footprint:

Figure 2: D²PAK and its recommended footprint (all dimensions are in mm)

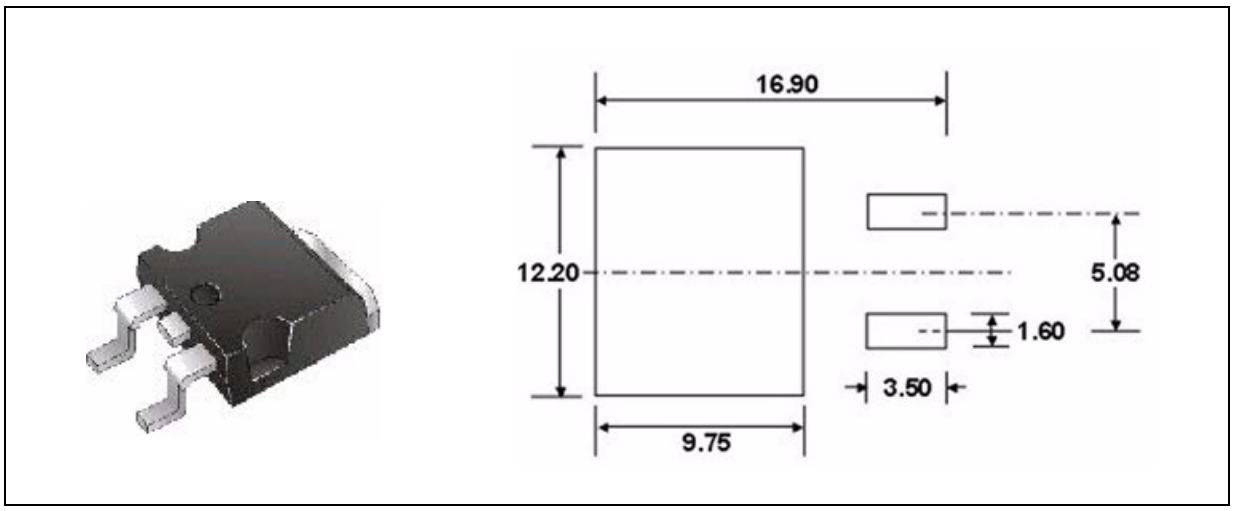
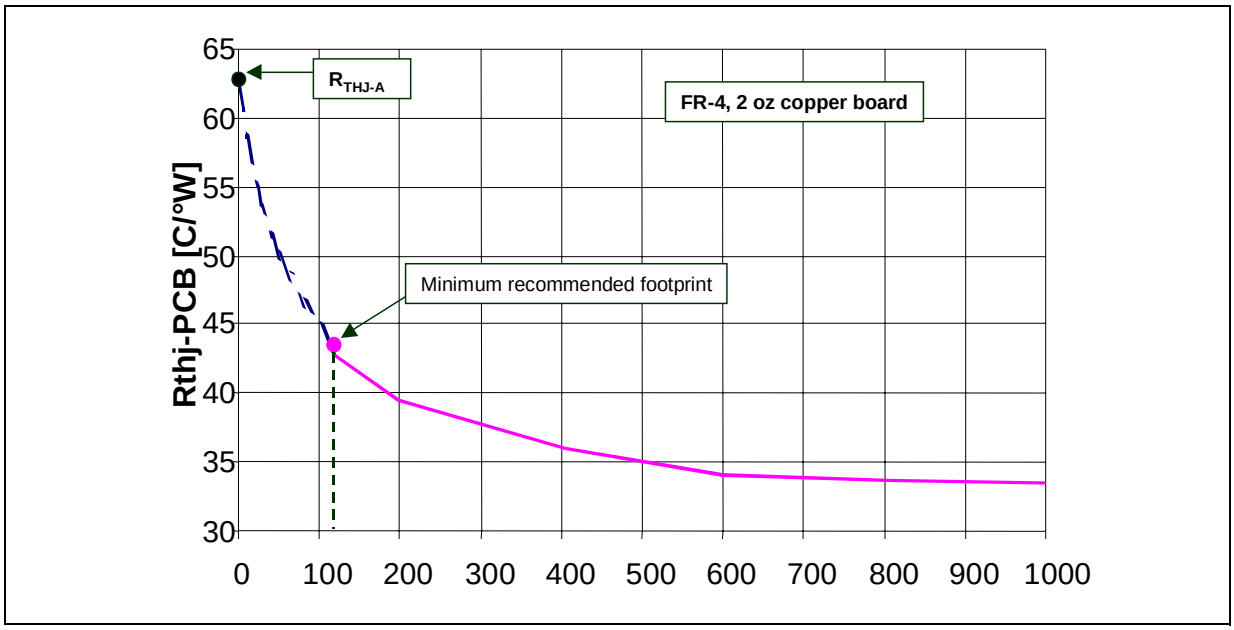


Figure 3 shows a graph of $R_{THJ\text{-}PCB}$ versus drain pad area from minimum recommended footprint to 10cm²:

Figure 3: $R_{THJ\text{-}PCB}$ versus drain pad area for D²PAK



In free air we must consider the R_{THJ-A}, with a value of 62.5°C/W, like that of the TO-220.

For the minimum recommended footprint (120mm^2) the $R_{THJ-PCB}$ value is 42°C/W and the maximum allowable power dissipation turns out to be:

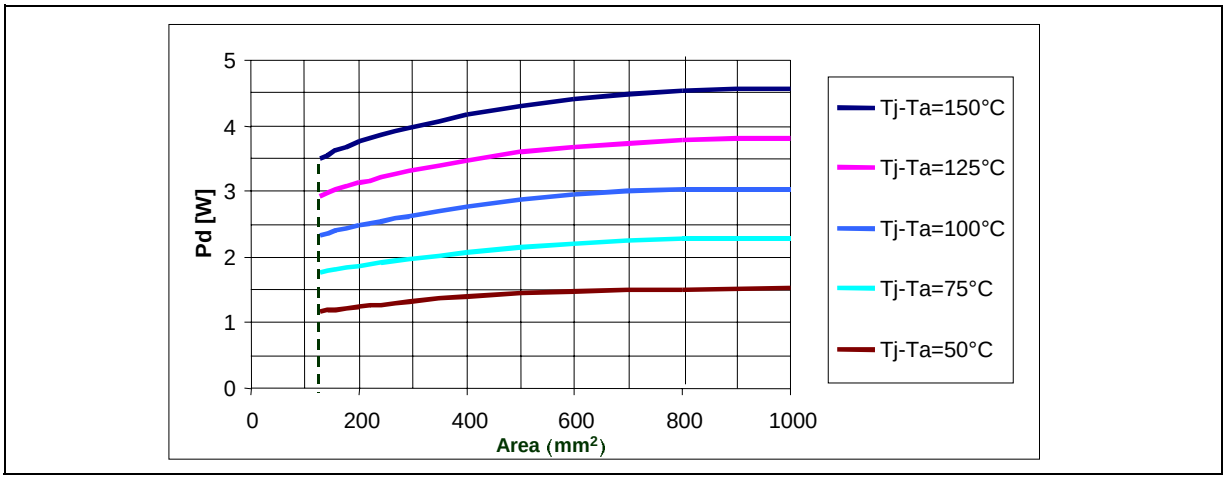
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{150}{42} = 3.5W \quad (T_{JMAX} = 175°C,\ T_C = 25°C)$$

For a drain pad area of 1in^2(about 600mm^2) we obtain**:**

$$R_{THJ-PCB} = 34\,{}^{°C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4.4W$$

The next figure shows the maximum allowable power dissipation versus drain pad area for different T_J-T_A values:

Figure 4: Maximum allowable power dissipation versus drain pad area



4. DPAK

Similar considerations can be made for DPAK, where its minimum recommended footprint is shown in figure 5:

Figure 5: DPAK and its recommended footprint (all dimensions are in mm)

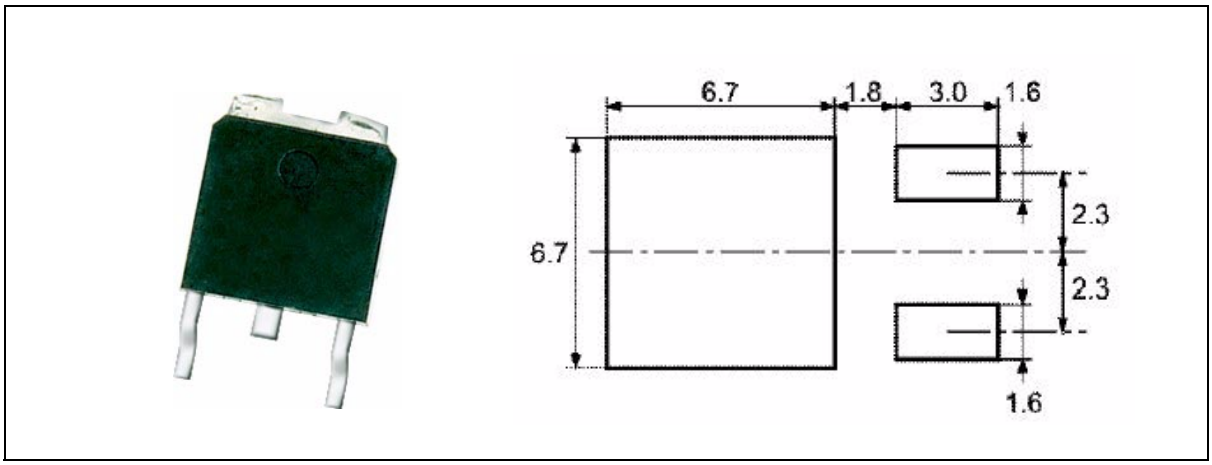
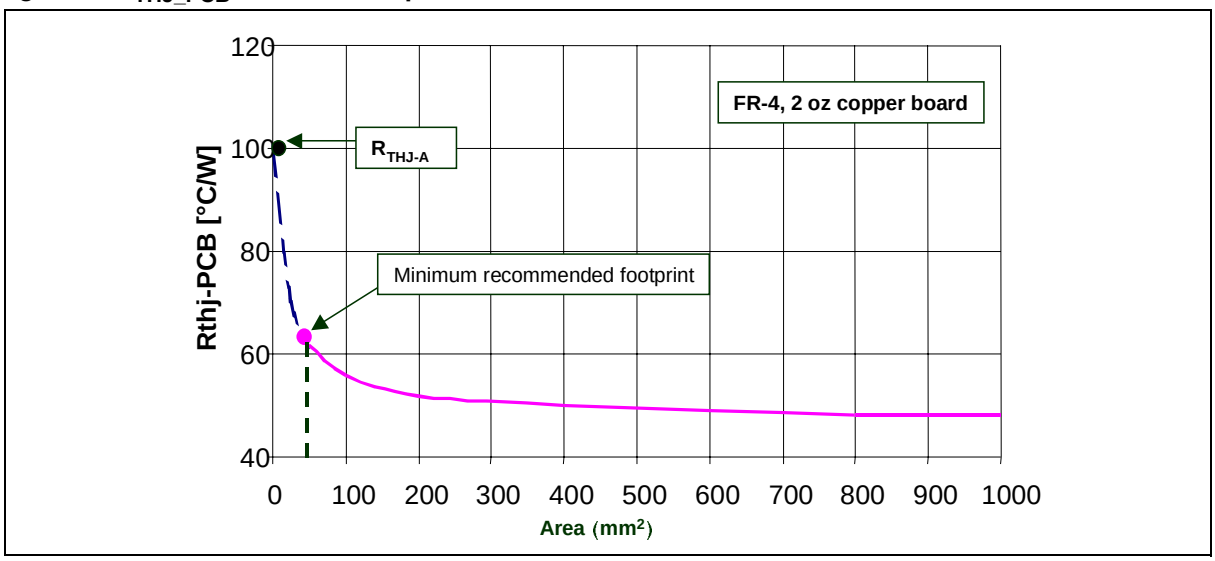


Figure 6 shows a graph of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to $10cm^2$:

Figure 6: R_{THJ_PCB} versus drain pad area for DPAK



In free air we must consider the R_{THJ-A} and its value 100°C/W.

For the recommended footprint (45mm^2) the $R_{THJ-PCB}$ value is 62°C/W and the maximum allowable power dissipation is:

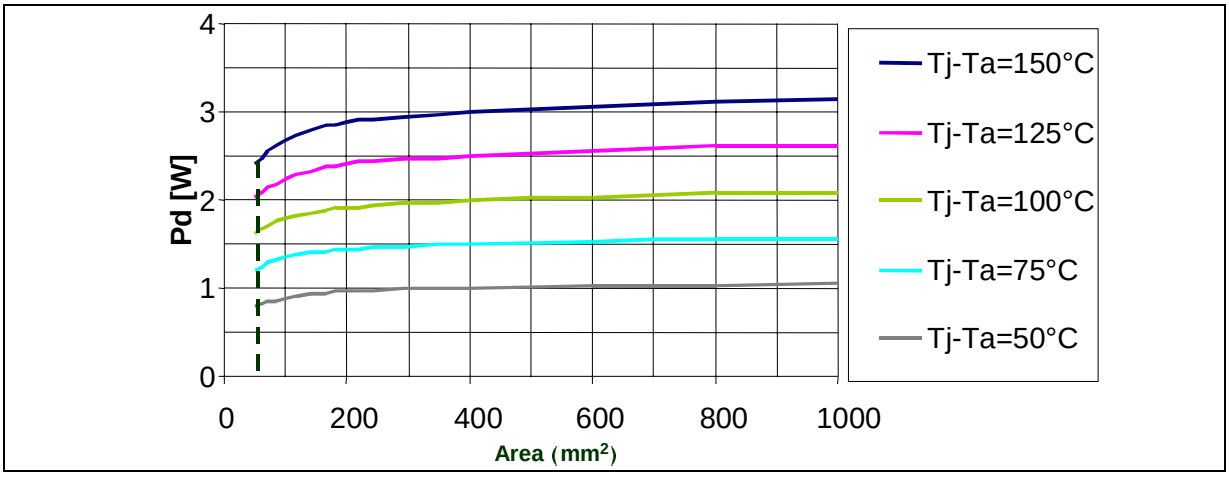
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{150}{62} = 2.4W \quad (T_{JMAX} = 175°C, T_C = 25°C)$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 50\,{}^{\circ C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3W$$

The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values:

Figure 7: Maximum allowable power dissipation versus drain pad area



5. SOT-223

The SOT-223 is a small package designed for surface mount applications. The formed leads absorb thermal stress during soldering, thereby eliminating the possibility of damage to the die. The encapsulation material used in this package enhances the device reliability which allows it to exhibit excellent performance in high temperature environments.

Figure 8: SOT-223 and its recommended footprint (all dimensions are in mm)

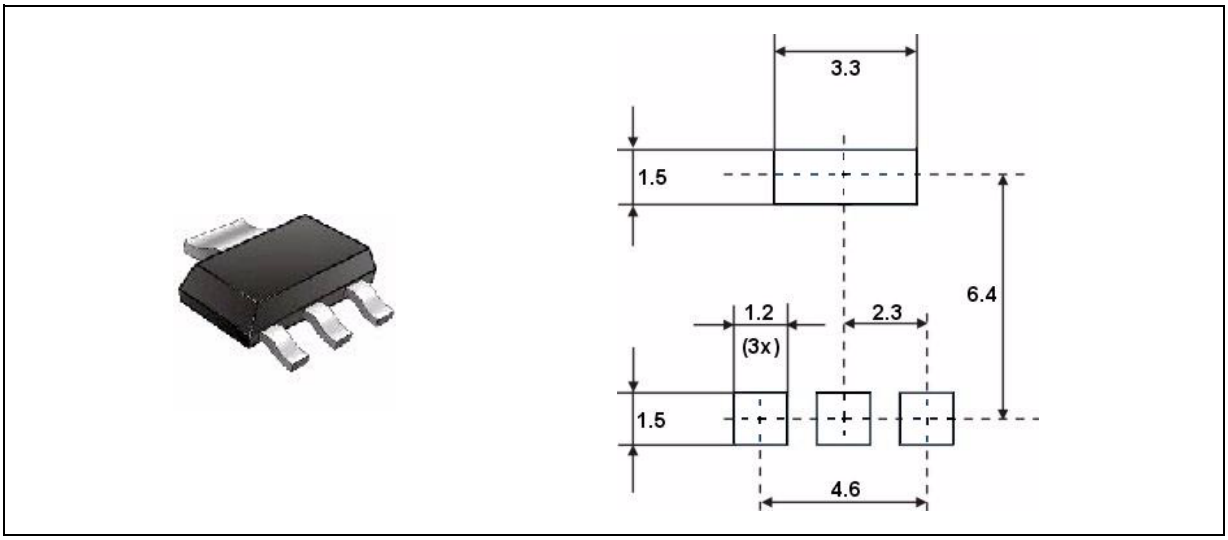
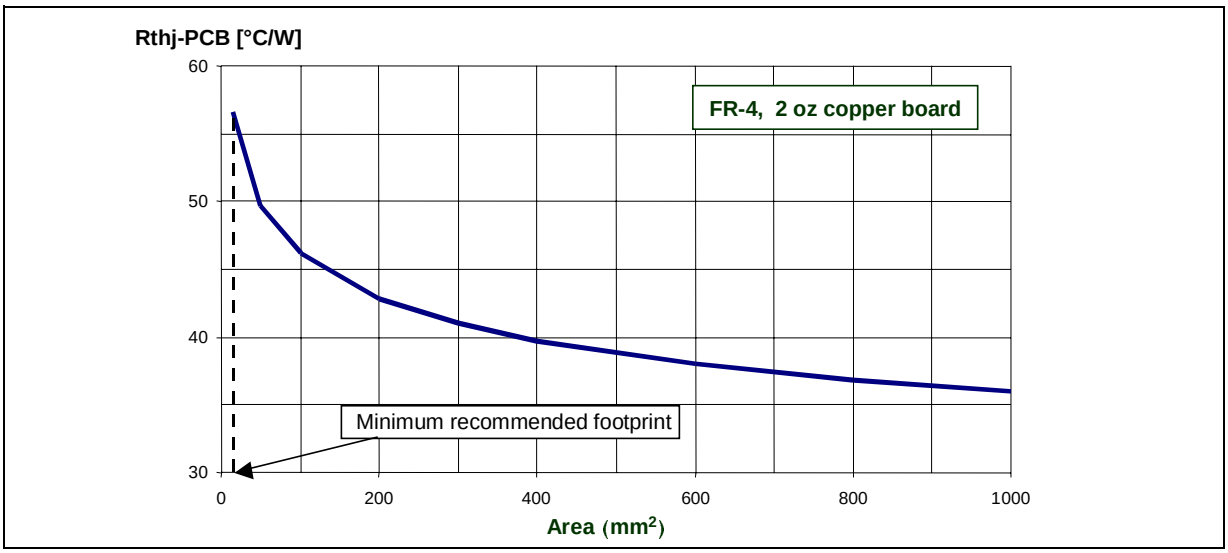


Figure 9 shows the measured values of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2, for $t \leq 10s$ as power pulse:

Figure 9: $R_{THJ-PCB}$ versus drain pad area for SOT-223



Measurements performed for minimum recommended footprint (15mm^2) and $t \leq 10s$ give $R_{THJ-PCB}$ = 56.6°C/W and the maximum allowable power dissipation results:

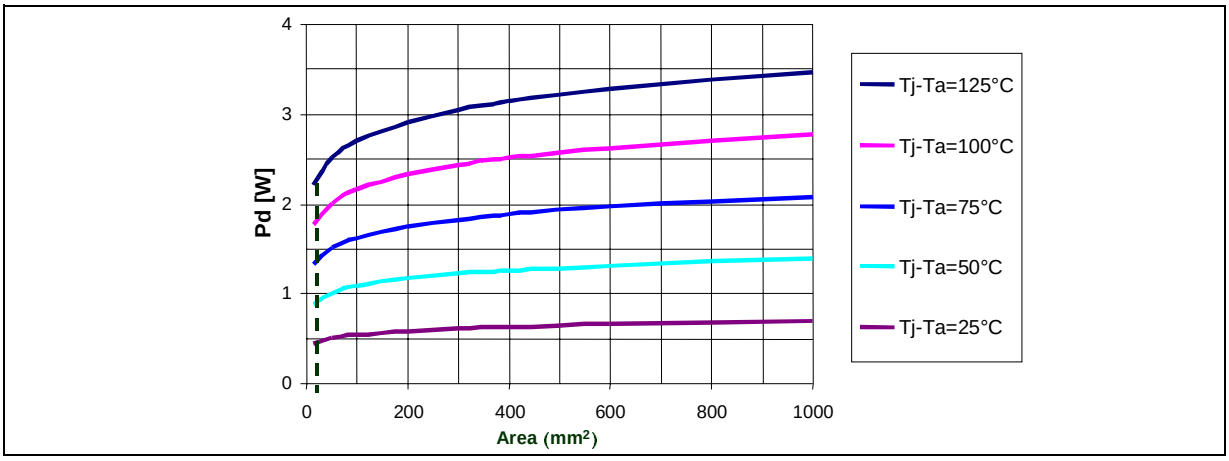
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{56.6} = 2.2W \quad (T_{JMAX} = 150°C, T_C = 25°C)$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 38\,^{\circ C}/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3.3W$$

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

Figure 10: Maximum allowable power dissipation versus drain pad area



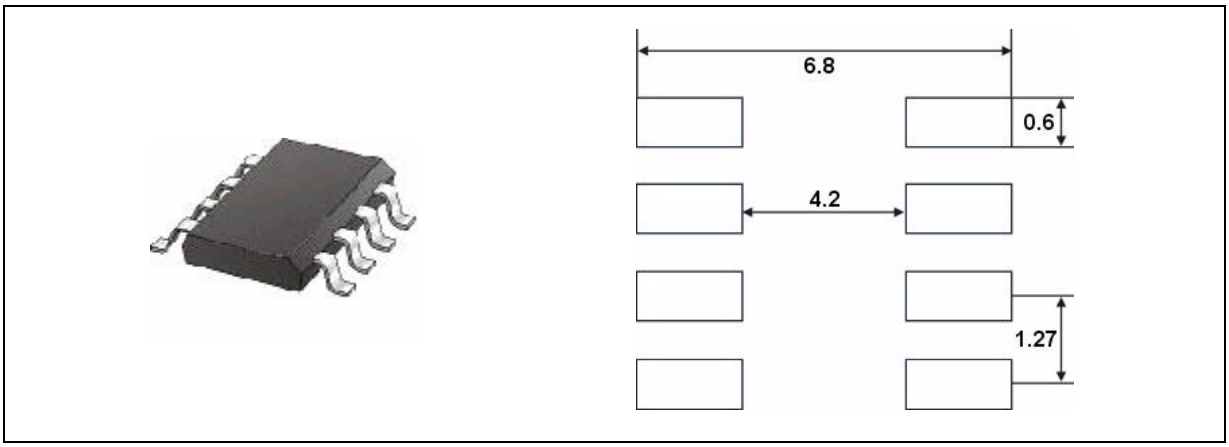
6. SO-8

The basis of the pad design for an SO-8 MOSFET is the package footprint. In converting the footprint to the pad set for a MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

For the SO-8 the thermal connections are very simple. Pins 5, 6, 7 and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain.

In figure 11 the basic SO-8 footprint is shown.

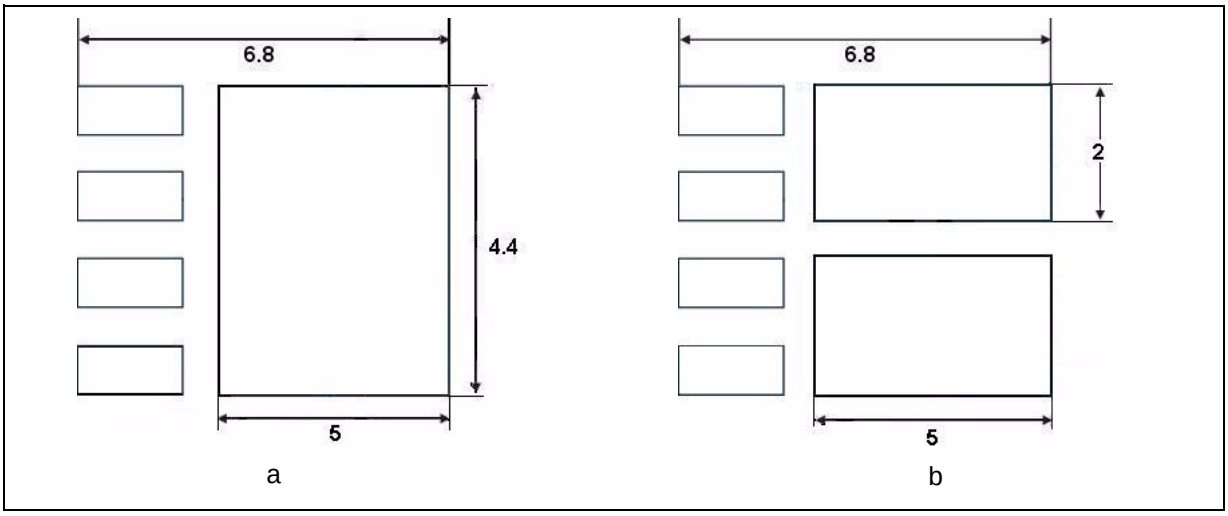
Figure 11: SO-8 and its basic footprint (all dimensions are in mm)



For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate.

The minimum recommended pad patterns for the single MOSFET SO-8 (figure 12a) and dual MOSFET SO-8 (figure 12b) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins.

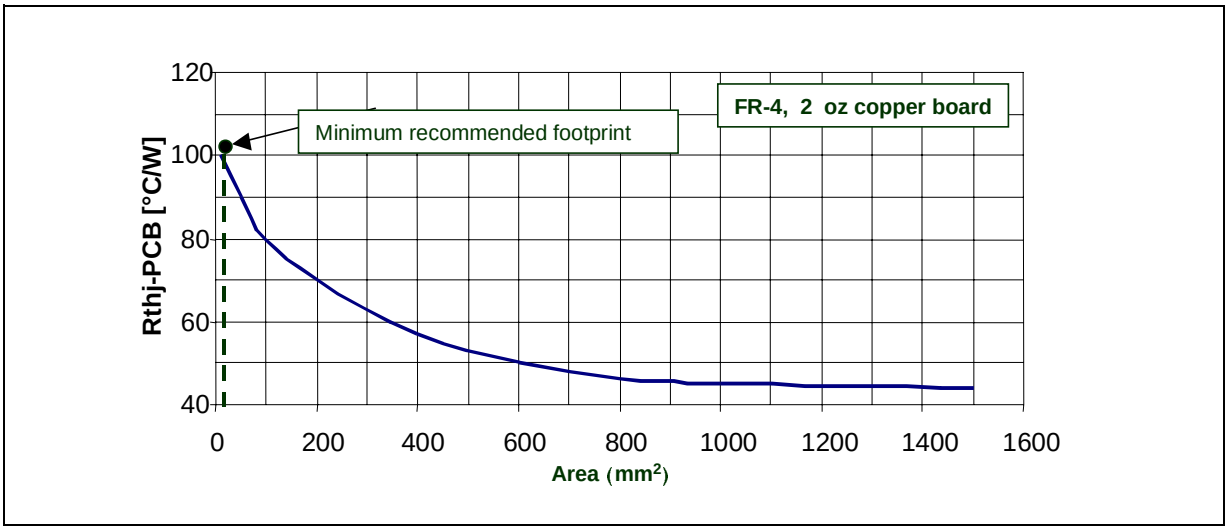
Figure 12:Single (a) & dual MOSFET (b) SO-8 minimum recommended pad pattern (all dimensions are in mm)



These connections provide planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the PCB. These patterns use all the available area underneath the body for this purpose.

Figure 13 shows a graph of $R_{THJ\text{-}PCB}$ versus drain pad area from minimum recommended footprint to 15cm^2, for $t \leq 10s$ as power pulse:

Figure 13: $R_{THJ\text{-}PCB}$ versus drain pad area for SO-8



For the minimum recommended footprint (22mm^2 for a single MOSFET and 10mm^2 for a dual MOSFET) the thermal resistance value is about $R_{THJ\text{-}PCB}$ = 100°C/W and the maximum allowable power dissipation results:

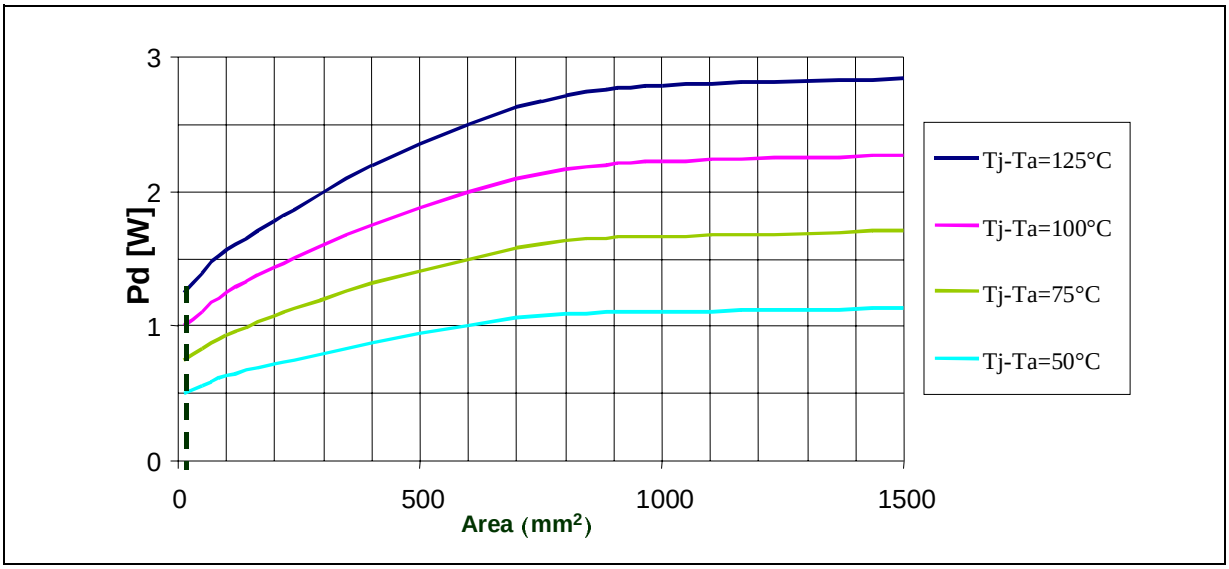
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{100} = 1.25W \quad (T_{JMAX} = 150°C, T_C = 25°C)$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 50\,^{\circ C}/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 2.5W$$

The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values.

Figure 14: Maximum allowable power dissipation versus drain pad area



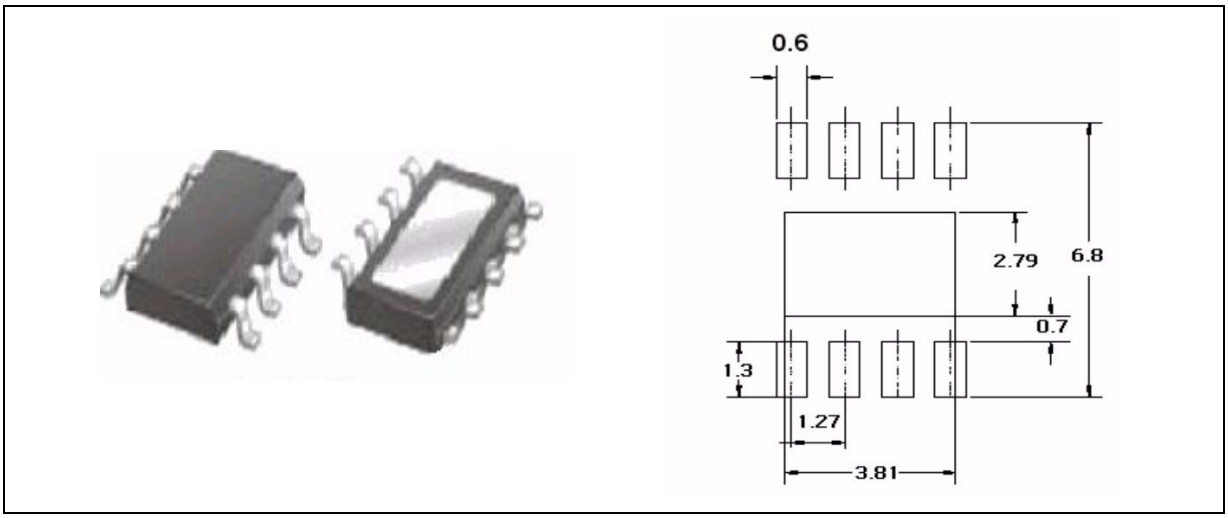
7. PowerSO-8™

To enlarge our product range and, in the meantime, improve the performance of our MOSFETs housed in SMD packages, we are introducing new options to comply with the next generation of DC to DC converters for the computer and telecom areas. In such applications high output current and good thermal performances are required. This new package tailored to the above requirements is PowerSO-8. Furthermore, power devices housed in this package can be used for automotive applications such as body electronic applications (door looking, wipers, seat positioning systems and so on).

PowerSO-8 is the power version of the standard SO-8 package. It maintains the same footprint as SO-8, but it also has a solderable drain contact on the back. Given that heat is dissipated through the drain and source leads and also through the back of the package, the junction-case thermal resistance is

drastically reduced and consequently the device is able to manage higher currents.
Figure 15 shows PowerSO-8 and its minimum recommended footprint.

Figure 15: PowerSO-8 with its minimum recommended footprint (all dimension are in mm)



Commonly pins 5 to 8 are the drain and are connected together to the exposed pad, so we have the same situation as figure 12a, while pin 4 is the gate and pins 1 to 3 are the source. Figure 16 shows the PowerSO-8 internal structure.

Figure 16: PowerSO-8™ internal structure

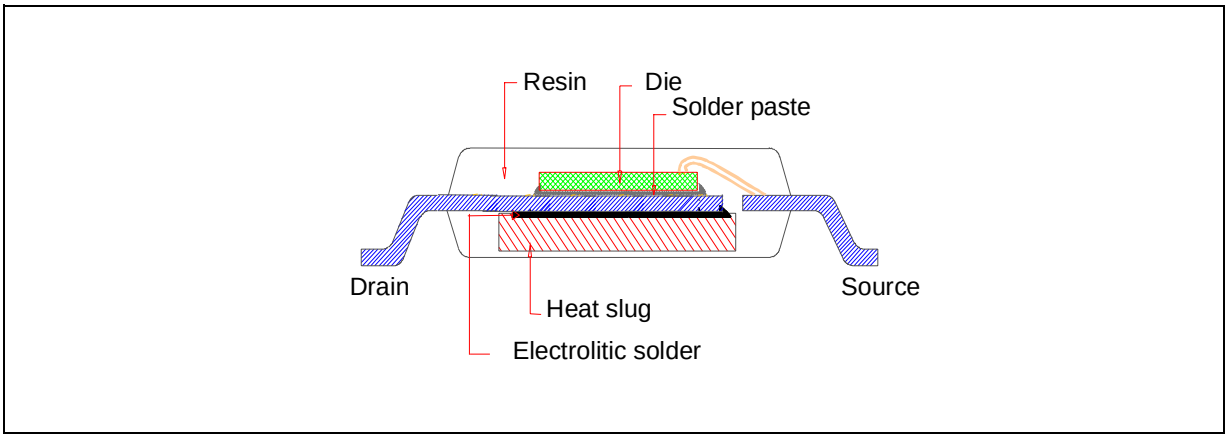
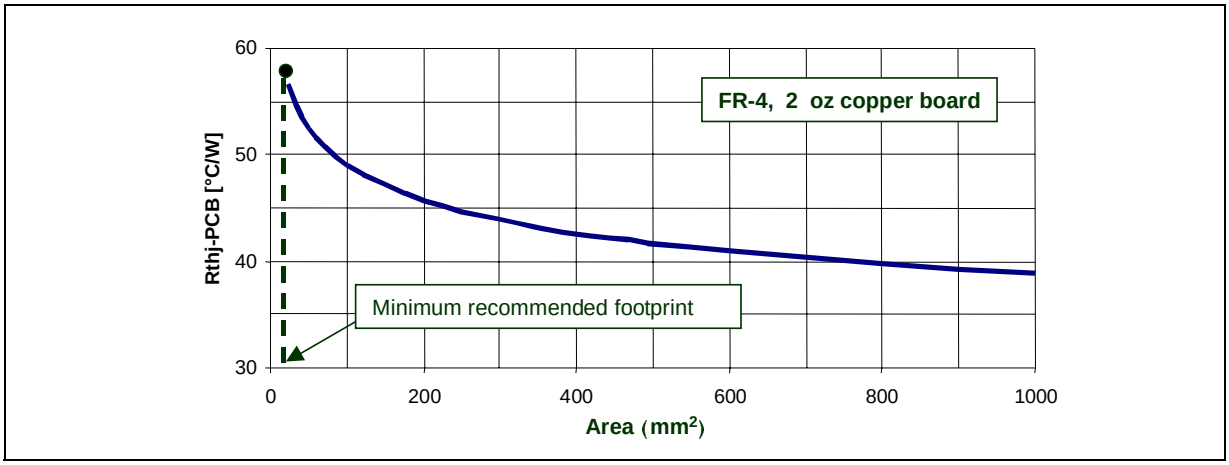


Figure 17 shows a graph of $R_{THJ\text{-}PCB}$ versus drain pad area from minimum recommended footprint to $10cm^2$, for $t \leq 10s$ as power pulse:

Figure 17: R_{THJ_PCB} versus drain pad area for PowerSO-8™



For the minimum recommended footprint ($23mm^2$) the thermal resistance value is about $R_{THJ\text{-}PCB}$ = 56.6 °C/W and the maximum allowable power dissipation results:

$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{56.6} = 2.2W \quad (T_{JMAX} = 150°C,\ T_C = 25°C)$$

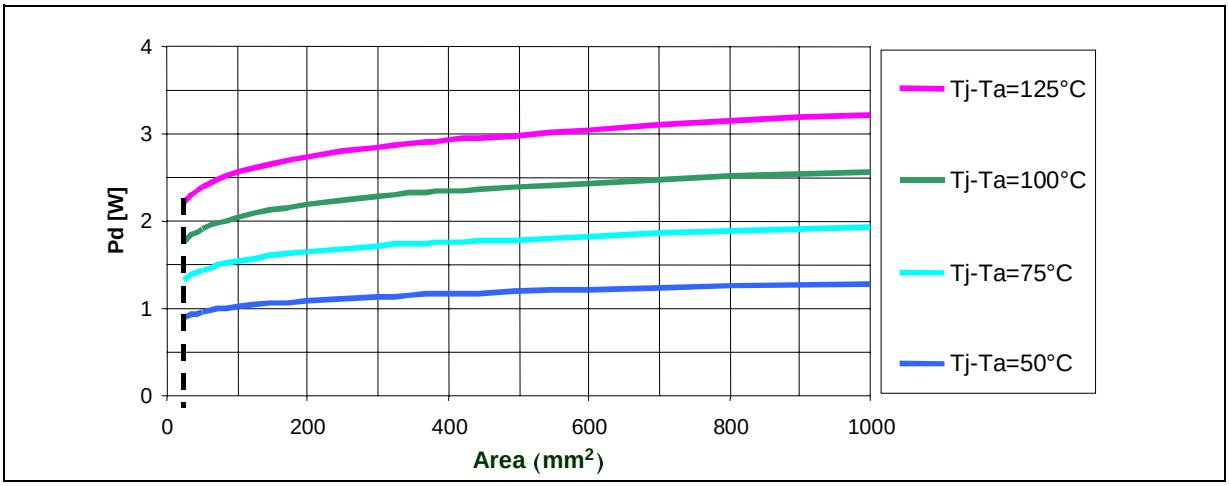
For a drain pad area of $1in^2$ (about $600mm^2$) we obtain:

$$R_{THJ-PCB} = 42\,{}^{°C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3W$$

that is 20% higher than that of the standard SO-8.

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

Figure 18: Maximum allowable power dissipation versus drain pad area



8. PowerFLAT™ (5x5) and PowerFLAT™ (6x5)

PowerFLAT, in both (5x5) and (6x5) versions, depending on the package body size in (mm x mm), allows substantially bigger die capability with respect to the old-fashioned SO-8, still with reduced height and weight. This in turn translates into a remarkable board space reduction. Furthermore, the lower profile (1mm) allows higher operation frequency due to less inductance.
The leads are accommodated into the plastic body in such a way that a perfect co-planarity in assured. Also a better thermal impedance is achieved by means of the exposed pad that provides a thermal path from the die attached copper frame directly to the PCB.
The above features are exactly what designers demand in making their designs increasingly more efficient.
Not only is the PowerFLAT (5x5) smaller, but it also differs from PowerFLAT (6x5) in the way the pads are connected to the package. In fact, in PowerFLAT (5x5) the source terminals are on both sides while the drain coincides with the exposed back metal side only. The PowerFLAT (6x5) case is pin to pin compatible with a standard SO-8 package, it can house a larger die, and the exposed pad is connected to the drain as well.

Figure 19: PowerFLAT (5x5) and PowerFLAT (6x5)

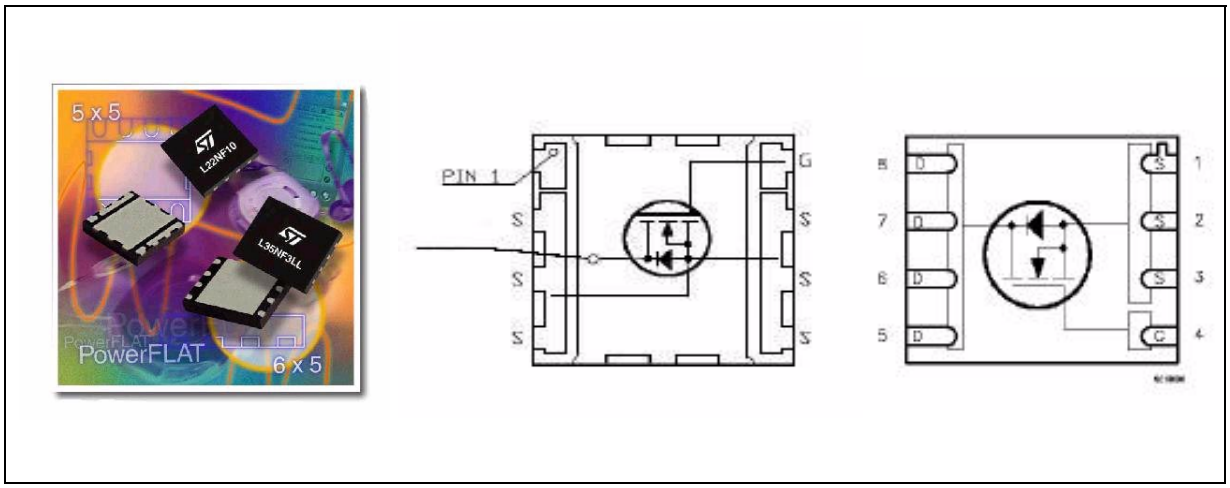


Figure 20 shows minimum recommended footprints for both types of PowerFLAT.

Figure 20:PowerFLAT (5x5) (a) and PowerFLAT (6x5) (b) minimum recommended footprints (all dimension are in mm)

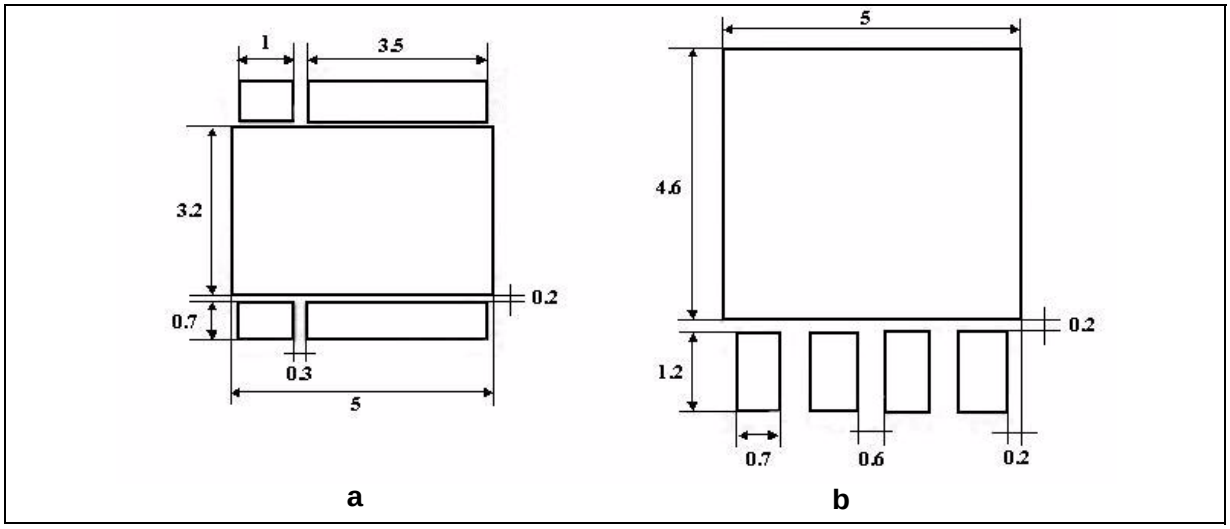
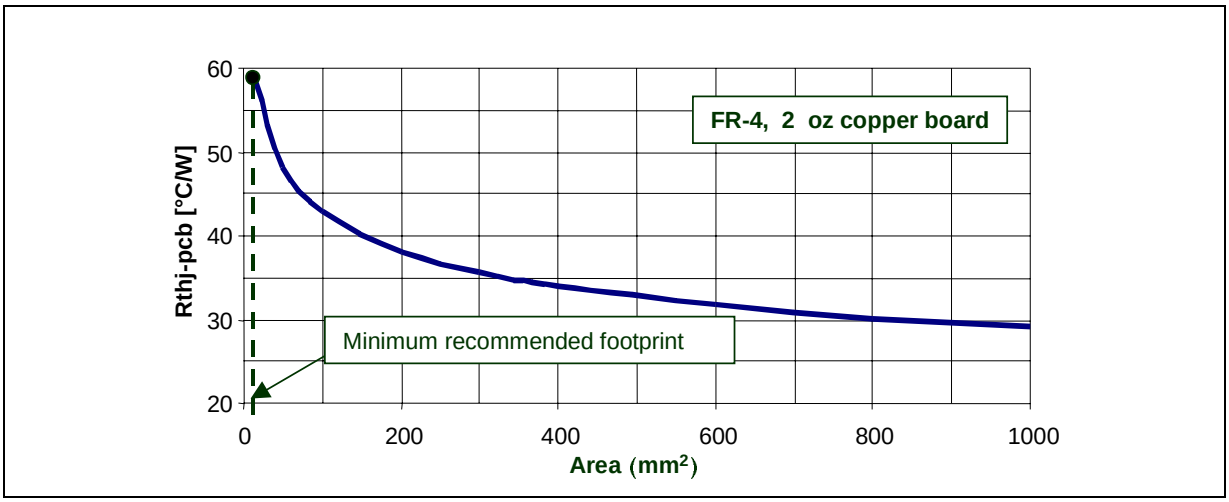


Figure 21 (obtained by measurements performed on PowerFLAT) shows the $R_{THJ\text{-}PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2, for $t \leq 10s$ as power pulse:

Figure 21: R_{THJ_PCB} versus drain pad area for both types of PowerFLAT™



For the minimum recommended footprint the thermal resistance value is about $R_{THJ\text{-}PCB}$ = 60 °C/W and the maximum allowable power dissipation results:

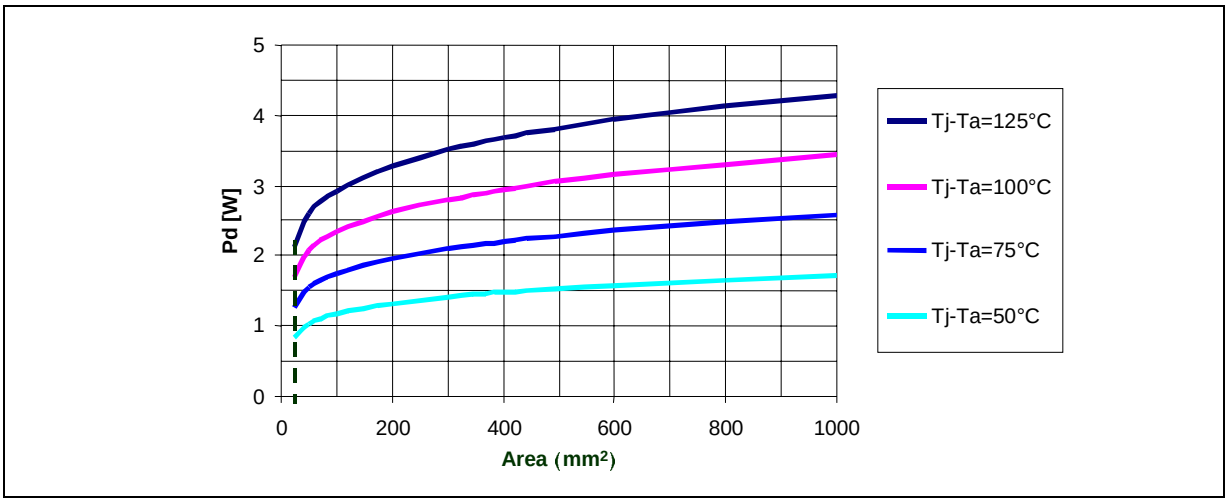
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{60} = 2.1W \quad (T_{JMAX} = 150°C,\ T_C = 25°C)$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 31.2\,{}^{\circ C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4W$$

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

Figure 22: Maximum allowable power dissipation versus drain pad area



9. TSSOP8

The new TSSOP8 power MOSFET package is the natural evolutionary response to the continuing demands of many markets for smaller packages. It has a smaller footprint and a lower profile than standard the SO-8 package, while maintaining low on-resistance and a good thermal performance. Furthermore TSSOP8 packages require approximately half the PCB area of a standard SO-8. It is available both in single die and/or in double dice in common drain configuration.
Figure 23 shows TSSOP8 and its internal schematic for dual configuration:

Figure 23: TSSOP8 package and its internal schematic

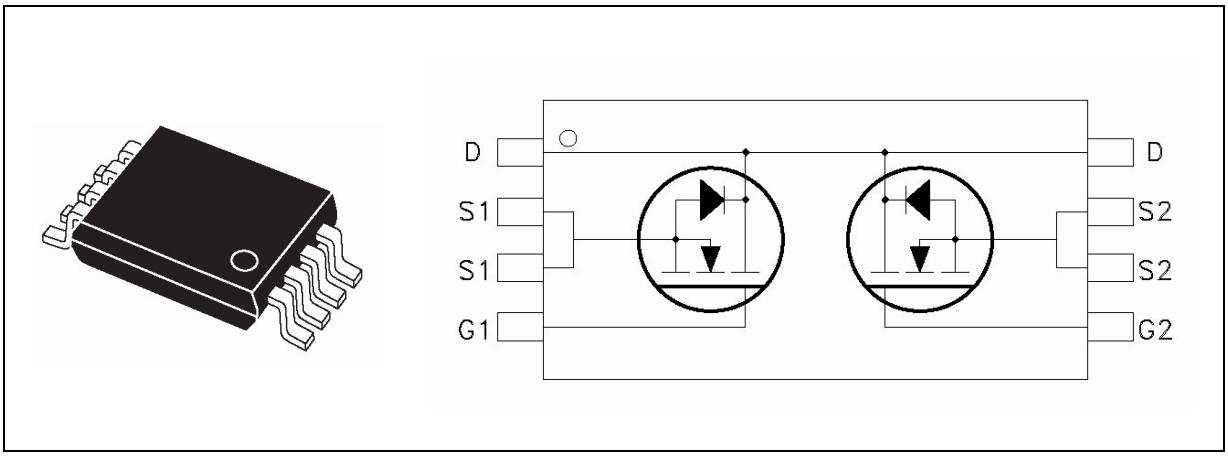
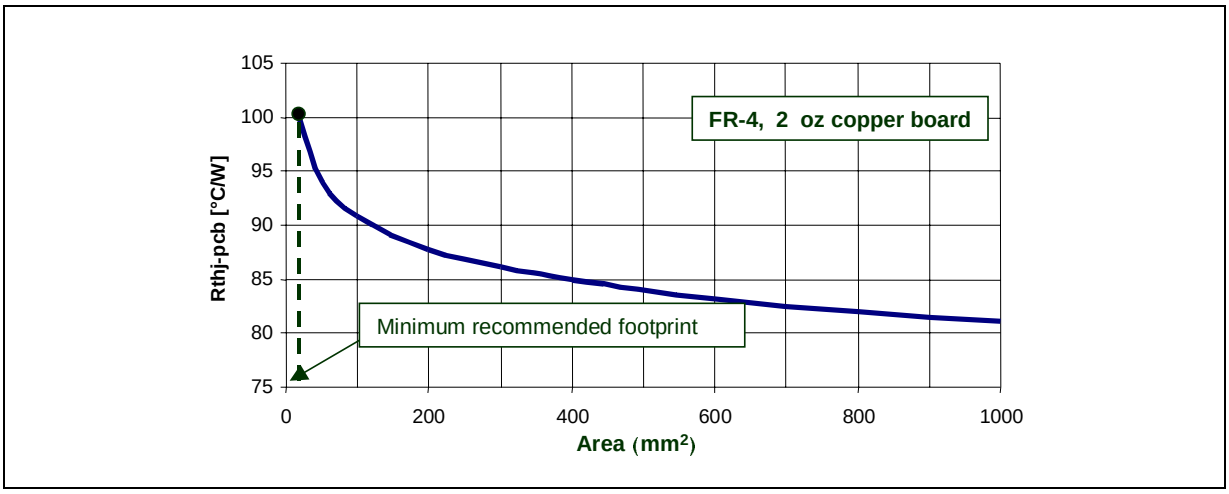


Figure 24 shows the $R_{THJ\text{-}PCB}$ versus drain pad area from minimum recommended footprint to $10cm^2$, for $t \leq 10s$ as power pulse:

Figure 24: R_{THJ_PCB} versus drain pad area for TSSOP8



For the minimum recommended footprint the thermal resistance value is about $R_{THJ\text{-}PCB}$ = 100 °C/W and the maximum allowable power dissipation results:

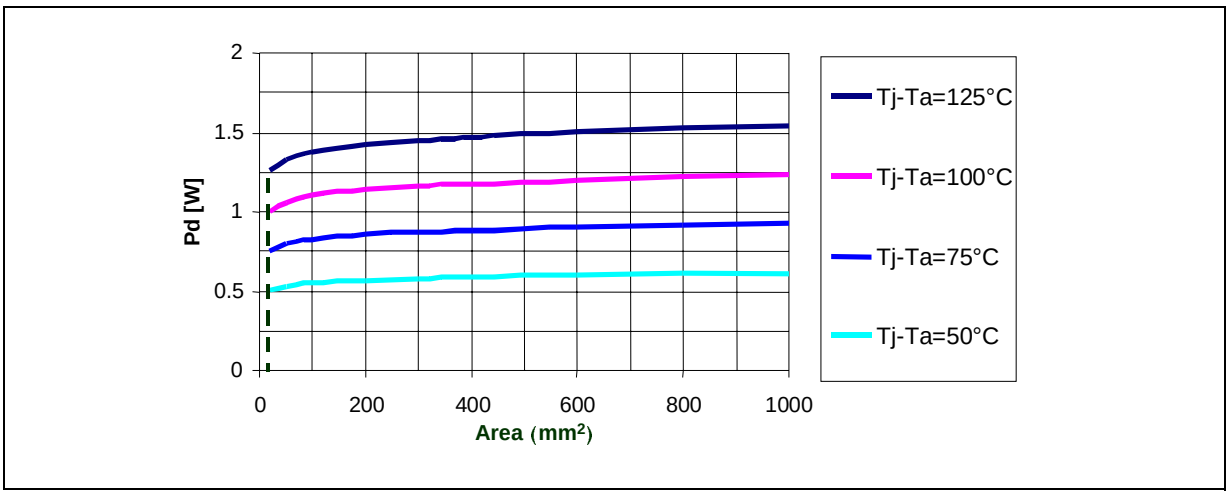
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{100} = 1.25W \qquad (T_{JMAX} = 150°C,\ T_C = 25°C)$$

For a drain pad area of $1in^2$ (about $600mm^2$) we obtain:

$$R_{THJ-PCB} = 83.5\,{}^{\circ C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 1.5W$$

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

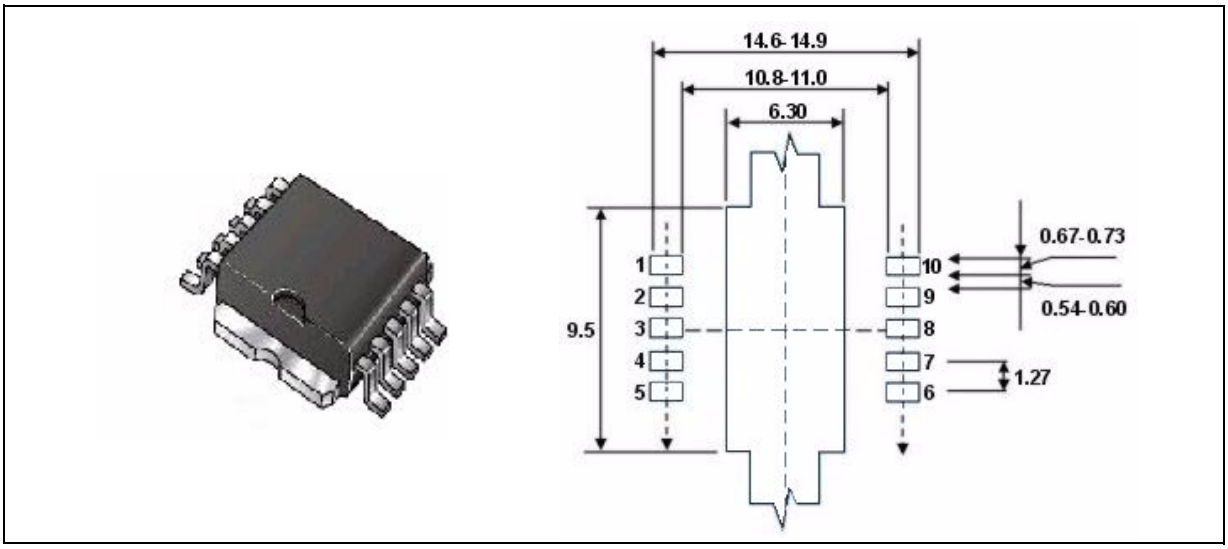
Figure 25: Maximum allowable power dissipation versus drain pad area



10. PowerSO-10™

Surface mounting packages, by their very nature are restricted to smaller footprints. Power devices need larger footprints to dissipate heat. PowerSO-10 is an optimized balance between these two conflicting requirements. Figure 26 shows PowerSO-10 with its minimum recommended footprint.

Figure 26: PowerSO-10™ package and its minimum recommended footprint (all dimensions are in mm)

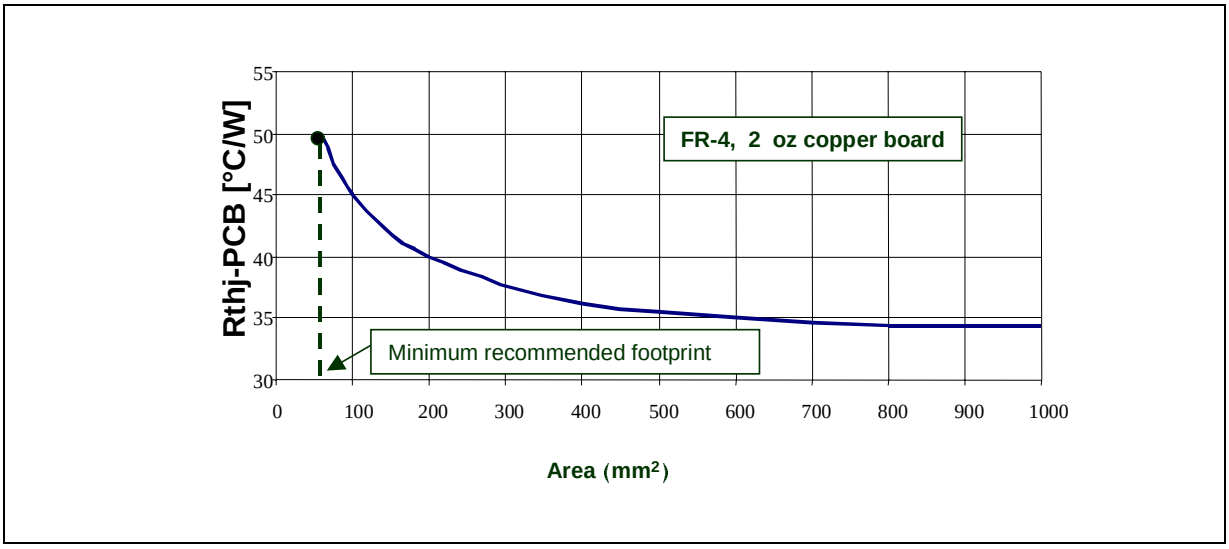


A 10-pin DIP package was manufactured also for use in intelligent power devices, which require many leads. Discrete can use high pin count packages to distribute the current through the power circuit.

The maximum die-size is the same as TO-220 and its derived versions, D^2PAK and I^2PAK. The lowering of the PowerSO-10 height results in about a 37% decrease in total volume of the package, while the spreader area remains large. Not only does this result in a lower package cost, but also from a high frequency standpoint, low height and less inductance are two big advantages.

The use of epoxy FR-4 boards is quite common in through-hole techniques; for surface mounting techniques, however, its poor thermal conduction means that it is not possible to benefit from the outstanding thermal performance of PowerSO-10. One way to improve the thermal conduction is the use of large heat spread areas at the copper layer of the PC board. This leads to a reduction of thermal resistance from 35-38°C/W for 3 to 6cm^2 on board heatsink (see figure 27).

Figure 27: R_{THJ_PCB} versus drain pad area for PowerSO-10



For the recommended footprint (about 60mm^2) the value is $R_{THJ\text{-}PCB}$ = 50°C/W and the maximum allowable power dissipation results:

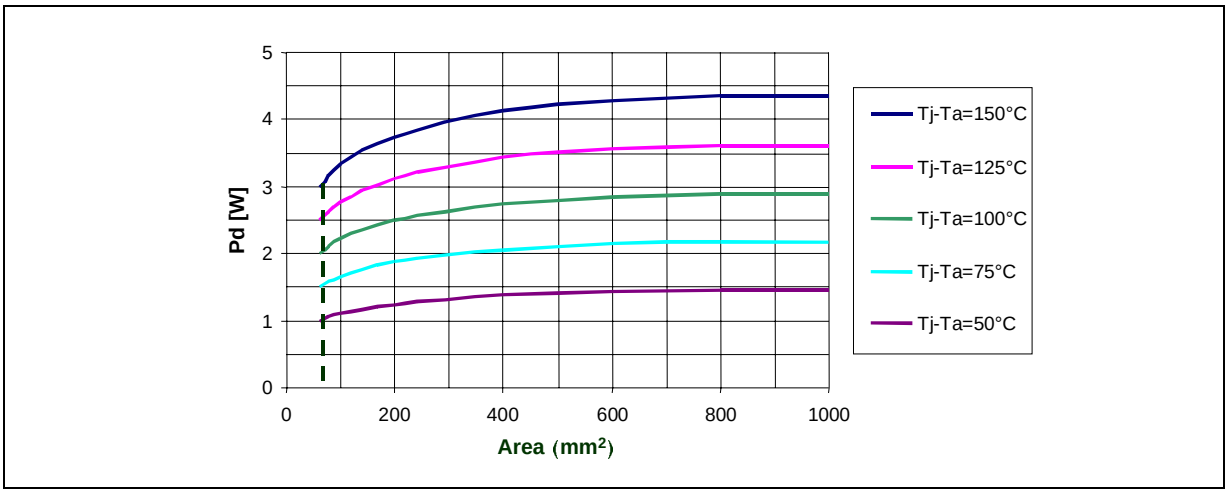
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{150}{50} = 3W \quad (T_{JMAX} = 175°C, T_C = 25°C)$$

By increasing the area of the drain pad, the power dissipation can be increased. For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 35\,{}^{°C}\!/_{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4.3W$$

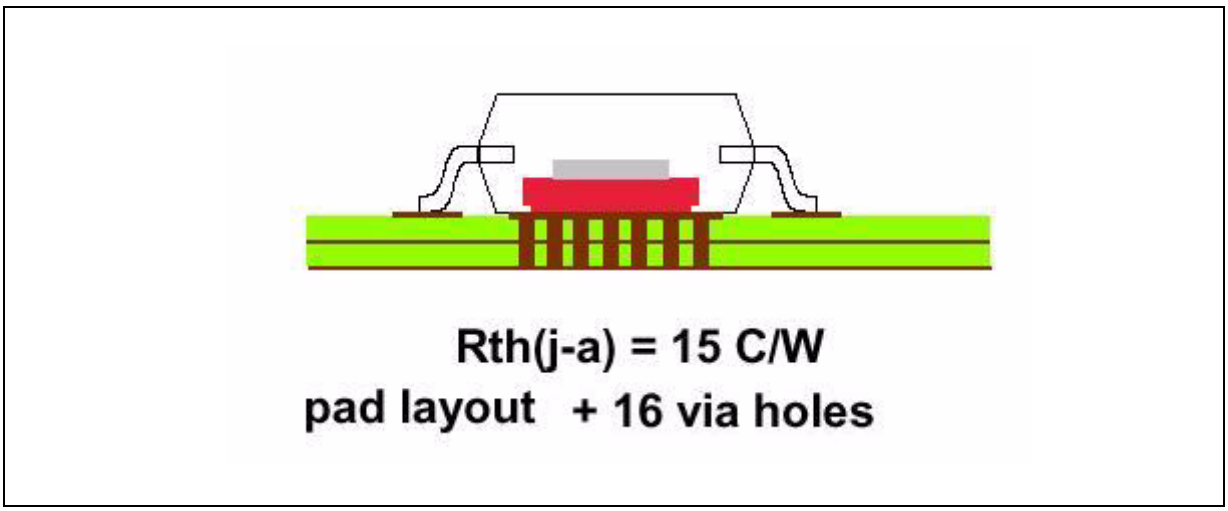
The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values.

Figure 28: Maximum allowable power dissipation versus drain pad area



Use of copper-filled through-holes with conventional FR-4 techniques increases the metallization and decreases thermal resistance accordingly. Using a configuration with 16 holes under the spreader of the package with a pitch of 1.8mm and a diameter of 0.7mm, the thermal resistance (junction - heats ink) can be reduces to 15 °C/W (see figure 29)

Figure 29: Mounting on FR-4 using copper-filled through holes for heat transfer



Apart from the thermal advantage, this solution allows the use of multi-layer boards. However, the limitations of this conventional material prevent its use in very high power, high current circuits.

The thermal characteristics of PowerSO-10 are comparable with those of the D^2PAK, as shown in the next table.

Table 1: Comparison between PowerSO-10™ and D2PAK

Comparison PowerSO-10 andTO-220 SMD-version

DESCRIPTION	TO-220 SMD-version	PowerSO-10	DELTA
Footprint Area in mm^2	203	141	-30%
Heat Spreader in mm^2	50 to 60	67	+10% to 30%
$R_{th(j-c)}$ in °C/W	0.8	0.8	equal
Chip Size in $mils^2$	180x220	180x220	equal
Total Volume in mm^3	597	373	-37%
Package Height in mm	4.5	3.5	-22%

Steady-state thermal resistance (junction-case) studies show approximately 0.8°C/W for both PowerSO-10 and D^2PAK, but PowerSO-10 exhibits 30% less footprint area than D^2PAK. The test vehicle used is a MOSFET with a die-size of about 32,000 $mils^2$ (about 20.6mm^2).
Furthermore, since PowerSO-10 has been designed solely to be an SMD, symmetry in the x- and y-planes gives the package excellent weight balance. Moreover, PowerSO-10 offers the unique opportunity to easily control the flatness and quality of the soldering process. Both the top and the bottom soldered edges of the package are accessible for visual inspection. PowerSO-10 is a package "designed for testability". Co-planarity between the substrate and the package can be easily verified.

11. SMD PACKAGES COMPARISON

Thermal performances for SMD packages are summarized in the following table:

Table 2: Thermal performances for SMD packages

Package	Package shaping area [mm^2]	Recommended Min. Footprint area [mm^2]	T_{JMAX} [°C]	$R_{THJ-PCB}$ [°C/W] (*)	$R_{THJ-PCB}$ [°C/W] (**)	P_D [W] (*)
D^2PAK	210	120	175	34.0	42.0	4.4
PowerSO-10	140	60	175	35.0	50.0	4.3
DPAK	80	45	175	50.0	62.0	3.0
PowerFLAT 5x5	25	15	150	31.2	60.0	4.0
PowerFLAT 6x5	30	23	150	31.2	60.0	4.0
SOT-223	50	15	150	38.0	56.6	3.3
PowerSO-8	30	23	150	42.0	56.6	3.0
SO-8	30	23	150	50.0	100	2.5
TSSOP8	20	15	150	83.5	100	1.5

(*) When mounted on 1 in^2 FR-4 board, 2 oz Cu, tp < 10s for small packages.
(**) When mounted on minimum recommended footprint.

First of all we have to note that the maximum allowable power dissipation for the newest small packages (PowerFLAT and PowerSO-8) is quite similar to that for DPAK but require approximately half the PC board space. This advantage is more impressive if we note that the max die housed in PowerFLAT (6x5 version) is about 30% greater than those in DPAK. Also SOT-223 has a high thermal performance, but the max die housed is half that of those for DPAK and PowerSO-8.
Since several automotive applications require devices rated at 175 °C, up to now only the standard SMD packages (D^2PAK, DPAK, PowerSO-10) are automotive graded. These packages have been designed to withstand the high stresses in under-hood applications.

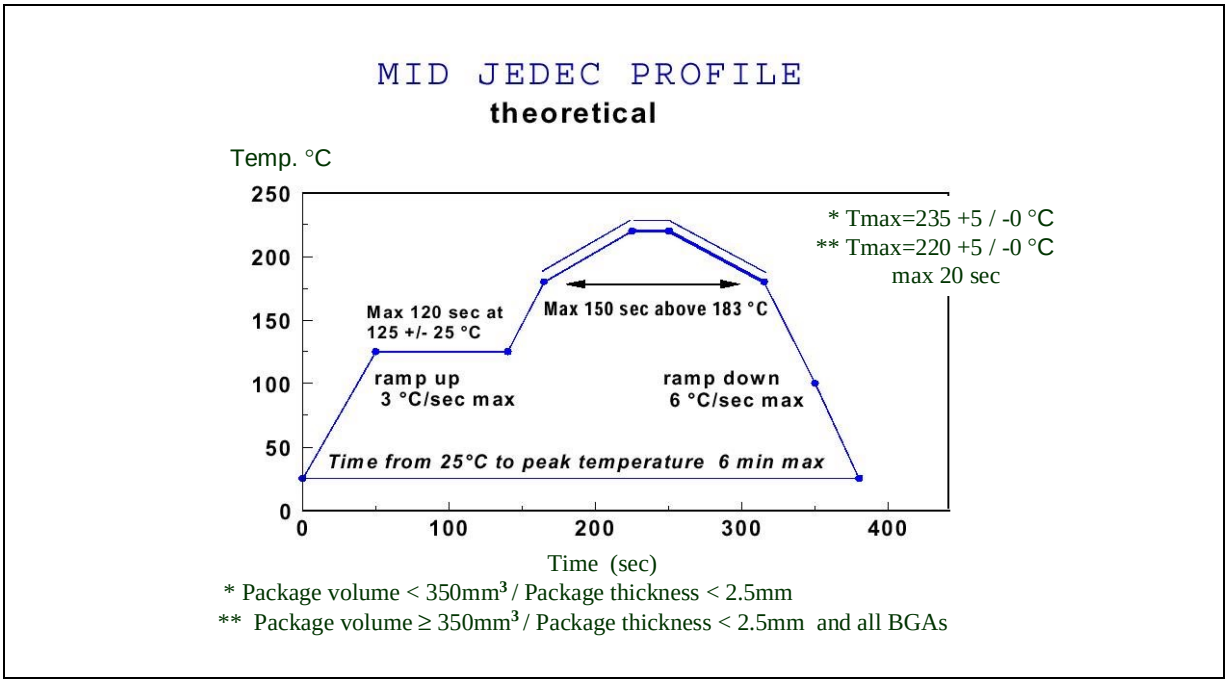
12. SOLDERING PROFILE

The most commonly used techniques for mounting SMD packages to the PCB are infrared and vapor phase reflow. These are preferred over wave soldering because this typically involves increased heating rate, higher temperatures and increased flux exposure.

The infrared reflow technique involves thermal energy supplied via lamps radiating at given wavelengths. Therefore, the amount of thermal energy absorbed varies with board size, component size, component orientation, and materials used. The surface temperature of the board is not uniform and the board edges tend to run 10°C to 20°C higher than the center.

The vapor phase reflow technique uses vapor from a boiling inert fluorocarbon liquid. The heat of condensation provides a thermal constraint dependent on the liquid selected. With essentially no temperature gradient across the surface of the board, component location design rules even for heating is not significant compared to infrared reflow.
The theoretical solder reflow temperature profile used, and the temperatures and time duration are shown in the next figure:

Figure 30: Soldering profile, recommended reflow oven profile



Any solder temperature profile should be within these limits. The soldering process causes considerable thermal stress to a semiconductor component. This has to be minimized to ensure a reliable and extended lifetime of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, in order to minimize the thermal stress to which the devices are subject, the device should always be preheated (max 120sec at 125 $\pm$ 25°C). Soldering a device without preheating can cause excessive thermal shock and stress that can result in damage to the device.

Voids pose a difficult reliability problem for large surface mount devices. Pockets of air under the package result in poor thermal contact and the resulting high thermal resistance leads to complete failure. Because of co-planarity problems, weight balance is critical.

The quality of the solder joints is very important for two reasons: firstly, poor quality solder joints result directly in poor reliability, and secondly, solder thickness significantly affects the thermal resistance. Thus a tight control of this parameter results in thermally efficient and reliable solder joints. Thermal conductivity in the region of 0.5°C/W can easily be lost through uneven solder and poor co-planarity of tabs and leads.

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