Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

FAIRCHILD SEMICONDUCTOR®

October 2006

FHP3130, FHP3230, FHP3430 Single, Dual, and Quad, High-Speed, 2.7V to 12V, Rail-to-Rail Amplifiers

Features at ±5V

- 2.5mA supply current per amplifier
- 0.008%/0.01° differential gain/phase
- 10MHz 0.1dB bandwidth
- Output voltage range at R_L = 150Ω: -4.8V to 4.8V
- Input includes negative rail
- 110V/μs slew rate
- ±100mA output current
- 17nV/√Hz input voltage noise
- >100dB PSRR, CMRR, and open-loop gain
- FHP3130 – improved replacement for KM4100
- FHP3230 – improved replacement for KM4200
- FHP3130 lead-free package options (SOT23-5, SOIC-8)
- FHP3230 lead-free package options (MSOP-8, SOIC-8)
- FHP3430 lead-free package options (TSSOP-14, SOIC-14)
- RoHS compliant
- Fully specified at +3V, +5V, and ±5V supplies

Applications

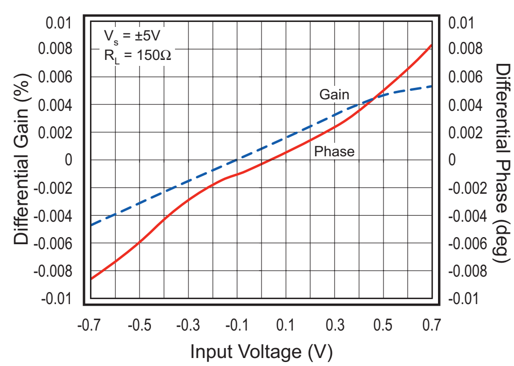
- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- Portable/battery-powered applications
- Twisted-pair driver
- Video driver

Description

The FHP3130 (single), FHP3230 (dual), and FHP3430 (quad) are low-cost, high-performance, voltage feedback amplifiers that consume only 2.5mA of supply current per channel, while providing ±100mA of output current. These amplifiers are designed to operate from 2.7V to 12V (±6V) supplies. The common mode voltage range includes the negative rail and the output provides rail-to-rail performance.

The FHP3130, FHP3230, and FHP3430 are designed on a complimentary bipolar process and provide 170MHz of bandwidth and 110V/μs of slew rate at a supply voltage of ±5V. The combination of low power, rail-to-rail performance, low-voltage operation, and tiny package options make these amplifiers well suited for use in many general-purpose, high-speed applications.

These amplifiers also provide excellent video specifications. They offer extremely low differential gain and phase (0.008%/0.01°) and 0.1dB gain flatness to 10MHz for superb standard definition video performance. Their output drive capability effortlessly supports four video loads.

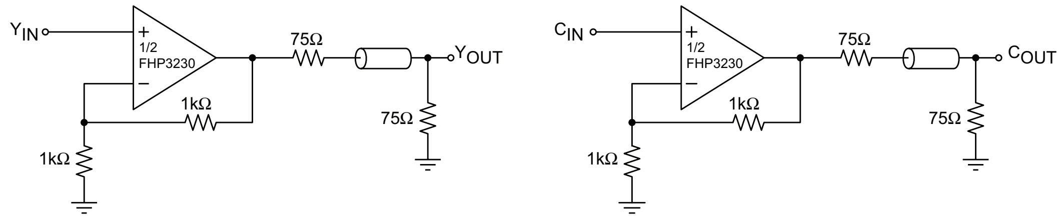


Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
FHP3130IS5X	SOT23-5	Yes	-40°C to +85°C	Reel
FHP3130IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
FHP3230IMU8X	MSOP-8	Yes	-40°C to +85°C	Reel
FHP3230IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
FHP3430IMTC14X	TSSOP-14	Yes	-40°C to +85°C	Reel
FHP3430IM14X	SOIC-14	Yes	-40°C to +85°C	Reel

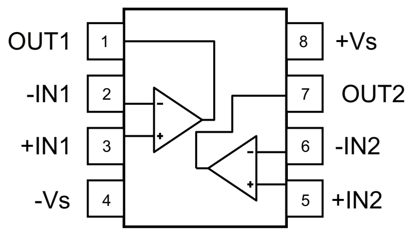
Moisture sensitivity level for all parts is MSL-1.

Typical Application - YC Video Line Driver

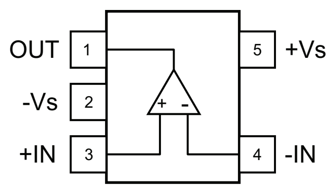


Pin Configurations

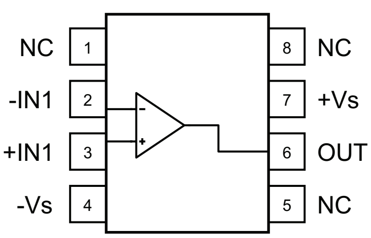
FHP3230
SOIC/MSOP



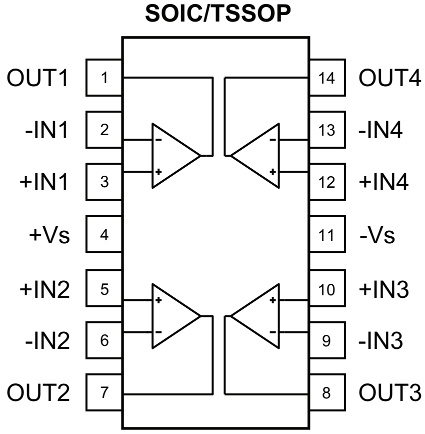
FHP3130
SOT23



FHP3130
SOIC



FHP3430
SOIC/TSSOP



Pin Assignments

FHP3230

Pin #	Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative Input, channel 1
3	+IN1	Positive Input, channel 1
4	-Vs	Negative supply
5	+IN2	Positive Input, channel 2
6	-IN2	Negative Input, channel 2
7	OUT2	Output, channel 2
8	+Vs	Positive supply

FHP3130

Pin # SOT/SOIC	Name	Description
1 / 6	OUT	Output
2 / 4	-Vs	Negative supply
3 / 3	+IN	Positive Input
4 / 2	-IN	Negative Input
5 / 7	+Vs	Positive supply
na / 1, 5, 8	NC	No Connect

FHP3430

Pin #	Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative Input, channel 1
3	+IN1	Positive Input, channel 1
4	+Vs	Positive supply
5	+IN2	Positive Input, channel 2
6	-IN2	Negative Input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative Input, channel 3
10	+IN3	Positive Input, channel 3
11	-Vs	Negative supply
12	+IN4	Positive Input, channel 4
13	-IN4	Negative Input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Parameter	Min.	Max.	Unit
Supply Voltage	0	13.3	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance				
8-Lead SOIC(1)		155		°C/W
8-Lead MSOP(1)		246		°C/W
5-Lead SOT23(1)		296		°C/W
14-Lead TSSOP(1)		140		°C/W
14-Lead SOIC(1)		128		°C/W

Notes:
1. Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	FHP3130		FHP3230		FHP3430	
Package	SOT23	SOIC	SOIC	MSOP	SOIC	TSSOP
Human Body Model (HBM)	3.5kV	>4kV	3.5kV	3.5kV	3kV	5kV
Charged Device Model (CDM)	>2kV	>2kV	2kV	1.5kV	2kV	1.5kV

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.7		12	V

Electrical Characteristics at +3V

T_A = 25°C, V_s = 3V, R_L = 2kΩ to V_s/2, G = 2, R_f = R_g =1kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		160		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BW_{Ls}	Full Power Bandwidth	G = +2, V_{OUT} = 1V_{pp}		45		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150kΩ, V_{OUT} = 0.2V_{pp}		11.5		MHz
GBWP	Gain Bandwidth Product	G = +6, V_{OUT} = 0.2V_{pp}		60		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		90		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		90		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		50		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		50		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz, R_L = 100Ω, G = -1		50		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			-1.8		µA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current			0.01		µA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifier			2.5		mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 2		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_s/2, G = -1		0.05 to 2.95		V
		RL = 150Ω to V_s/2, G = -1		0.1 to 2.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_s/2		±120		mA

Electrical Characteristics at +5V

$T_A = 25°C$, $V_s = 5V$, $R_L = 2k\Omega$ to $V_s/2$, $G = 2$, $R_f = R_g = 1k\Omega$; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		165		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BW_{Ls}	Full Power Bandwidth	G = +2, V_{OUT} = 2V_{pp}		30		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150kΩ, V_{OUT} = 0.2V_{pp}		18		MHz
GBWP	Gain Bandwidth Product	G = +6, VOUT = 0.2V_{pp}		60		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		90		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		105		V/μs
Distortion / Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		56		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		65		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		55		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), R_L = 150Ω, AC-coupled into 220μF, V_s = ±2.5V		0.02		%
DP	Differential Phase	NTSC (3.58MHz), R_L = 150Ω, AC-coupled into 220μF, V_s = ±2.5V		0.04		°
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			5		μV/°C
I_b	Input Bias Current			-1.8		μA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current			0.01		μA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifer			2.5		mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 4		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to $V_s/2$		0.05 to 4.95		V
		R_L = 150Ω to $V_s/2$		0.1 to 4.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = $V_s/2$		±120		mA

Electrical Characteristics at ±5V

T_A = 25°C, V_s = ±5V, R_L = 2kΩ to GND, G = 2, R_f = R_g =1kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		170		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BWLs	Full Power Bandwidth	G = +2, V_{OUT} = 2V_{pp}		30		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150Ω, V_{OUT} = 0.2V_{pp}		10		MHz
GBWP	Gain Bandwidth Product	G = +6, V_{OUT} = 0.2V_{pp}		60		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		90		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		110		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		65		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		65		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		54		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), R_L = 150Ω, AC-coupled into 220µF		0.008		%
DP	Differential Phase	NTSC (3.58MHz), R_L = 150Ω, AC-coupled into 220µF		0.01		°
DC Performance						
V_{IO}	Input Offset Voltage(1)		-6	1	6	mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current(1)		-4	-1.8		µA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current(1)		-0.8	0.01	0.8	µA
PSRR	Power Supply Rejection Ratio(2)	DC	80	100		dB
A_{OL}	Open-Loop Gain(2)	DC, R_L = 150Ω	80	100		dB
I_S	Supply Current per Amplifier(1)			2.5	3.5	mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-5 to 4		V
CMRR	Common Mode Rejection Ratio(2)	DC, V_{CM} = -5V to 3.5V	75	100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ		±4.95		V
		R_L = 150Ω(1)	-4.65	±4.7	4.65	V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0V		±120		mA

Notes:
1. 100% tested at 25°C
2. Min/max guaranteed by design/characterization.

Typical Performance Characteristics

$T_A = 25°C$, $V_s = 5V$, $R_L = 2k\Omega$ to $V_s/2$ for $V_s = 5V$ and 3V, $R_L = 2k\Omega$ to GND for $V_s = \pm5V$, G = 2, $R_f = R_g = 1k\Omega$; unless otherwise noted.

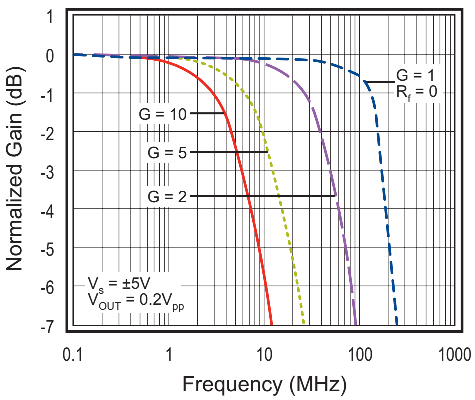


Figure 1. Non-Inverting Freq. Response (±5V)

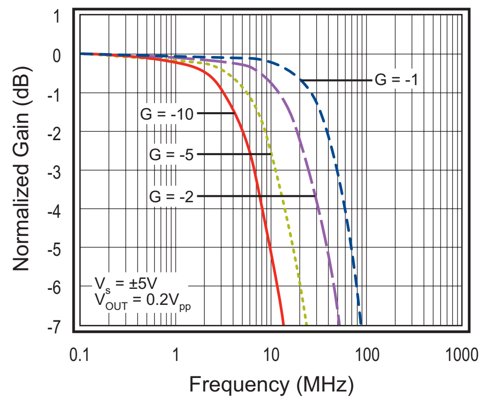


Figure 2. Inverting Freq. Response (±5V)

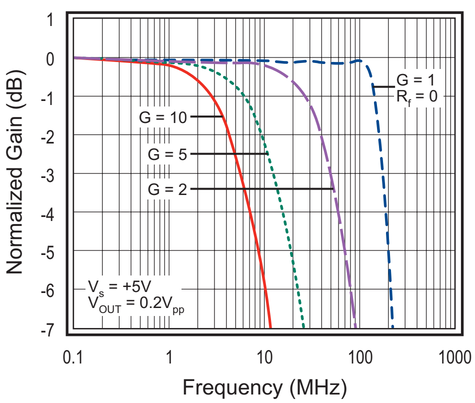


Figure 3. Non-Inverting Freq. Response (+5V)

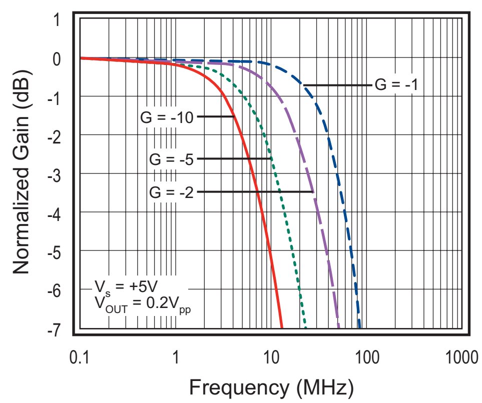


Figure 4. Inverting Freq. Response (+5V)

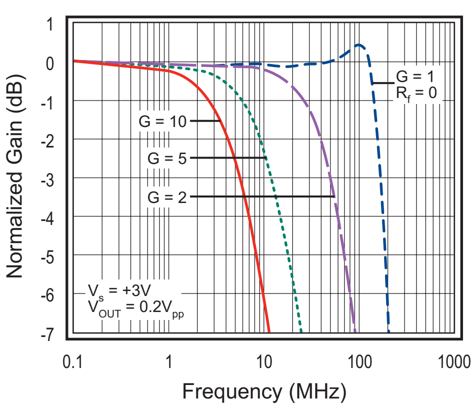


Figure 5. Non-Inverting Freq. Response (+3V)

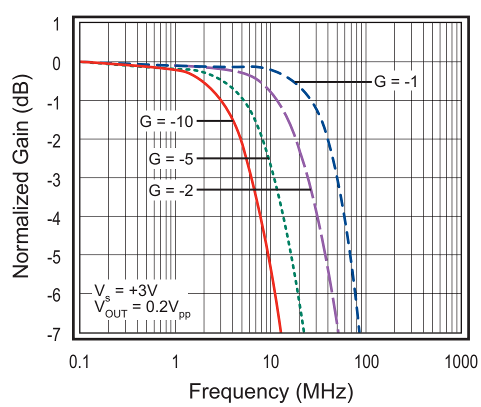


Figure 6. Inverting Freq. Response (+3V)

Typical Performance Characteristics - Continued

T_A = 25°C, V_s = 5V, R_L = 2kΩ to V_s/2 for V_s = 5V and 3V, R_L = 2kΩ to GND for V_s = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

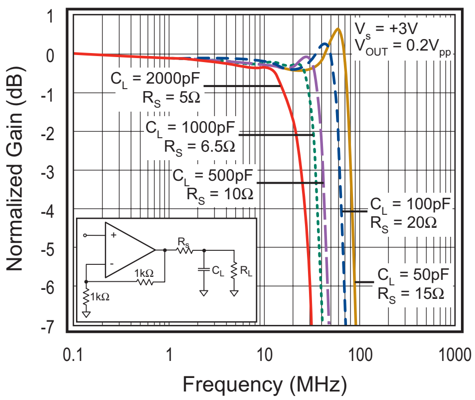


Figure 7. Frequency Response vs. C_L (+3V)

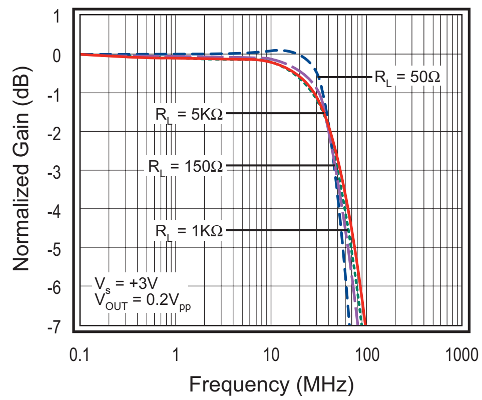


Figure 8. Frequency Response vs. R_L (+3V)

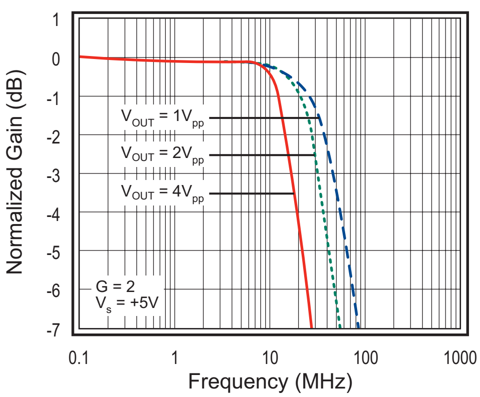


Figure 9. Large Signal Freq. Response (±5V)

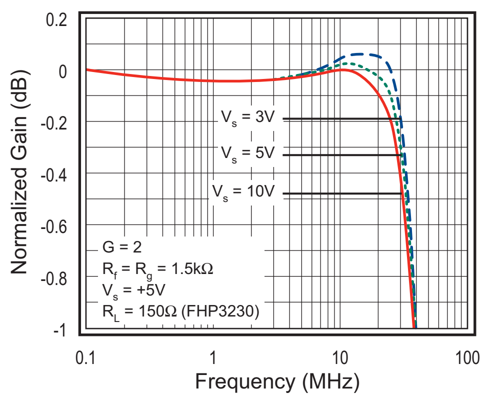


Figure 10. Gain Flatness

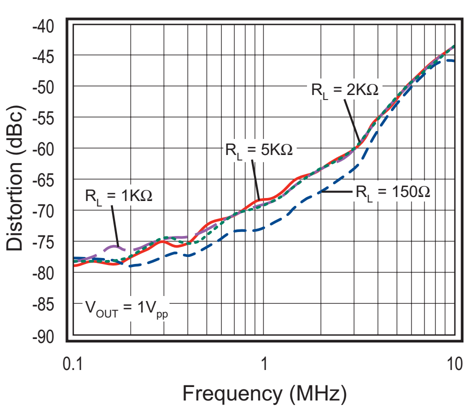


Figure 11. HD2 vs. R_L (+3V)

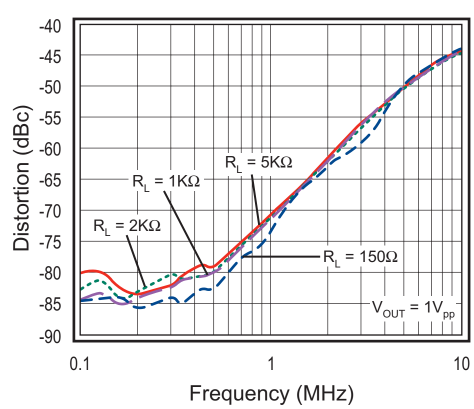


Figure 12. HD2 vs. R_L (+3V)

Typical Performance Characteristics - Continued

T_A = 25°C, V_s = 5V, R_L = 2kΩ to V_s/2 for V_s = 5V and 3V, R_L = 2kΩ to GND for V_s = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

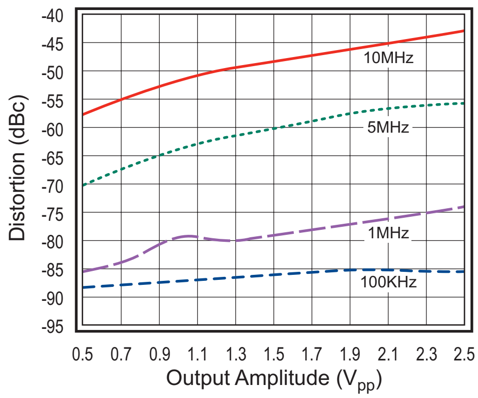


Figure 13. HD2 vs. V_{OUT} (+5V)

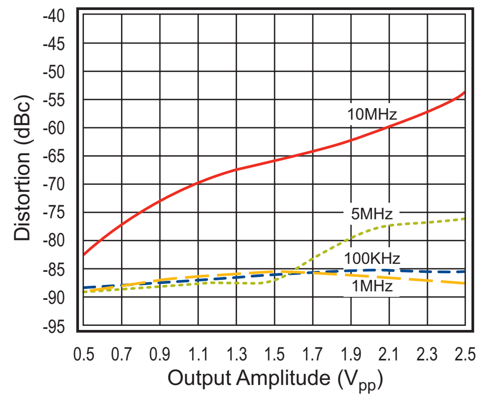


Figure 14. HD3 vs. V_{OUT} (+5V)

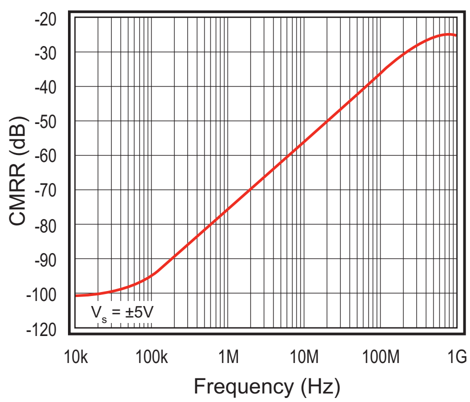


Figure 15. CMMR vs. Frequency

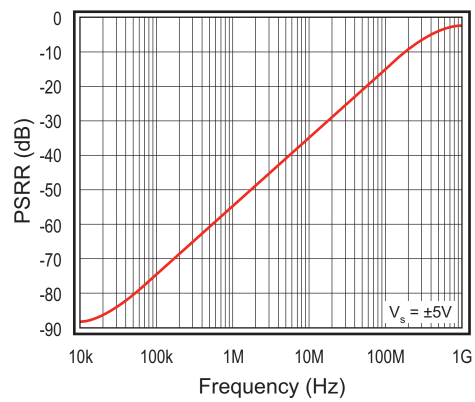


Figure 16. PSRR vs. Frequency

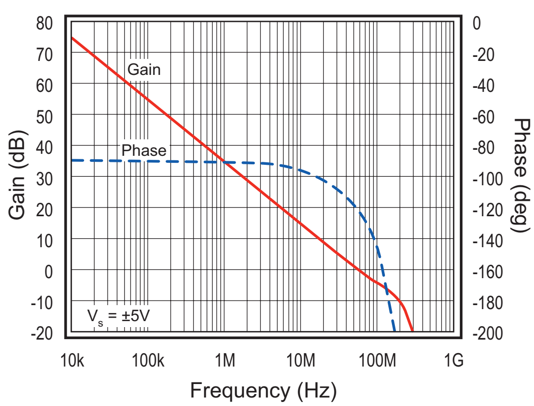


Figure 17. Open-Loop Gain and Phase

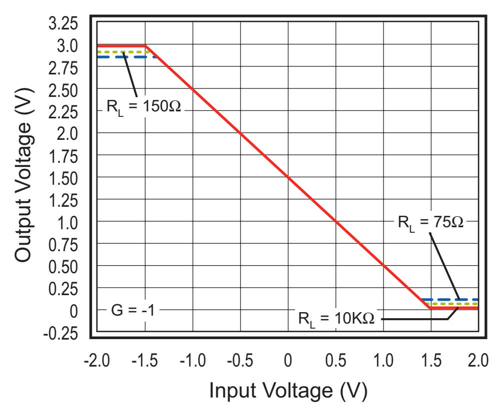


Figure 18. Output Swing vs. Load (+3V)

Typical Performance Characteristics - Continued

T_A = 25°C, V_s = 5V, R_L = 2kΩ to $V_s/2$ for V_s = 5V and 3V, R_L = 2kΩ to GND for V_s = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

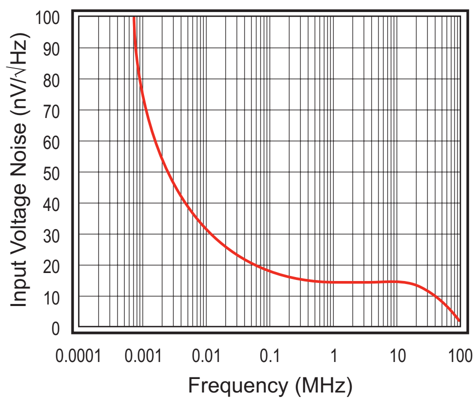


Figure 19. Input Voltage Noise (+3V)

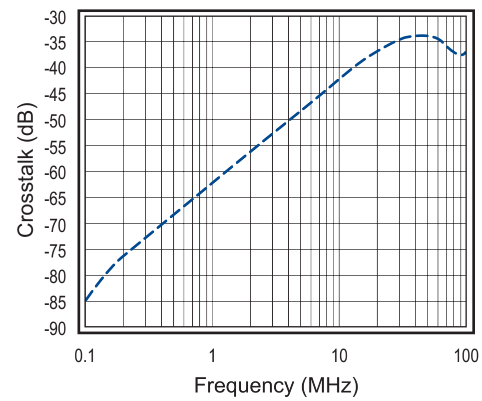


Figure 20. Crosstalk vs. Frequency (+3V)

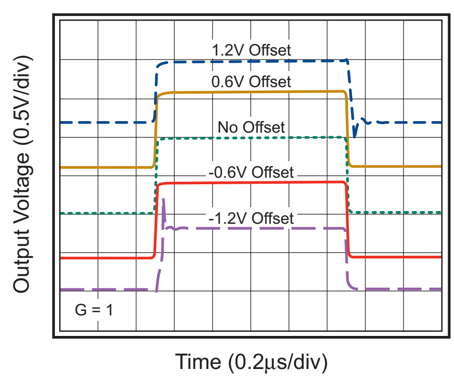


Figure 21. Pulse Resp. vs. Common Mode Voltage

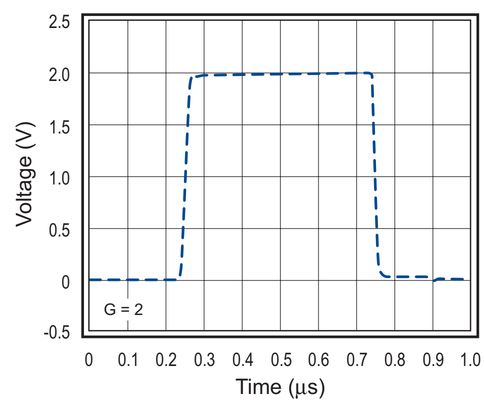


Figure 22. Large Signal Pulse Response (+3V)

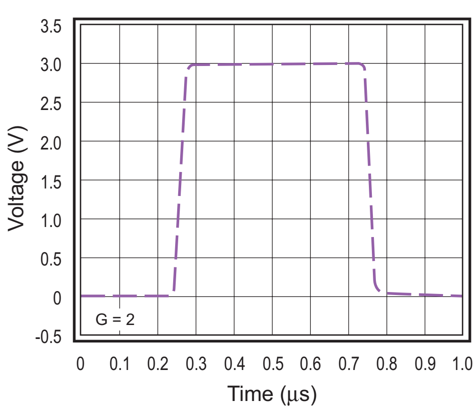


Figure 23. Large Signal Pulse Response (+5V)

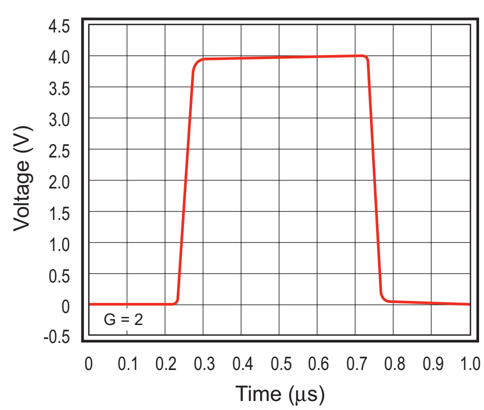


Figure 24. Large Signal Pulse Response (±5V)

Typical Performance Characteristics - Continued

T_A = 25°C, V_s = 5V, R_L = 2kΩ to V_s/2 for V_s = 5V and 3V, R_L = 2kΩ to GND for V_s = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

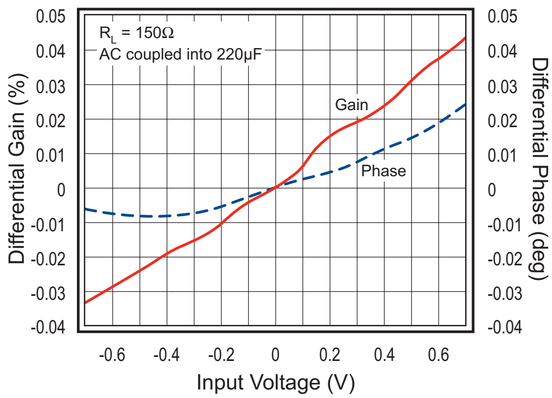


Figure 25. Differential Gain and Phase (±2.5)

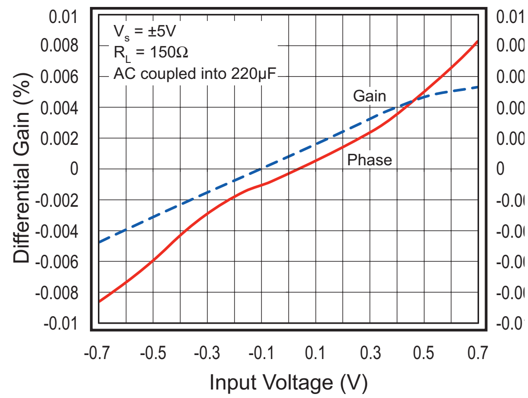


Figure 26. Differential Gain and Phase (±5)

Application Information

Driving Capacitive Loads

The FREQUENCY RESPONSE VS. C_L plot in Figure 7, illustrates the response of the FHP3230 Family. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 27, improves stability and settling performance. R_S values in the FREQUENCY RESPONSE VS. C_L plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S.

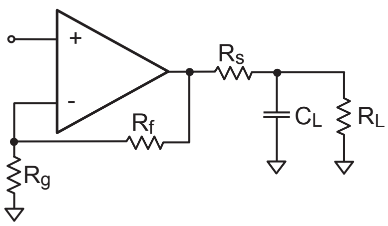


Figure 27. Typical Topology for Driving Capacitive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

The FHP3130, FHP3230, and FHP3430 are short-circuit protected; however, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

$$\text{Power Dissipation} = I_s * (V_s + - V_s -) + (V_s + - V_{o(RMS)}) * I_{OUT(RMS)}$$

where I_S is the supply current, V_{S+} is the positive supply pin voltage, V_{S-} is the negative supply pin voltage, $V_{o(RMS)}$ is the RMS output voltage, and $I_{OUT(RMS)}$ is the RMS output current delivered to the load.

Follow the maximum power derating curves shown in Figure 28 below to ensure proper operation.

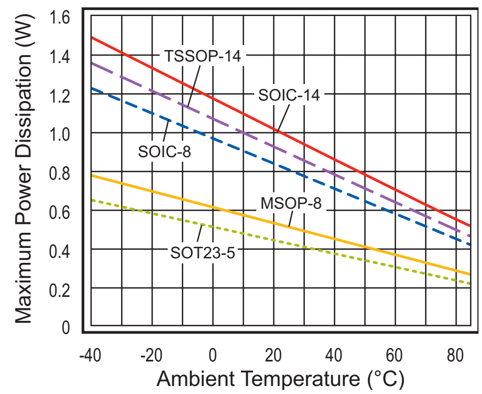


Figure 28. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3130/3230/3430 typically recovers in less than 50ns from an overdrive condition. Figure 29 shows the FHP3230 in an overdriven condition.

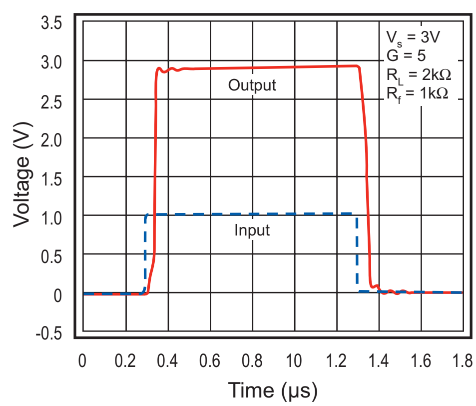


Figure 29. Overdrive Recovery

Composite Video Summer

The bandwidth and differential gain/phase performance of the FHP3130/3230/3430 amplifiers make them well suited for video applications. Figure 30 shows a typical Composite Video Summer. The high output current capability allows for driving multiple video loads. Figure 31 shows the resulting differential gain/phase of this three-amplifier configuration driving four video loads, or 37.5Ω.

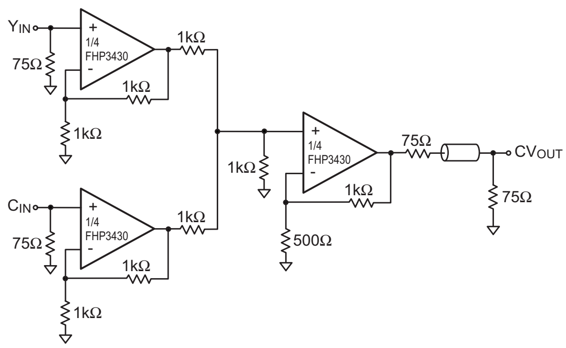


Figure 30. Typical Composite Video Summer

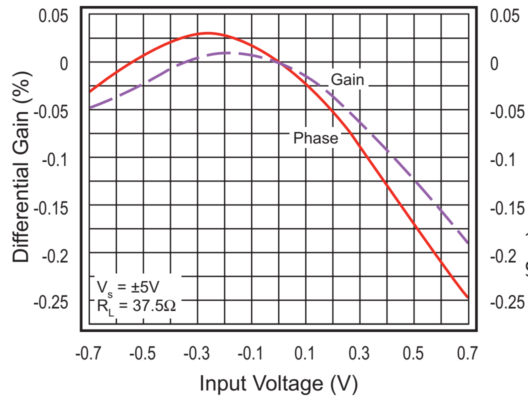


Figure 31. DG/DP of CV Summer Driving Four Video Loads

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild has evaluation boards to guide high-frequency layout and aid device testing and characterization. Follow the guidelines below as a basis for high-frequency layout:

- Include 6.8μF and 0.01μF ceramic capacitors.
- Place the 6.8μF capacitor within 0.75 inches of the power pin.
- Place the 0.01μF capacitor within 0.1 inches of the power pin.
- Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown below for more information.

Evaluation Board Information

The following evaluation boards are available to aid testing and layout of these devices:

Evaluation Board	Products
KEB002	FHP3130IS5X
KEB003	FHP3130IM8X
KEB010	FHP3230IMU8X
KEB006	FHP3230IM8X
KEB012	FHP3430IMTC14X
KEB018	FHP3430IM14X

Evalutaion Board Schematics

Evaluation board schematics and layouts are shown in Figures 32 – 46. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4 if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

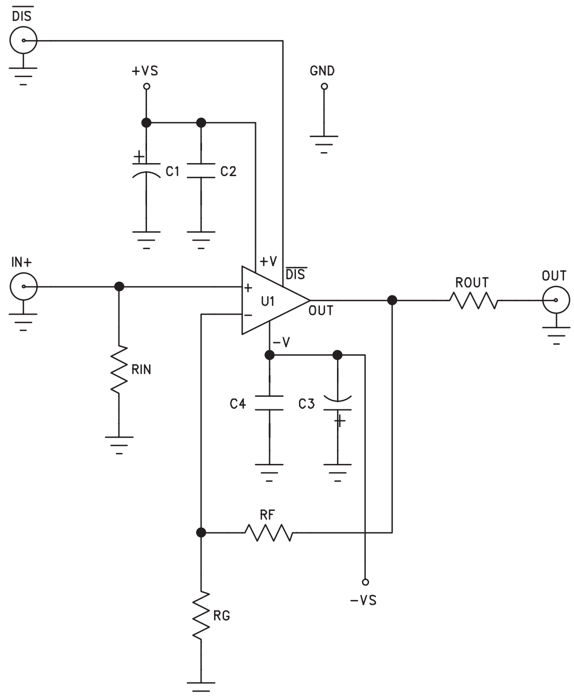


Figure 32. FHP3130 KEB002/KEB003 Schematic

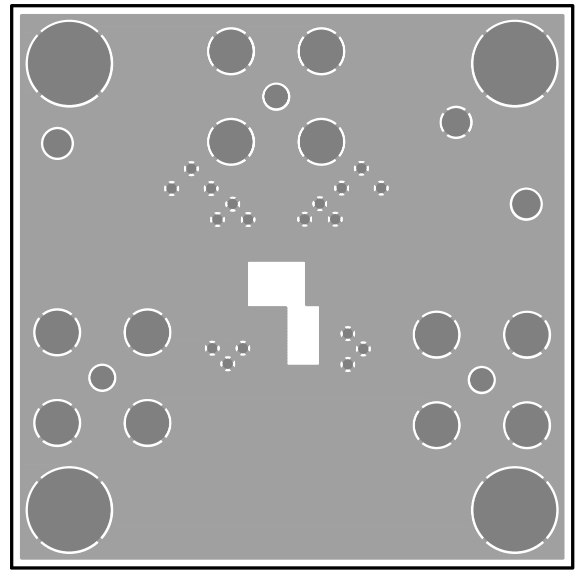


Figure 34. FHP3130 KEB002 (Bottom-side)

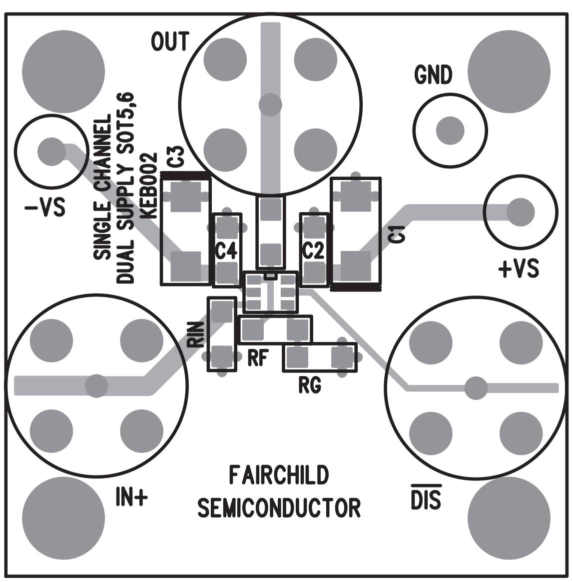


Figure 33. FHP3130 KEB002 (Top-side)

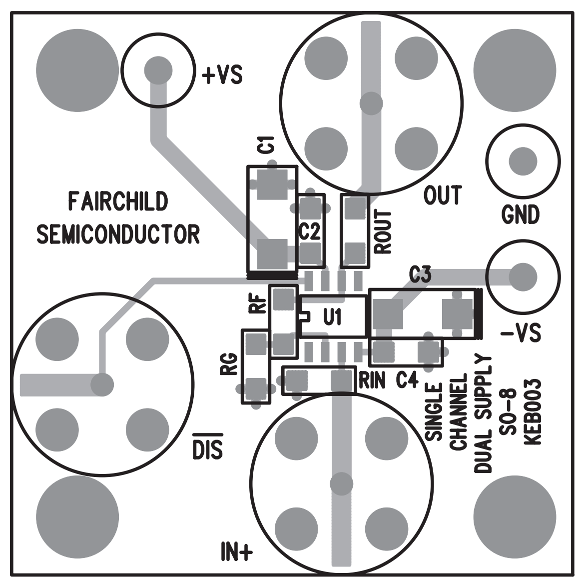


Figure 35. FHP3130 KEB003 (Top-side)

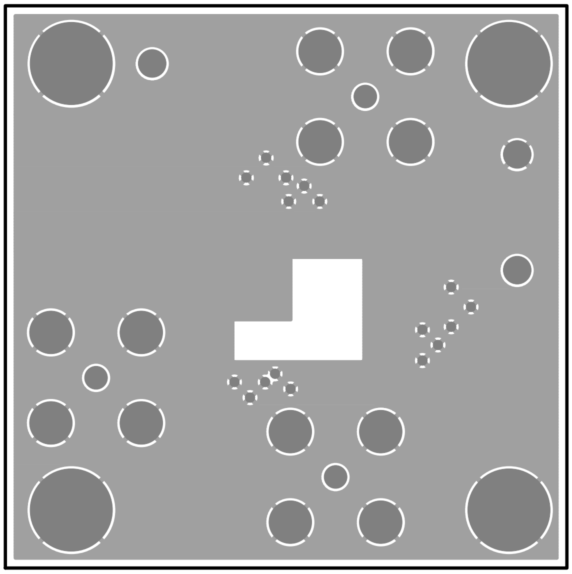


Figure 36. FHP3130 KEB003 (Bottom-side)

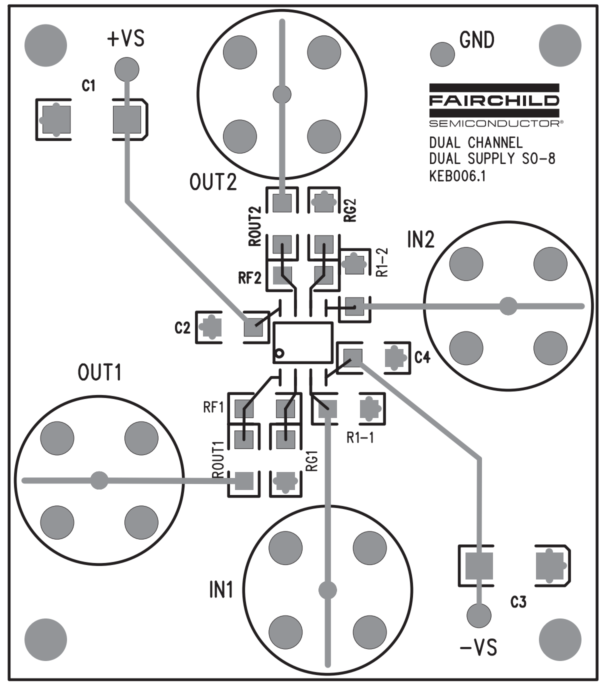


Figure 38. FHP3230 KEB006 (Top-side)

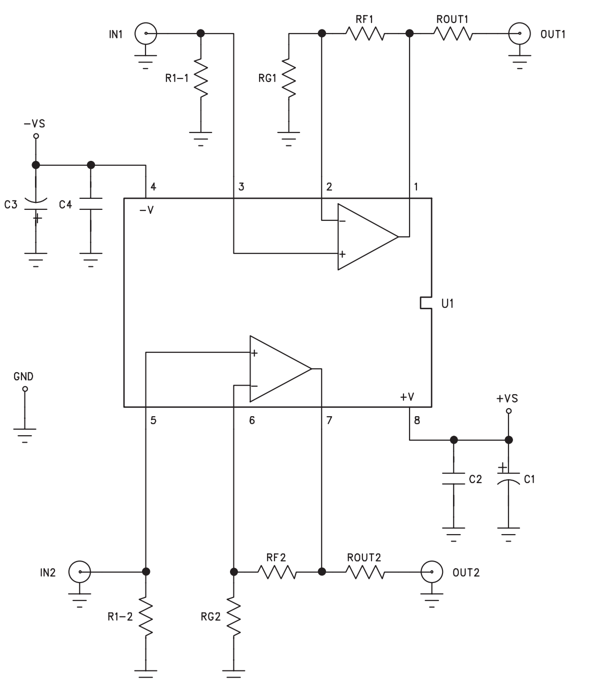


Figure 37. FHP3230 KEB006/KEB010 Schematic

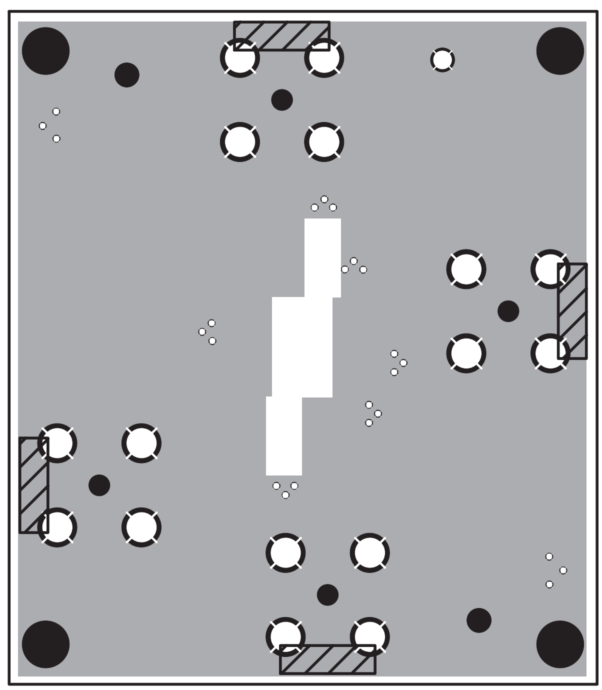


Figure 39. FHP3230 KEB006 (Bottom-side)

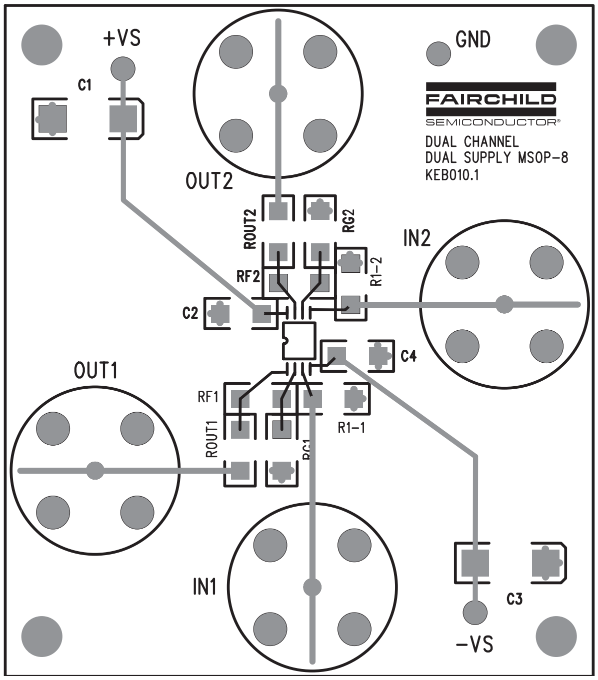


Figure 40. FHP3230 KEB010 (Top-side)

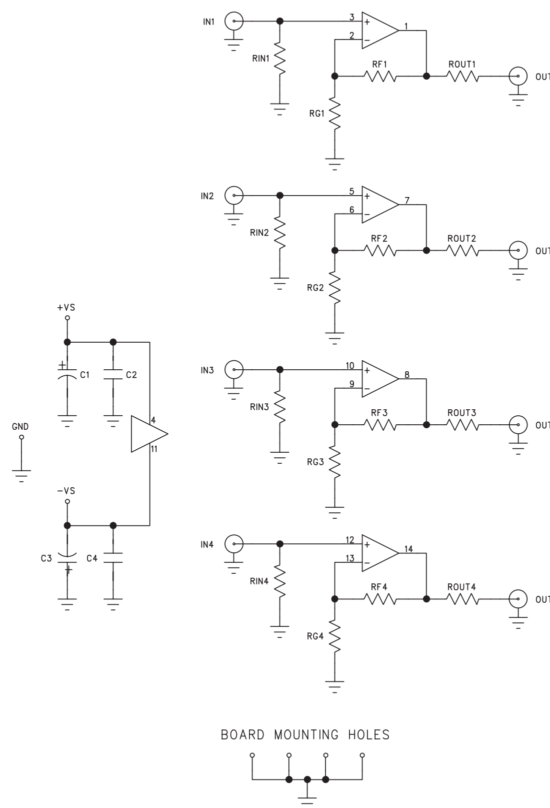


Figure 42. FHP3430 KEB012/KEB018 Schematic

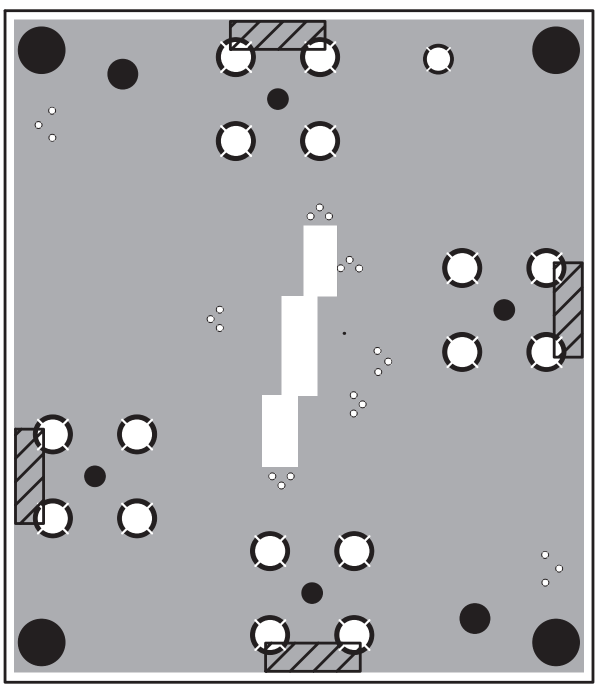


Figure 41. FHP3230 KEB010 (Bottom-side)

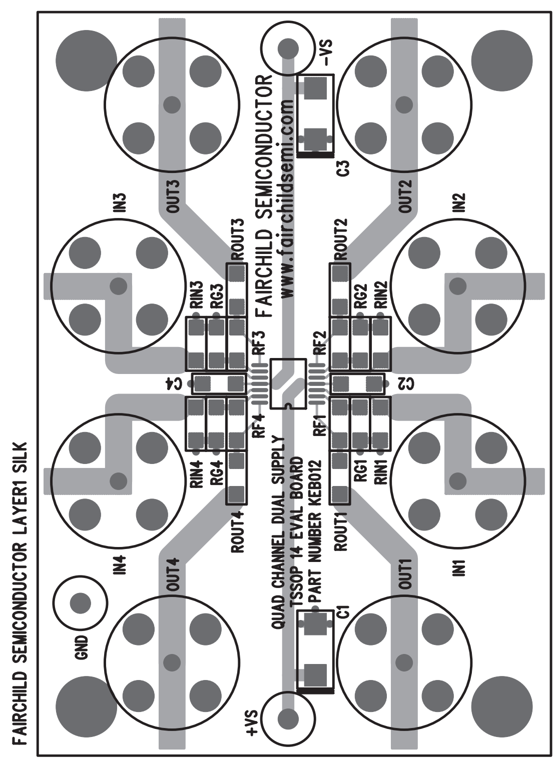


Figure 43. FHP3430 KEB012 (Top-side)

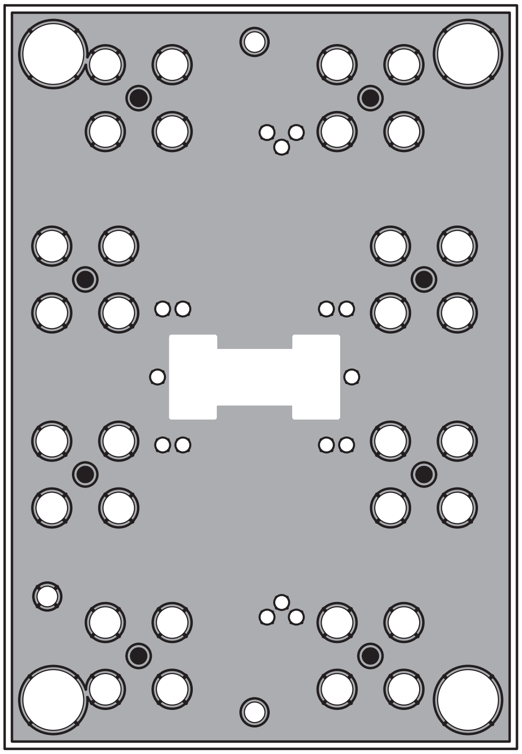


Figure 44. FHP3430 KEB012 (Bottom-side)

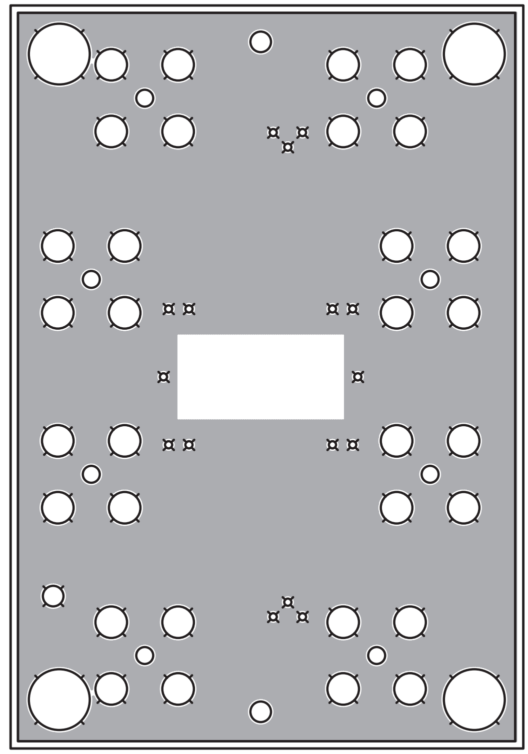


Figure 46. FHP3430 KEB018 (Bottom-side)

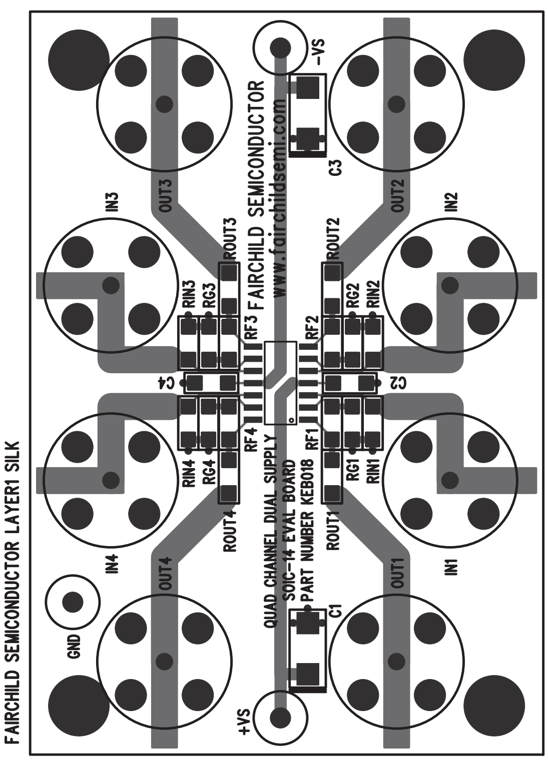


Figure 45. FHP3430 KEB018 (Top-side)

Mechanical Dimensions

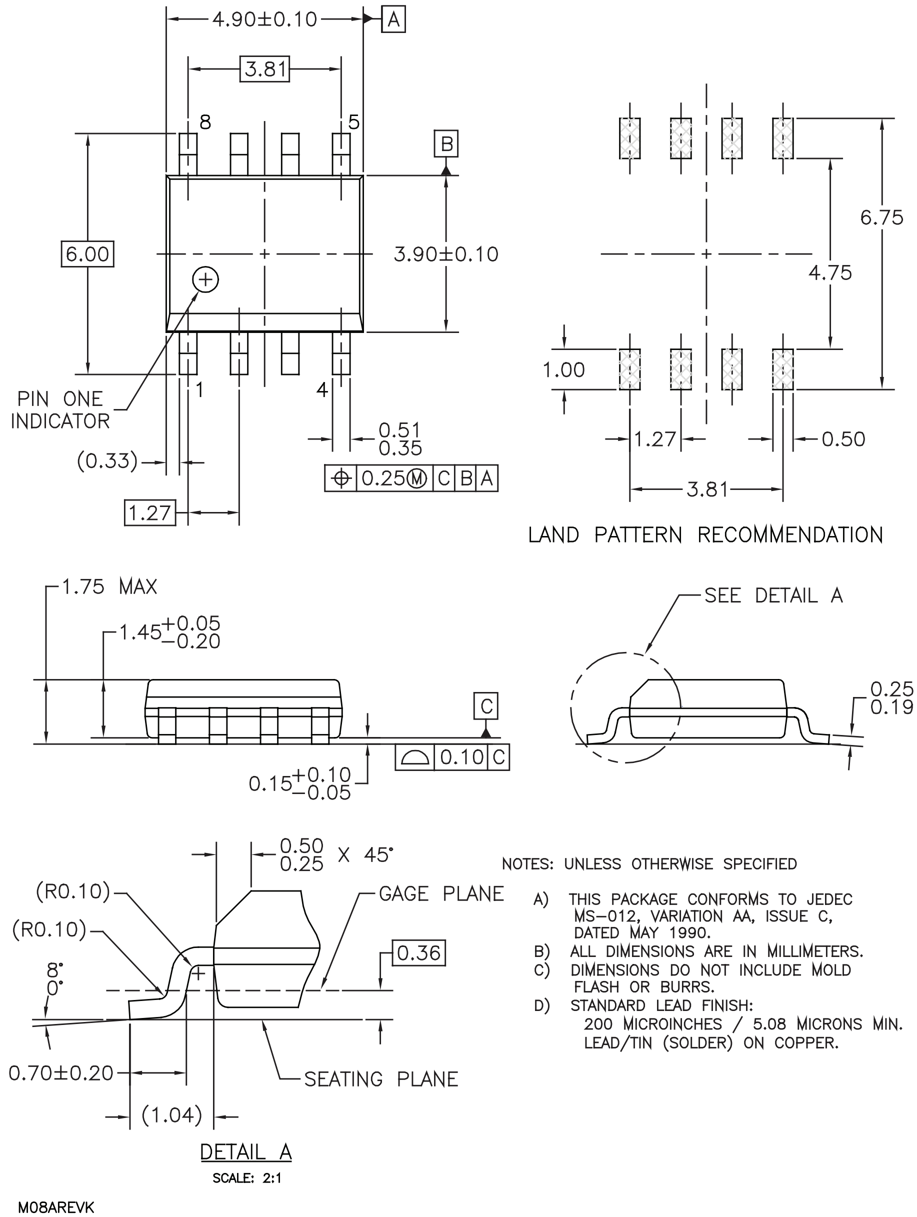
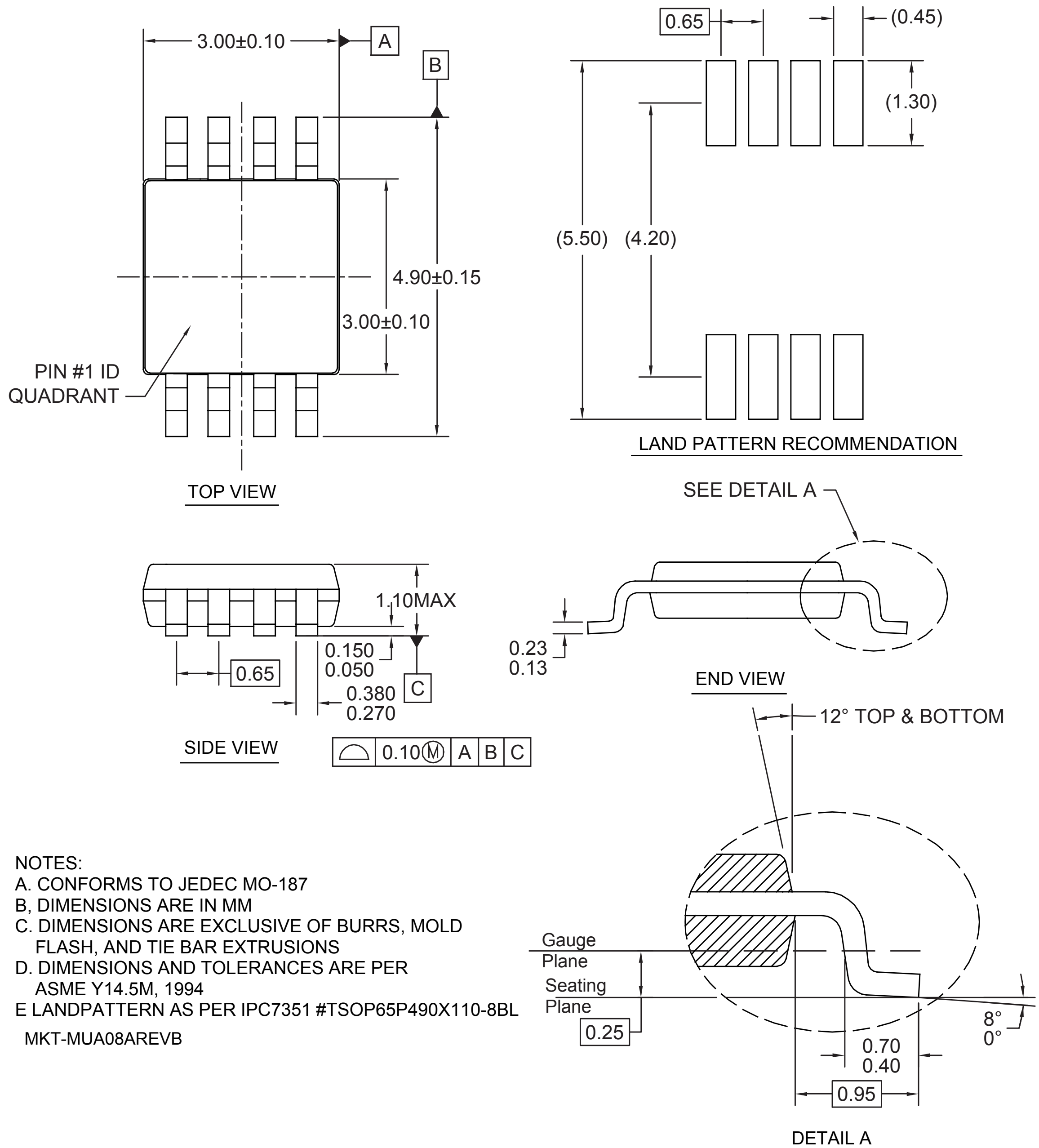


Figure 47. SOIC-8 Package

Mechanical Dimensions



NOTES:
A. CONFORMS TO JEDEC MO-187
B, DIMENSIONS ARE IN MM
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES ARE PER
ASME Y14.5M, 1994
E LANDPATTERN AS PER IPC7351 #TSOP65P490X110-8BL

MKT-MUA08AREVB

Figure 48. MSOP-8 Package

Mechanical Dimensions

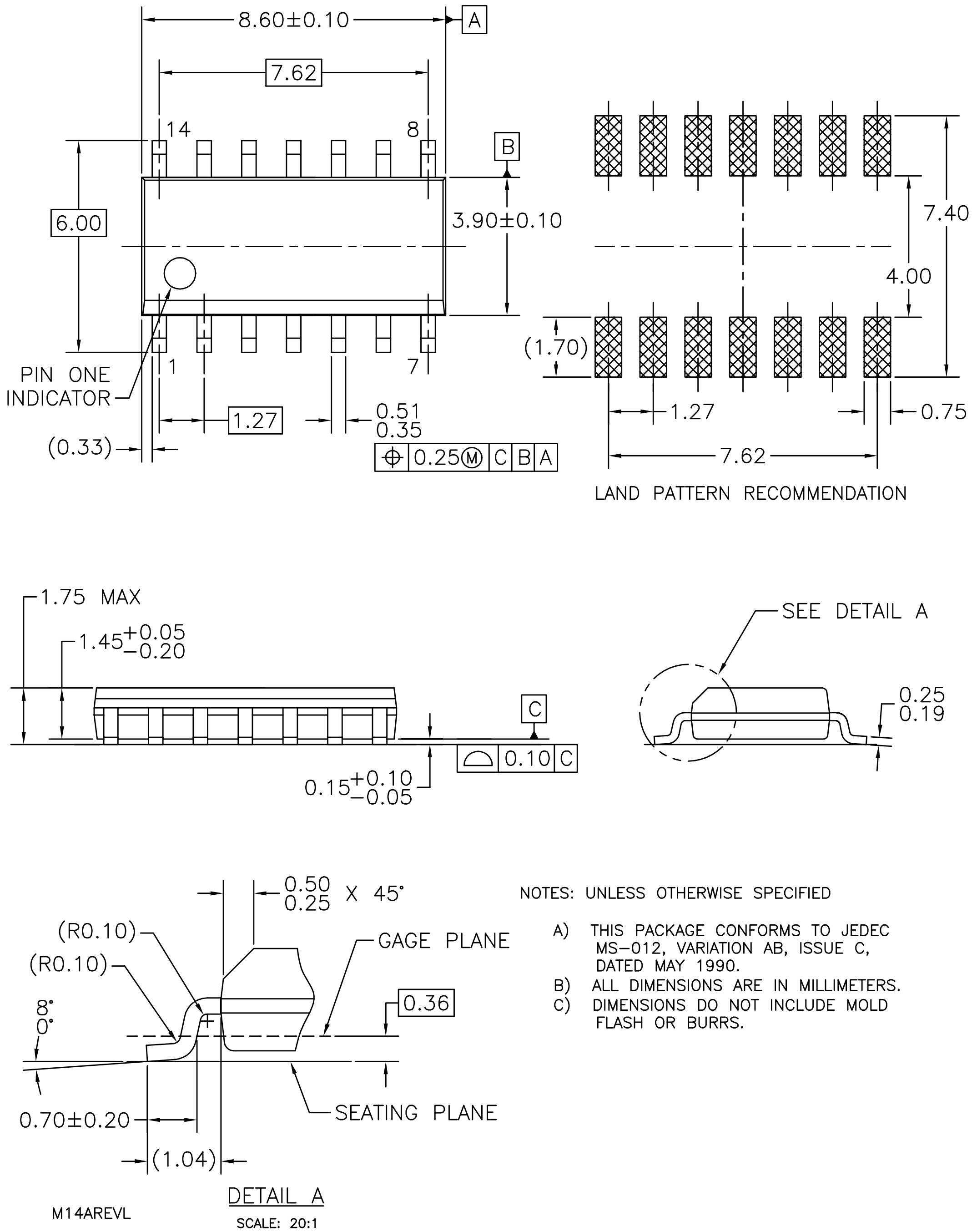


Figure 49. SOIC-14 Package

Mechanical Dimensions

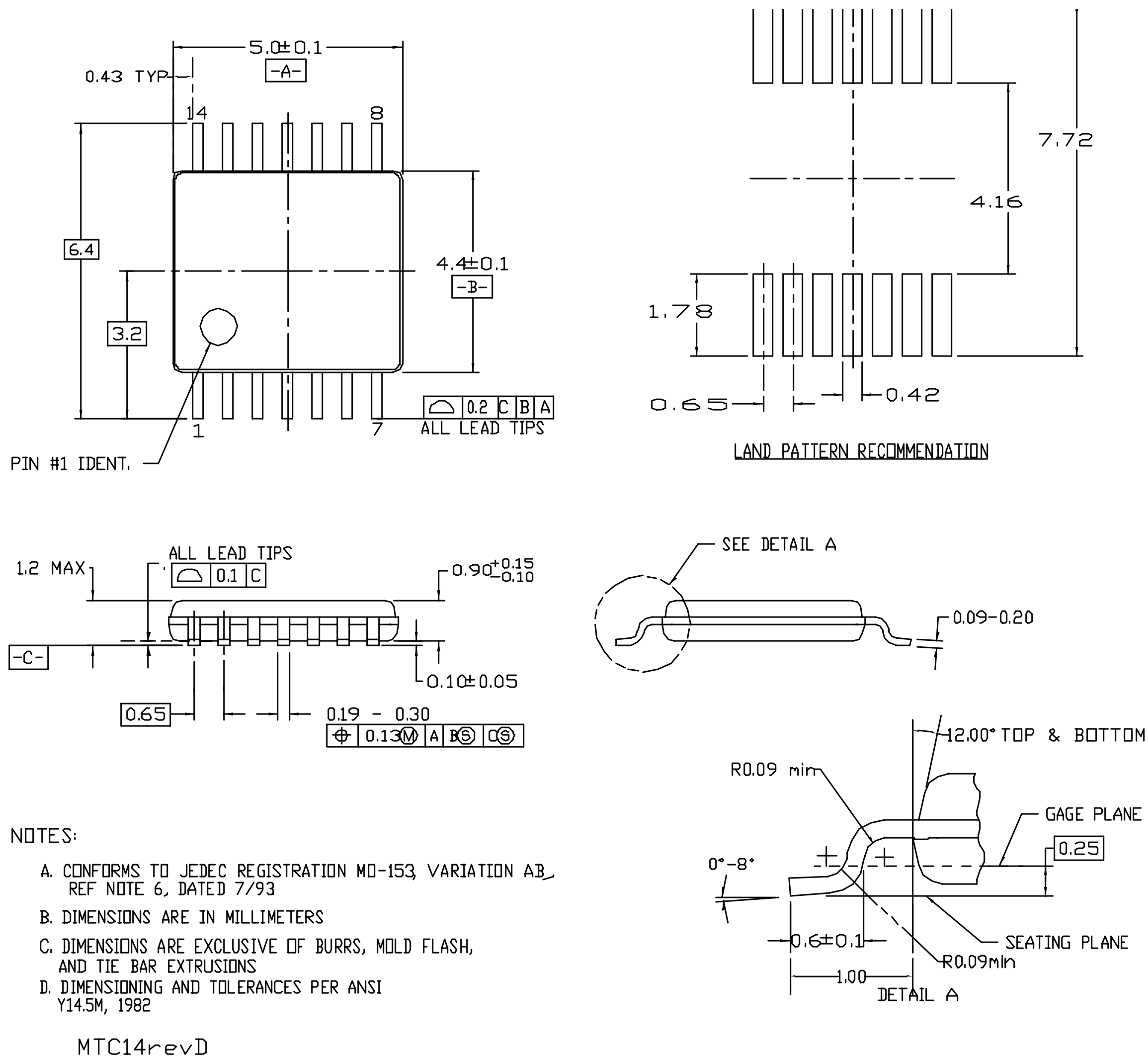
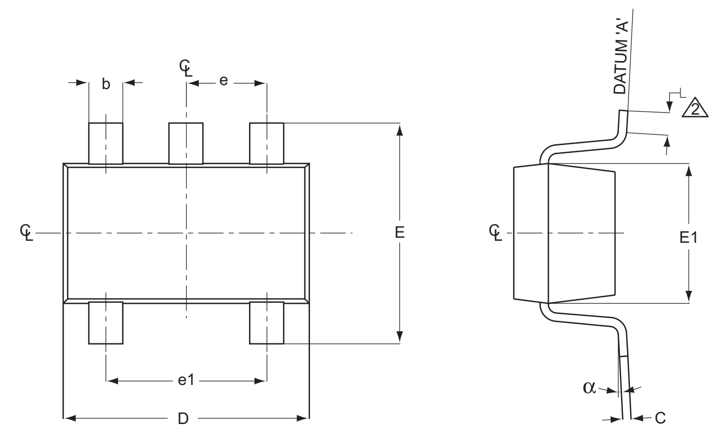
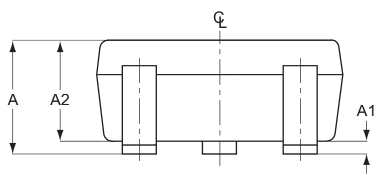


Figure 50. TSSOP-14 Package

Mechanical Dimensions



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 ref	
e1	1.90 ref	
α	0°	10°



NOTE:
1. All dimensions are in millimeters.
2. Foot length measured reference to flat foot surface parallel to DATUM 'A' and lead surface.
3. Package outline exclusive of mold flash & metal burr.
4. Package outline inclusive of solder plating.
5. Comply to EIAJ SC74A.
6. Package ST 0003 REV A supercedes SOT-D-2005 REV C.

Figure 51. SOT23-5 Package

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
DOME™
EcoSPARK™
E^2CMOS™
EnSigna™
FACT™
FAST®
FASTr™
FPS™
FRFET™
FACT Quiet Series™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
Across the board. Around the world.™
The Power Franchise®
Programmable Active Droop™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerEdge™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
µSerDes™
ScalarPump™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
TinyBoost™
TinyBuck™
TinyPWM™
TinyPower™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UniFET™
UltraFET®
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I20

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative