✓RoHS

# RF Power LDMOS Transistors
## N–Channel Enhancement–Mode Lateral MOSFETs

These 56 W RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 716 to 960 MHz.

**900 MHz**

- Typical Single–Carrier W–CDMA Performance: $V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1400 mA, $P_{out}$ = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

| Frequency | $G_{ps}$ (dB) | $\eta_D$ (%) | Output PAR (dB) | ACPR (dBc) | IRL (dB) |
|---|---|---|---|---|---|
| 920 MHz | 19.2 | 34.0 | 6.9 | –35.7 | –25 |
| 940 MHz | 19.3 | 35.1 | 7.0 | –36.0 | –20 |
| 960 MHz | 19.2 | 36.5 | 6.8 | –34.8 | –13 |

**700 MHz**

- Typical Single–Carrier W–CDMA Performance: $V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1400 mA, $P_{out}$ = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.
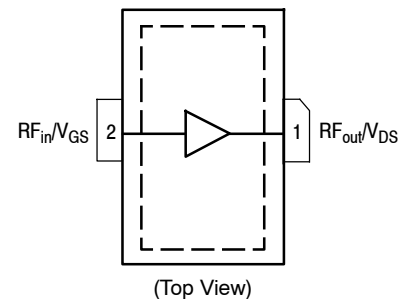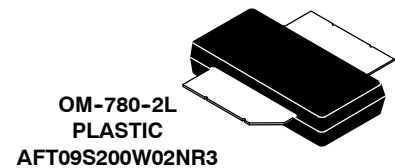
| Frequency | $G_{ps}$ (dB) | $\eta_D$ (%) | Output PAR (dB) | ACPR (dBc) | IRL (dB) |
|---|---|---|---|---|---|
| 716 MHz | 22.7 | 37.5 | 6.9 | –34.7 | –18 |
| 722 MHz | 22.6 | 37.2 | 6.9 | –34.6 | –19 |
| 728 MHz | 22.5 | 36.9 | 6.9 | –34.6 | –18 |

**Features**

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13–inch Reel.

## AFT09S200W02NR3
## AFT09S200W02GNR3

**716–960 MHz, 56 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS**



**OM–780–2L PLASTIC AFT09S200W02NR3**

**OM–780G–2L PLASTIC AFT09S200W02GNR3**



RF$_{in}$/V$_{GS}$  2  ▷  1  RF$_{out}$/V$_{DS}$

(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

**Figure 1. Pin Connections**

✦ freescale™
Airfast

#### Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | –0.5, +70 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | –6.0, +10 | Vdc |
| Operating Voltage | $V_{DD}$ | 32, +0 | Vdc |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature Range | $T_C$ | –40 to +125 | °C |
| Operating Junction Temperature Range [1,2] | $T_J$ | –40 to +225 | °C |

#### Table 2. Thermal Characteristics

| Characteristic | Symbol | Value [2,3] | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>Case Temperature 80°C, 56 W CW, 28 Vdc, $I_{DQ}$ = 1400 mA, 940 MHz | $R_{\theta JC}$ | 0.35 | °C/W |

#### Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22–A114) | 2 |
| Machine Model (per EIA/JESD22–A115) | B |
| Charge Device Model (per JESD22–C101) | IV |

#### Table 4. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD22–A113, IPC/JEDEC J–STD–020 | 3 | 260 | °C |

#### Table 5. Electrical Characteristics ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics** | | | | | |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 70 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | µAdc |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 28 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 5 | µAdc |
| Gate–Source Leakage Current<br>($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | µAdc |
| **On Characteristics** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = 10 Vdc, $I_D$ = 729 µAdc) | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Gate Quiescent Voltage<br>($V_{DS}$ = 28 Vdc, $I_D$ = 1400 mA) | $V_{GS(Q)}$ | — | 2.15 | — | Vdc |
| Fixture Gate Quiescent Voltage [4]<br>($V_{DD}$ = 28 Vdc, $I_D$ = 1400 mA, Measured in Functional Test) | $V_{GG(Q)}$ | 3.2 | 4.3 | 5.2 | Vdc |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 4.1 Adc) | $V_{DS(on)}$ | 0.1 | 0.2 | 0.3 | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. $V_{GG}$ = 2.0 × $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistor divider network on the board. Refer to Test Fixture Layout.

(continued)

**Table 5. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Functional Tests** [1,2] (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1400 mA, $P_{out}$ = 56 W Avg., f = 960 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. | | | | | |
| Power Gain | $G_{ps}$ | 18.5 | 19.2 | 21.5 | dB |
| Drain Efficiency | $\eta_D$ | 32.5 | 36.5 | — | % |
| Output Peak–to–Average Ratio @ 0.01% Probability on CCDF | PAR | 6.5 | 6.8 | — | dB |
| Adjacent Channel Power Ratio | ACPR | — | –34.8 | –33.5 | dBc |
| Input Return Loss | IRL | — | –13 | –9 | dB |

**Load Mismatch** (In Freescale Test Fixture, 50 ohm system) $I_{DQ}$ = 1400 mA, f = 940 MHz

| | |
|---|---|
| VSWR 10:1 at 32 Vdc, 260 W CW Output Power (3 dB Input Overdrive from 180 W CW Rated Power) | No Device Degradation |

**Typical Performance** (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1400 mA, 920–960 MHz Bandwidth

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $P_{out}$ @ 1 dB Compression Point, CW | P1dB | — | 200 | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range) | Φ | — | –11.5 | — | ° |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | 140 | — | MHz |
| Gain Flatness in 40 MHz Bandwidth @ $P_{out}$ = 56 W Avg. | $G_F$ | — | 0.1 | — | dB |
| Gain Variation over Temperature (–30°C to +85°C) | ΔG | — | 0.018 | — | dB/°C |
| Output Power Variation over Temperature (–30°C to +85°C) | ΔP1dB | — | 0.004 | — | dB/°C |

1. Part internally matched both on input and output.
2. Measurement made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

**AFT09S200W02NR3 AFT09S200W02GNR3**
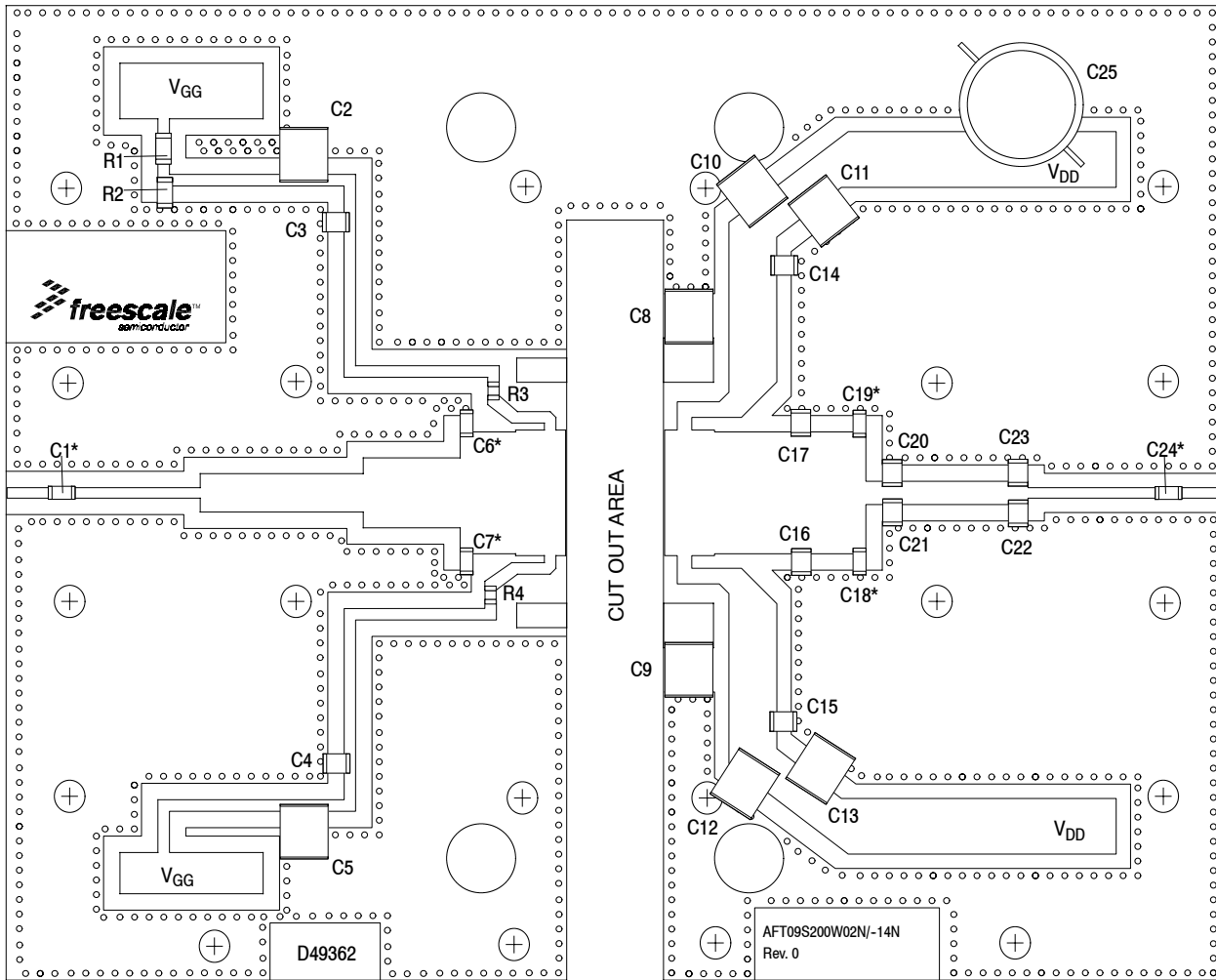
*C1, C6, C7, C18, C19 and C24 are mounted vertically.

**Figure 2. AFT09S200W02NR3 Test Circuit Component Layout — 920–960 MHz**

**Table 6. AFT09S200W02NR3 Test Circuit Component Designations and Values — 920–960 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C3, C4, C14, C15, C24 | 47 pF Chip Capacitors | ATC100B470JT500XT | ATC |
| C2, C5, C8, C9, C10, C11, C12, C13 | 10 $\mu$F Chip Capacitors | C5750X7S2A106M230KB | TDK |
| C6, C7 | 2.7 pF Chip Capacitors | ATC100B2R7BT500XT | ATC |
| C16, C17 | 5.6 pF Chip Capacitors | ATC100B5R6CT500XT | ATC |
| C18, C19 | 2.0 pF Chip Capacitors | ATC100B2R0BT500XT | ATC |
| C20, C21 | 1.0 pF Chip Capacitors | ATC100B1R0BT500XT | ATC |
| C22, C23 | 0.3 pF Chip Capacitors | ATC100B0R3BT500XT | ATC |
| C25 | 220 $\mu$F, 100 V Electrolytic Capacitor | EEV-FK2A221M | Panasonic-ECG |
| R1, R2 | 1000 $\Omega$, 1/4 W Chip Resistors | CRCW12061K00FKEA | Vishay |
| R3, R4 | 10 $\Omega$, 1/8 W Chip Resistors | RK73H2ATTD10R0F | KOA Speer |
| PCB | Rogers RO4350B, 0.020″, $\varepsilon_r$ = 3.66 | D49362 | MTL |

## TYPICAL CHARACTERISTICS — 920–960 MHz



$V_{DD}$ = 28 Vdc, $P_{out}$ = 56 W (Avg.)
$I_{DQ}$ = 1400 mA, Single-Carrier W-CDMA
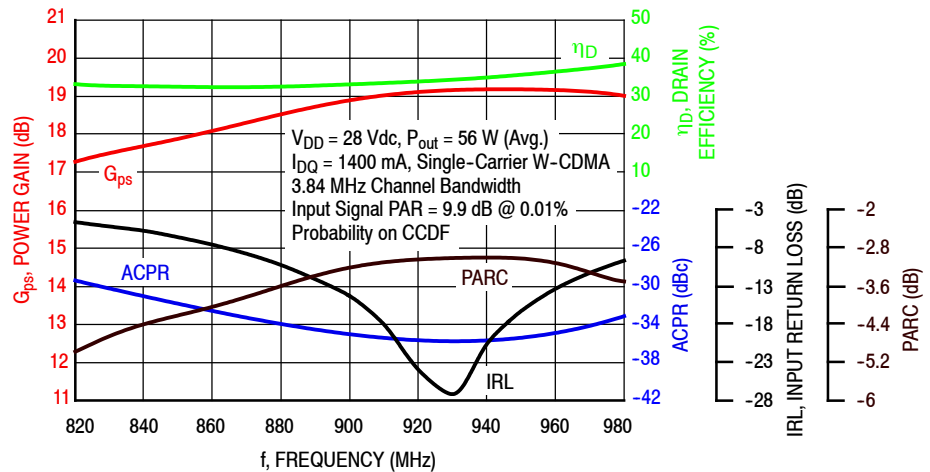3.84 MHz Channel Bandwidth
Input Signal PAR = 9.9 dB @ 0.01%
Probability on CCDF

**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 56 Watts Avg.**
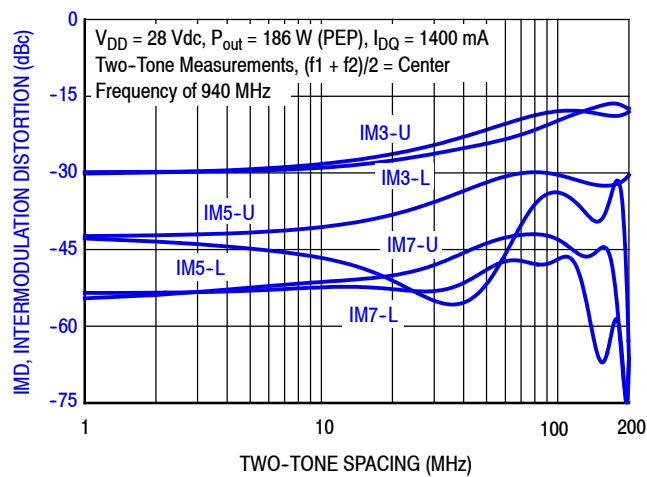


$V_{DD}$ = 28 Vdc, $P_{out}$ = 186 W (PEP), $I_{DQ}$ = 1400 mA
Two-Tone Measurements, (f1 + f2)/2 = Center
Frequency of 940 MHz

**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**



$V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1400 mA, f = 940 MHz
Single-Carrier W-CDMA, 3.84 MHz Channel
Bandwidth, Input Signal PAR = 9.9 dB @ 0.01%
Probability on CCDF

-1 dB = 28 W
-2 dB = 41 W
-3 dB = 56 W
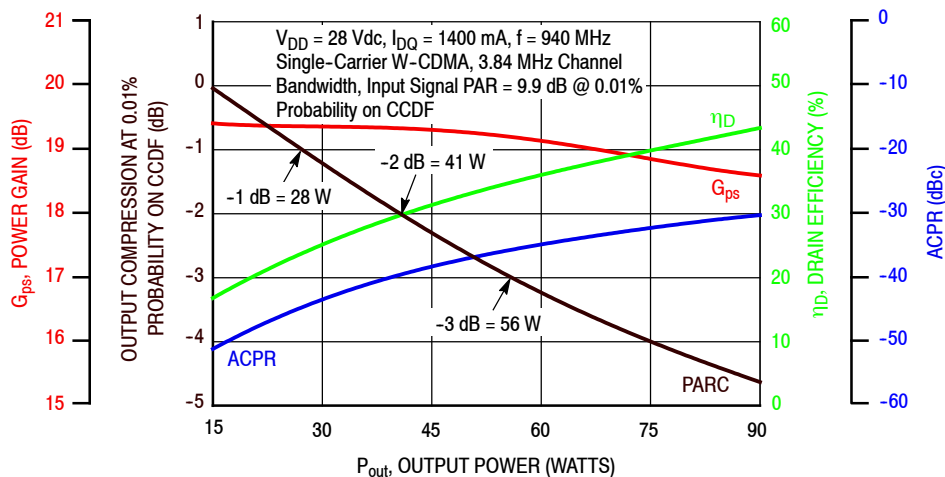
**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

**AFT09S200W02NR3 AFT09S200W02GNR3**
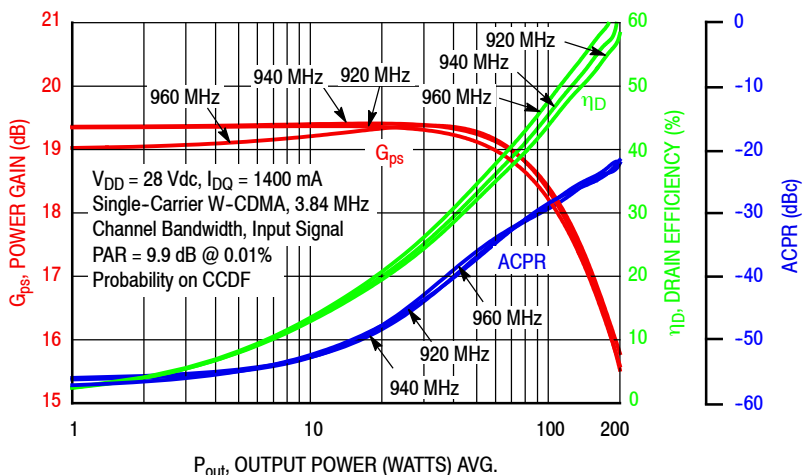
## TYPICAL CHARACTERISTICS — 920–960 MHz



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



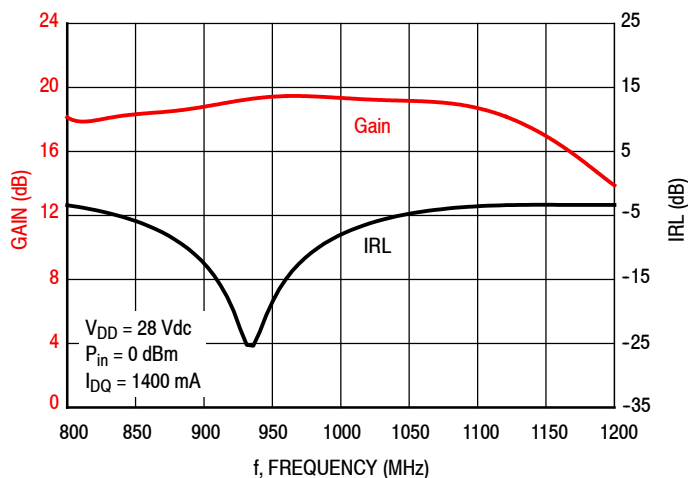**Figure 7. Broadband Frequency Response**

$V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1484 mA, Pulsed CW, 10 $\mu$sec(on), 10% Duty Cycle

| f (MHz) | $Z_{source}$ ($\Omega$) | $Z_{in}$ ($\Omega$) | Max Output Power | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | P1dB | | | | | |
| | | | $Z_{load}$ (1) ($\Omega$) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 920 | 1.94 - j4.69 | 2.09 + j4.54 | 0.625 - j0.97 | 17.7 | 54.0 | 253 | 51.4 | -6 |
| 940 | 2.29 - j5.04 | 2.41 + j4.89 | 0.611 - j1.00 | 17.4 | 53.9 | 245 | 49.2 | -6 |
| 960 | 2.98 - j5.40 | 2.82 + j5.25 | 0.653 - j1.12 | 17.2 | 53.8 | 239 | 49.0 | -6 |

| f (MHz) | $Z_{source}$ ($\Omega$) | $Z_{in}$ ($\Omega$) | Max Output Power | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | P3dB | | | | | |
| | | | $Z_{load}$ (2) ($\Omega$) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 920 | 1.94 - j4.69 | 2.09 + j4.64 | 0.566 - j1.00 | 15.3 | 55.2 | 333 | 53.8 | -9 |
| 940 | 2.29 - j5.04 | 2.43 + j4.99 | 0.564 - j1.06 | 15.0 | 55.1 | 325 | 52.5 | -9 |
| 960 | 2.98 - j5.40 | 2.83 + j5.37 | 0.578 - j1.11 | 14.8 | 55.0 | 318 | 52.0 | -8 |

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

**Figure 8. Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 28 Vdc, $I_{DQ}$ = 1484 mA, Pulsed CW, 10 $\mu$sec(on), 10% Duty Cycle

| f (MHz) | $Z_{source}$ ($\Omega$) | $Z_{in}$ ($\Omega$) | Max Drain Efficiency | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | P1dB | | | | | |
| | | | $Z_{load}$ (1) ($\Omega$) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 920 | 1.94 - j4.69 | 2.10 + j4.65 | 1.36 - j0.05 | 21.1 | 51.6 | 144 | 65.6 | -12 |
| 940 | 2.29 - j5.04 | 2.45 + j4.99 | 1.33 - j0.14 | 20.8 | 51.6 | 145 | 63.6 | -11 |
| 960 | 2.98 - j5.40 | 2.87 + j5.33 | 1.30 - j0.35 | 20.2 | 51.9 | 154 | 62.5 | -10 |

| f (MHz) | $Z_{source}$ ($\Omega$) | $Z_{in}$ ($\Omega$) | Max Drain Efficiency | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | P3dB | | | | | |
| | | | $Z_{load}$ (2) ($\Omega$) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 920 | 1.94 - j4.69 | 2.12 + j4.72 | 1.34 - j0.18 | 18.9 | 52.8 | 191 | 68.6 | -17 |
| 940 | 2.29 - j5.04 | 2.47 + j5.10 | 1.30 - j0.13 | 18.8 | 52.5 | 179 | 67.1 | -17 |
| 960 | 2.98 - j5.40 | 2.89 + j5.44 | 1.27 - j0.35 | 18.2 | 52.8 | 191 | 65.6 | -15 |

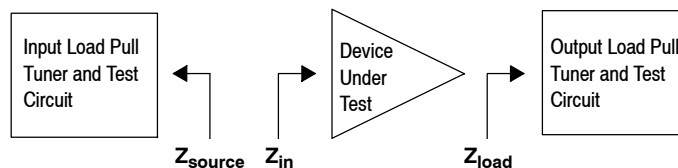(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

**Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning**



Input Load Pull Tuner and Test Circuit — Device Under Test — Output Load Pull Tuner and Test Circuit

$Z_{source}$  $Z_{in}$  $Z_{load}$
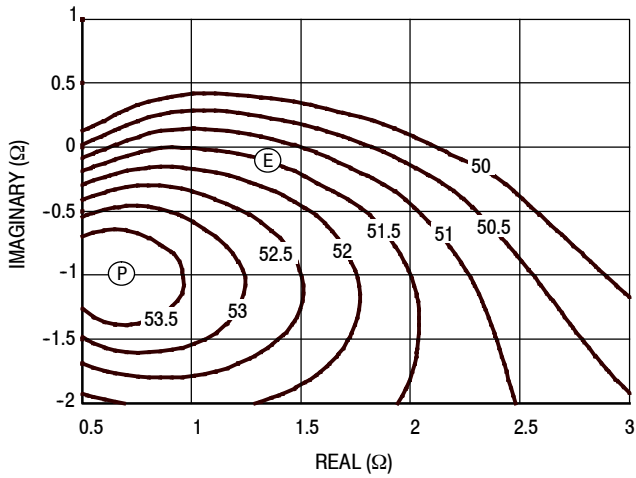
# P1dB - TYPICAL LOAD PULL CONTOURS — 940 MHz



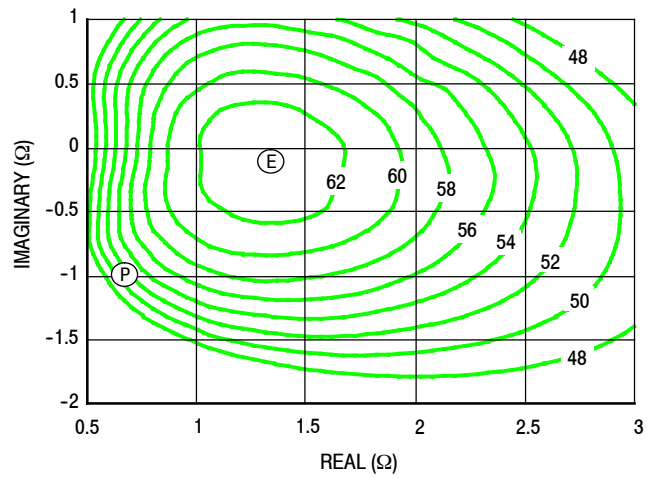Figure 10. P1dB Load Pull Output Power Contours (dBm)
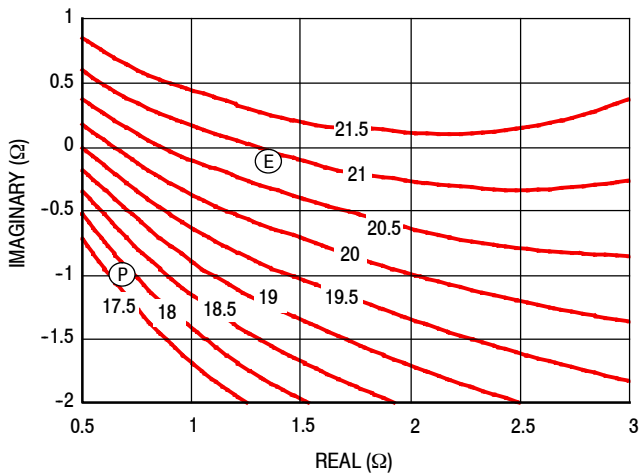


Figure 11. P1dB Load Pull Efficiency Contours (%)
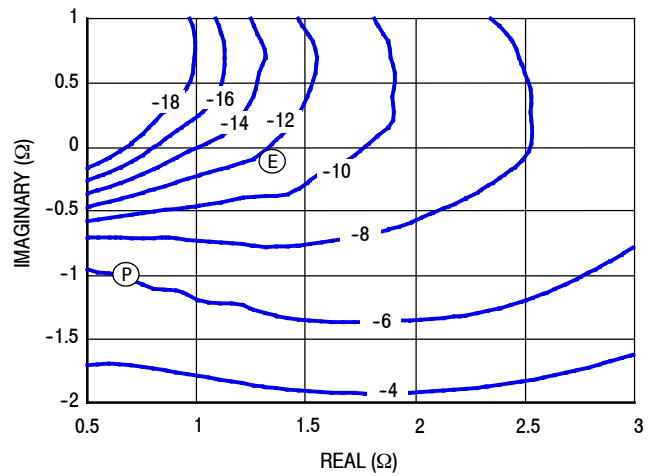


Figure 12. P1dB Load Pull Gain Contours (dB)



Figure 13. P1dB Load Pull AM/PM Contours (°)

**NOTE:** ⓅP = Maximum Output Power

ⒺE = Maximum Drain Efficiency

— Gain
— Drain Efficiency
— Linearity
— Output Power

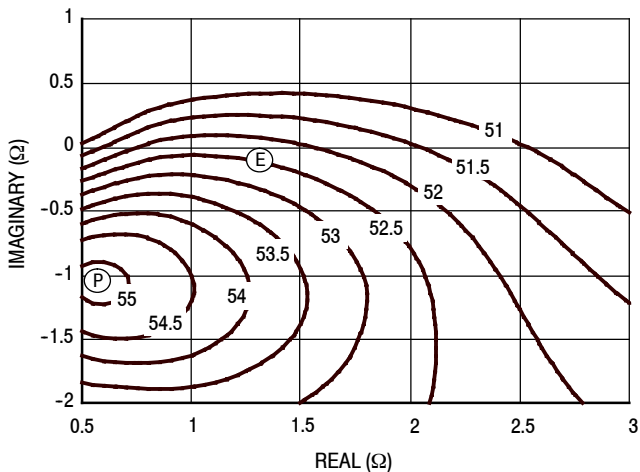## P3dB – TYPICAL LOAD PULL CONTOURS — 940 MHz



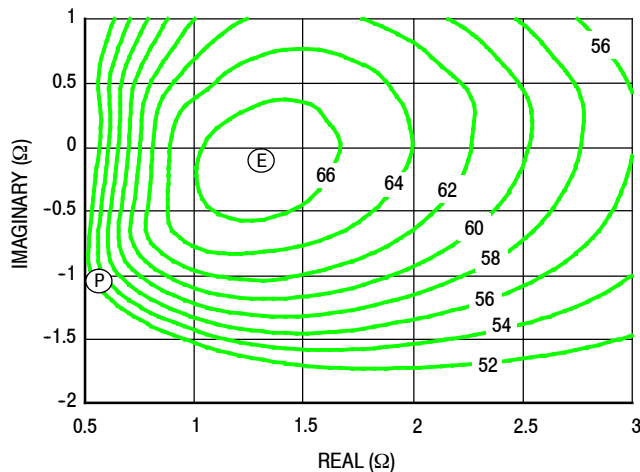Figure 14. P3dB Load Pull Output Power Contours (dBm)



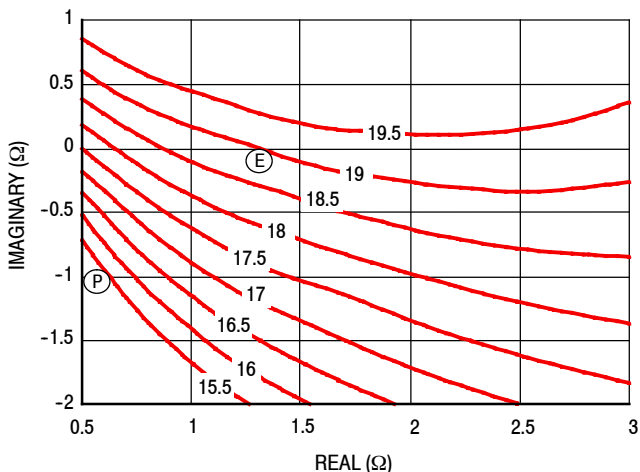Figure 15. P3dB Load Pull Efficiency Contours (%)
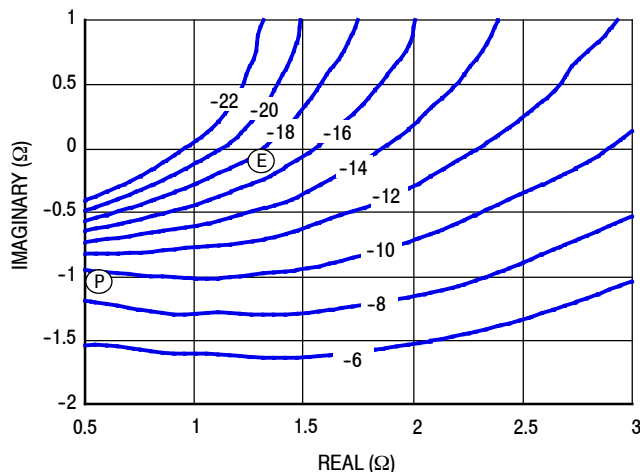

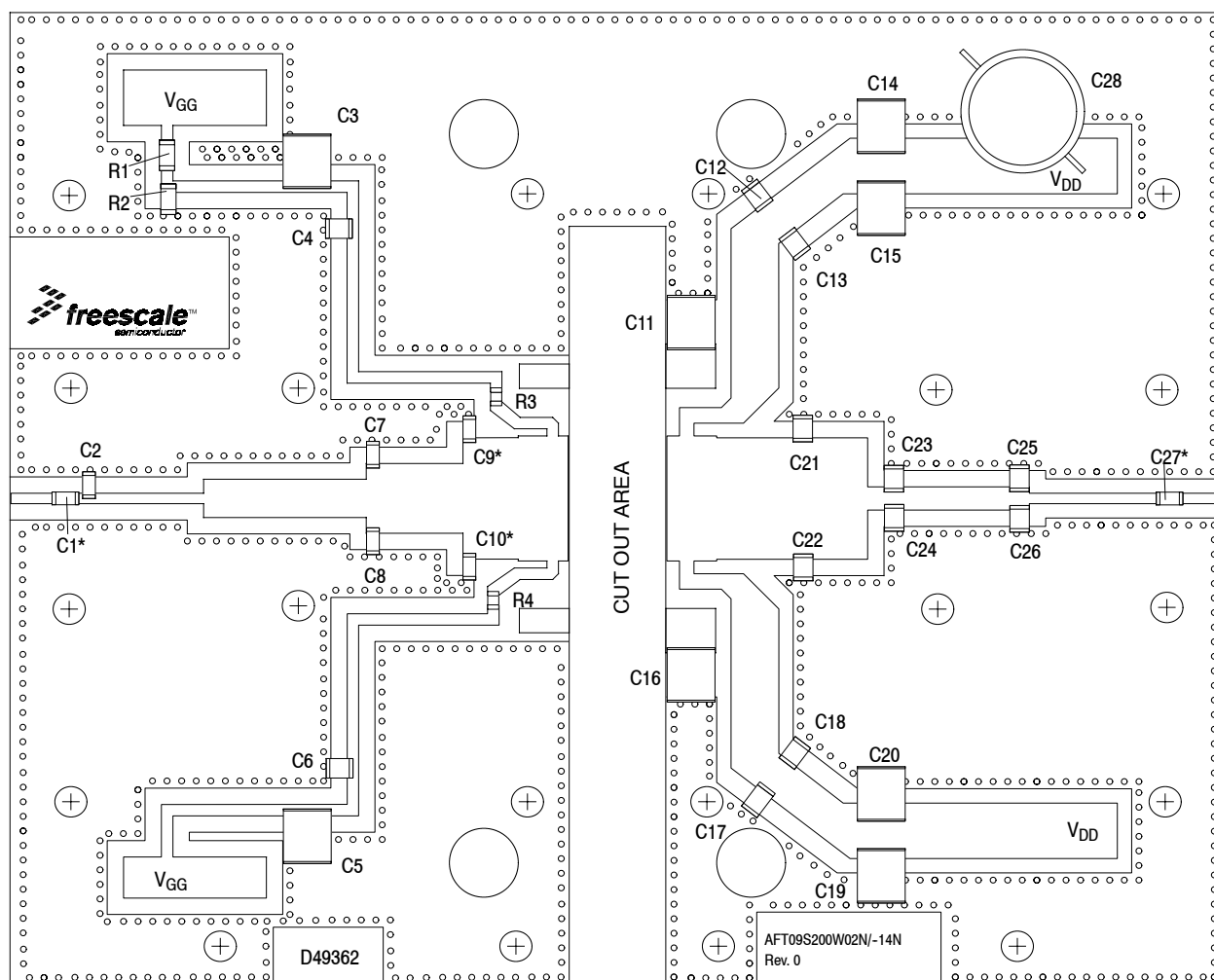
Figure 16. P3dB Load Pull Gain Contours (dB)



Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

—— Gain
—— Drain Efficiency
—— Linearity
—— Output Power

*C1, C9, C10, and C27 are mounted vertically.

**Figure 18. AFT09S200W02NR3 Test Circuit Component Layout — 716–728 MHz**

**Table 7. AFT09S200W02NR3 Test Circuit Component Designations and Values — 716–728 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C4, C6, C12, C13, C17, C18, C27 | 68 pF Chip Capacitors | ATC100B680JT500XT | ATC |
| C2 | 1.1 pF Chip Capacitor | ATC100B1R1BT500XT | ATC |
| C3, C5, C11, C14, C15, C16, C19, C20 | 15 $\mu$F Chip Capacitors | C5750X7S2A156M250KB | TDK |
| C7, C8, C21, C22 | 5.1 pF Chip Capacitors | ATC100B5R1CT500XT | ATC |
| C9, C10 | 9.1 pF Chip Capacitors | ATC100B9R1CT500XT | ATC |
| C23, C24 | 6.8 pF Chip Capacitors | ATC100B6R8CT500XT | ATC |
| C25, C26 | 1.7 pF Chip Capacitors | ATC100B1R7BT500XT | ATC |
| C28 | 220 $\mu$F, 100 V Electrolytic Capacitor | EEV-FK2A221M | Panasonic-ECG |
| R1, R2 | 1000 $\Omega$, 1/4 W Chip Resistors | CRCW12061K00FKEA | Vishay |
| R3, R4 | 10 $\Omega$, 1/8 W Chip Resistors | RK73H2ATTD10R0F | KOA Speer |
| PCB | Rogers RO4350B, 0.020″, $\varepsilon_r$ = 3.66 | D49362 | MTL |

**AFT09S200W02NR3 AFT09S200W02GNR3**

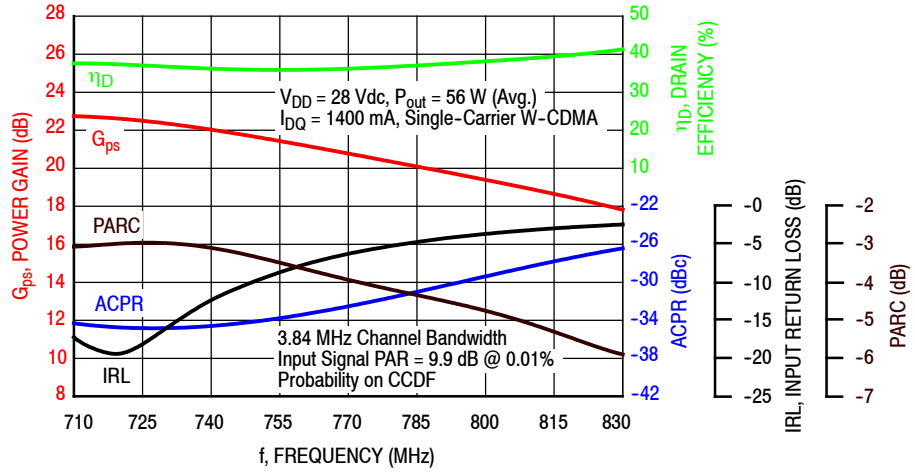## ALTERNATIVE CHARACTERIZATION—716–728 MHz



**Figure 19. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 56 Watts Avg.**
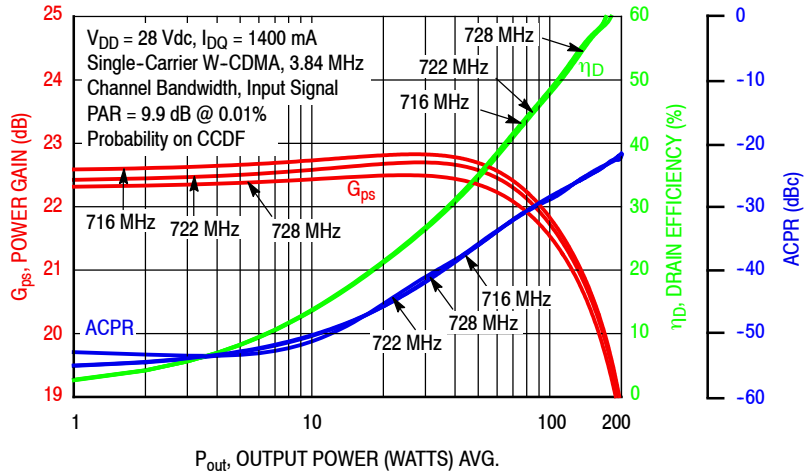


**Figure 20. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**
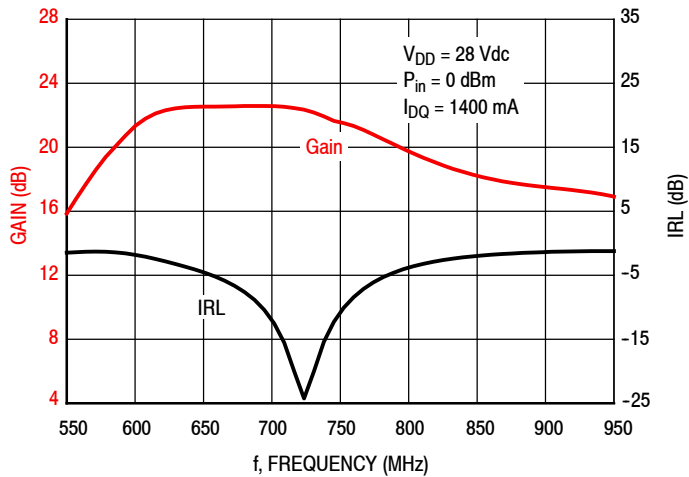


**Figure 21. Broadband Frequency Response**

**AFT09S200W02NR3 AFT09S200W02GNR3**

**PACKAGE DIMENSIONS**



| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
|---|---|---|---|
| TITLE:<br><br>OM780−2<br>STRAIGHT LEAD | DOCUMENT NO: 98ASA10831D | | REV: B |
| | CASE NUMBER: 2021−03 | | 22 OCT 2009 |
| | STANDARD: NON−JEDEC | | |

BOTTOM VIEW
VIEW G—G

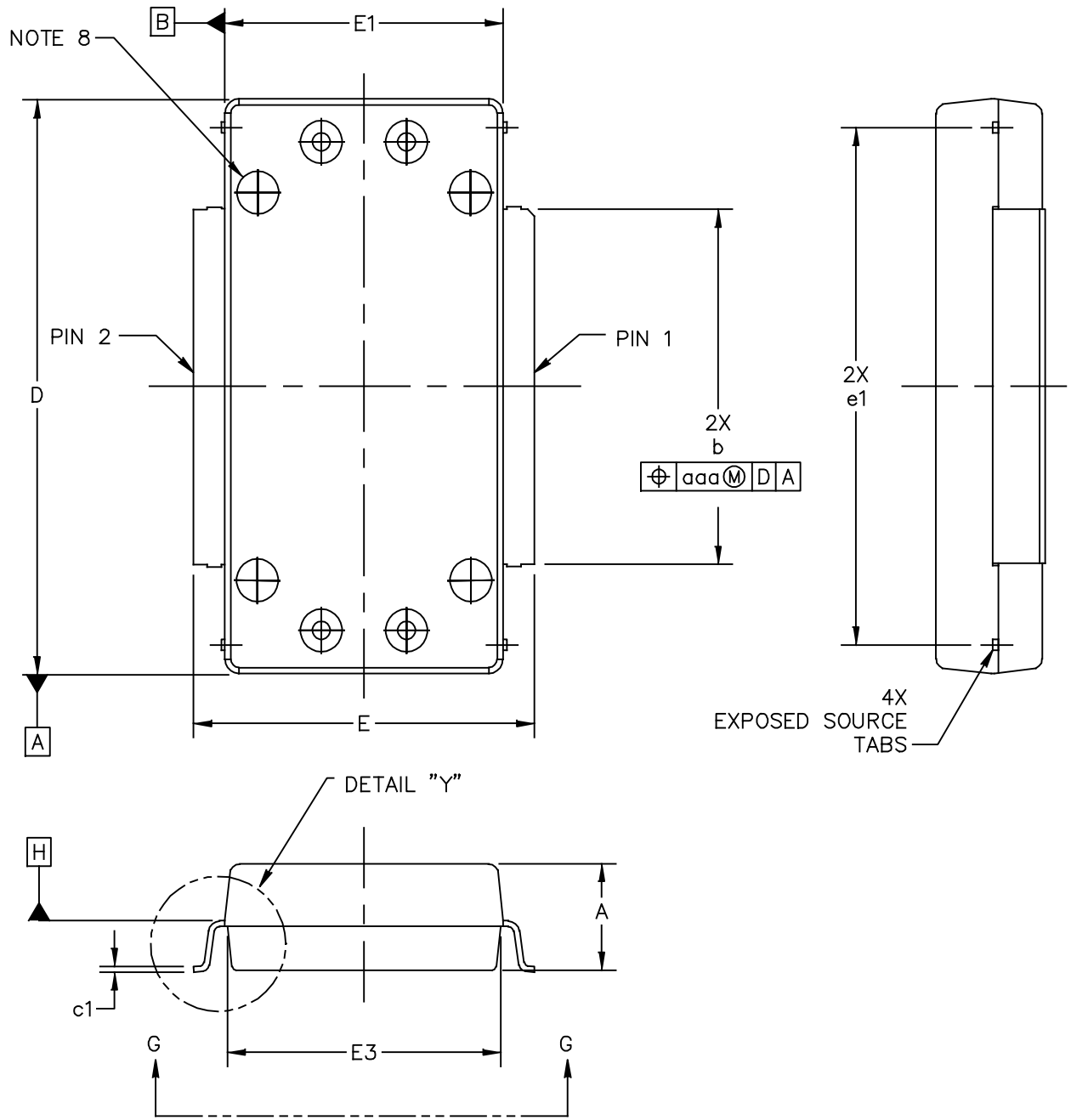| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
|---|---|---|---|
| TITLE: OM780−2 STRAIGHT LEAD | DOCUMENT NO: 98ASA10831D | | REV: B |
| | CASE NUMBER: 2021−03 | | 22 OCT 2009 |
| | STANDARD: NON−JEDEC | | |

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD
   WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION.  ALLOWABLE
   PROTRUSION IS .006 PER SIDE.  DIMENSIONS "D AND "E1" DO INCLUDE MOLD
   MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.  ALLOWABLE DAMBAR
   PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM
   MATERIAL CONDITION.

6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1
   AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES
   OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
     PIN 1 - DRAIN
     PIN 2 - GATE
     PIN 3 - SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|-----|------|------|------|------|-----|------|------|------|------|
| A   | 0.148 | .152 | 3.76 | 3.86 | b   | .497 | .503 | 12.62 | 12.78 |
| A1  | .059 | .065 | 1.50 | 1.65 | c1  | .007 | .011 | 0.18 | 0.28 |
| D   | .808 | .812 | 20.52 | 20.62 | e1  | .721 | .729 | 18.31 | 18.52 |
| D1  | .720 | ---- | 18.29 | ---- |   |   |   |   |   |
| E   | .762 | .770 | 19.36 | 19.56 | aaa | .004 |   | 0.10 |   |
| E1  | .390 | .394 | 9.91 | 10.01 |   |   |   |   |   |
| E2  | .306 | ---- | 7.77 | ---- |   |   |   |   |   |
| E3  | .383 | .387 | 9.73 | 9.83 |   |   |   |   |   |
| F   | .025 BSC |   | 0.635 BSC |   |   |   |   |   |   |

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

| TITLE: | | |
|--------|--|--|
| OM780-2 STRAIGHT LEAD | DOCUMENT NO: 98ASA10831D | REV: B |
| | CASE NUMBER: 2021-03 | 22 OCT 2009 |
| | STANDARD: NON-JEDEC | |

**AFT09S200W02NR3 AFT09S200W02GNR3**

NOTE 8

B ◄ |← E1 →|

PIN 2 →

D

PIN 1 ←

2X
b

⊕ aaa Ⓜ D A

2X
e1

A

4X
EXPOSED SOURCE
TABS

DETAIL "Y"

H

A

c1

G ← E3 → G

| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE:<br><br>OM−780−2 GULL | DOCUMENT NO: 98ASA00442D | REV: O |
|---|---|---|
| | CASE NUMBER: 2267−01 | 14 DEC 2011 |
| | STANDARD: NON−JEDEC | |

AFT09S200W02NR3 AFT09S200W02GNR3

E2

NOTE 7

PIN 2

PIN 1

D1

PIN 3

BOTTOM VIEW
VIEW G—G

DETAIL "Y"

(A2)

GAGE
PLANE

L1

D

Θ

L

A1

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

OM—780—2 GULL

DOCUMENT NO: 98ASA00442D

REV: O

CASE NUMBER: 2267—01

14 DEC 2011

STANDARD: NON—JEDEC

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD
   WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.  ALLOWABLE
   PROTRUSION IS .006 INCH (0.15 MM) PER SIDE.  DIMENSIONS D AND E1 DO INCLUDE MOLD
   MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.  ALLOWABLE DAMBAR
   PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE b DIMENSION AT
   MAXIMUM MATERIAL CONDITION.

6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENT THE EXPOSED AREA OF THE HEAT SLUG.THE DIMENSIONS D1
   AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE
   EDGES OF EXPOSED AREA OF HEAT SLUG.

8. DIMPLED HOLE REPRESENTS INPUT SIDE.

9. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE
   IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

| DIM | INCH MIN | MAX | MILLIMETER MIN | MAX | DIM | INCH MIN | MAX | MILLIMETER MIN | MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .148 | .152 | 3.76 | 3.86 | b | .497 | .503 | 12.62 | 12.78 |
| A1 | −.003 | .003 | −0.08 | 0.08 | c1 | .007 | .011 | 0.18 | 0.28 |
| A2 | (.150) | | (3.81) | | Θ | 0° | 8° | 0° | 8° |
| D | .808 | .812 | 20.52 | 20.62 | e1 | .721 | .729 | 18.31 | 18.52 |
| D1 | .720 | ---- | 18.29 | ---- | aaa | .004 | | 0.10 | |
| E | .472 | .480 | 11.99 | 12.19 | | | | | |
| E1 | .390 | .394 | 9.91 | 10.01 | | | | | |
| E2 | .306 | ---- | 7.77 | ---- | | | | | |
| E3 | .383 | .387 | 9.73 | 9.83 | | | | | |
| L | .018 | .024 | 0.46 | 0.61 | | | | | |
| L1 | .01 BSC | | 0.25 BSC | | | | | | |

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MECHANICAL OUTLINE    PRINT VERSION NOT TO SCALE

TITLE:

OM−780−2 GULL

DOCUMENT NO: 98ASA00442D    REV: 0

CASE NUMBER: 2267−01    14 DEC 2011

STANDARD: NON−JEDEC

**AFT09S200W02NR3 AFT09S200W02GNR3**

RF Device Data
Freescale Semiconductor, Inc.                                    17

NOTES:

1. CONTROLLING DIMENSION: INCH

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| DIM | INCH MIN | MAX | MILLIMETER MIN | MAX | DIM | INCH MIN | MAX | MILLIMETER MIN | MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .148 | .152 | 3.76 | 3.86 | b | .497 | .503 | 12.62 | 12.78 |
| A1 | −.003 | .003 | −0.08 | 0.08 | c1 | .007 | .011 | 0.18 | 0.28 |
| A2 | (.150) | | (3.81) | | Θ | 0° | 8° | 0° | 8° |
| D | .808 | .812 | 20.52 | 20.62 | e1 | .721 | .729 | 18.31 | 18.52 |
| D1 | .720 | ---- | 18.29 | ---- | aaa | .004 | | 0.10 | |
| E | .472 | .480 | 11.99 | 12.19 | | | | | |
| E1 | .390 | .394 | 9.91 | 10.01 | | | | | |
| E2 | .306 | ---- | 7.77 | ---- | | | | | |
| E3 | .383 | .387 | 9.73 | 9.83 | | | | | |
| L | .018 | .024 | 0.46 | 0.61 | | | | | |
| L1 | .01 BSC | | 0.25 BSC | | | | | | |

MECHANICAL OUTLINE    PRINT VERSION NOT TO SCALE

TITLE:

OM−780−2 GULL

DOCUMENT NO: 98ASA00442D    REV: 0

CASE NUMBER: 2267−01    14 DEC 2011

STANDARD: NON−JEDEC

**AFT09S200W02NR3 AFT09S200W02GNR3**

# PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

**Application Notes**

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over–Molded Plastic Packages

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

**Development Tools**

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

# REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|------|-------------|
| 0 | Apr. 2014 | • Initial Release of Data Sheet |

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