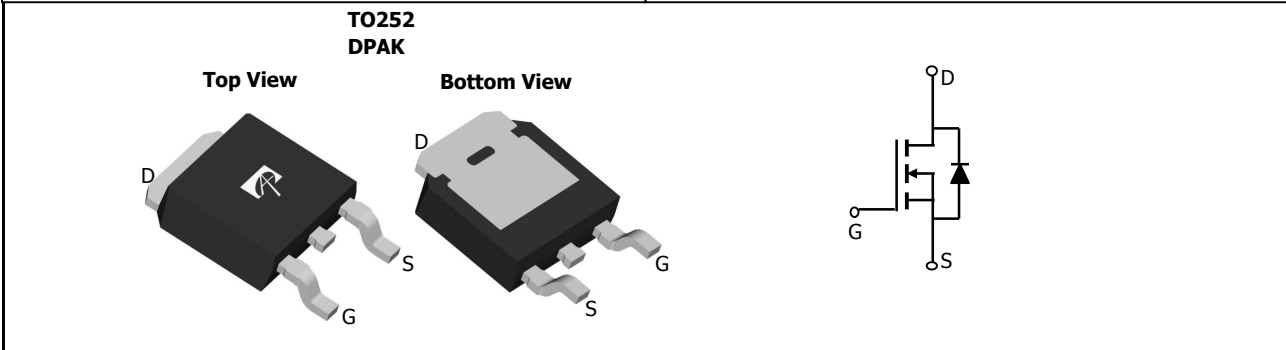




AOD488

N-Channel Enhancement Mode Field Effect Transistor

| | |
|--|--|
| <p>General Description</p> <p>The AOD488 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.</p> <ul style="list-style-type: none"> -RoHS Compliant -Halogen Free* | <p>Features</p> <p>$V_{DS} = 40V$ $I_D = 20 A$ ($V_{GS} = 10V$) $R_{DS(ON)} < 26 m\Omega$ ($V_{GS} = 10V$) $R_{DS(ON)} < 39 m\Omega$ ($V_{GS} = 4.5V$)</p> <p style="text-align: right;">100% UIS Tested! 100% Rg Tested!</p> |
|--|--|



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|-------------------|------------|------------|
| Drain-Source Voltage | V_{DS} | 40 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current | $T_C=25^\circ C$ | 20 | A |
| | $T_C=100^\circ C$ | 23 | |
| Pulsed Drain Current ^C | I_{DM} | 50 | |
| Avalanche Current ^C | I_{AR} | 12 | A |
| Repetitive avalanche energy $L=0.3mH$ ^C | E_{AR} | 22 | mJ |
| Power Dissipation ^B | $T_C=25^\circ C$ | 50 | W |
| | $T_C=100^\circ C$ | 25 | |
| Power Dissipation ^A | $T_A=25^\circ C$ | 2 | W |
| | $T_A=70^\circ C$ | 1.3 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 175 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 17.4 | 30 | $^\circ C/W$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 50 | 60 |
| Maximum Junction-to-Case ^B | $R_{\theta JC}$ | 2.3 | 3 | $^\circ C/W$ |

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|--|------|--------|------------------|
| STATIC PARAMETERS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D=10\text{mA}$, $V_{GS}=0\text{V}$ | 40 | 45 | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$ | | | 1 5 | μA |
| I_{GSS} | Gate-Body leakage current | $V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$ | | | 0.1 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$ | 1 | 2.3 | 3 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$ | 50 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}=10\text{V}$, $I_D=20\text{A}$ | | 21.5 | 26 | $\text{m}\Omega$ |
| | | $T_J=125^\circ\text{C}$ | | 34 | 41 | |
| | | $V_{GS}=4.5\text{V}$, $I_D=8\text{A}$ | | 31 | 39 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{DS}=5\text{V}$, $I_D=20\text{A}$ | | 25 | | S |
| V_{SD} | Diode Forward Voltage | $I_S=1\text{A}$, $V_{GS}=0\text{V}$ | | 0.76 | 1 | V |
| I_S | Maximum Body-Diode Continuous Current | | | | 20 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$ | | 404 | 500 | pF |
| C_{oss} | Output Capacitance | | | 95 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 37 | | pF |
| R_g | Gate resistance | $V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$ | | 2.7 | 4 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| $Q_g(10\text{V})$ | Total Gate Charge | $V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$ | | 9.2 | 12 | nC |
| $Q_g(4.5\text{V})$ | Total Gate Charge | | | 4.5 | | nC |
| Q_{gs} | Gate Source Charge | | | 1.6 | | nC |
| Q_{gd} | Gate Drain Charge | | | 2.6 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=1.0\Omega$, $R_{GEN}=3\Omega$ | | 3.5 | | ns |
| t_r | Turn-On Rise Time | | | 6 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 13.2 | | ns |
| t_f | Turn-Off Fall Time | | | 3.5 | | ns |
| t_{rr} | Body Diode Reverse Recovery Time | | $I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 22.9 | |
| Q_{rr} | Body Diode Reverse Recovery Charge | $I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 18.3 | | nC |

A: The value of R_{qJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on R_{thJA} and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on $T_J(\text{MAX})=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=175^\circ\text{C}$.

D: The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\text{ms}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX})=175^\circ\text{C}$.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: July 2010

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

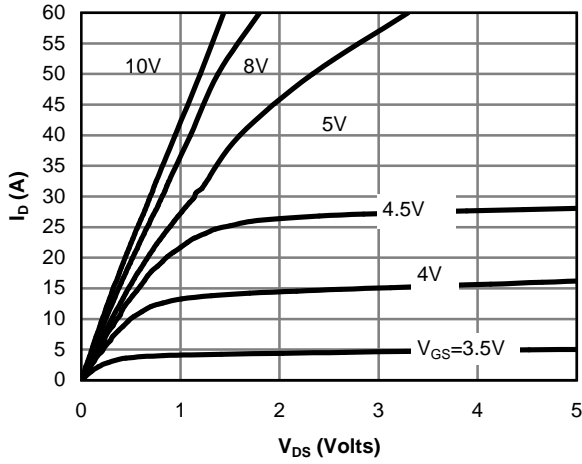


Fig 1: On-Region Characteristics

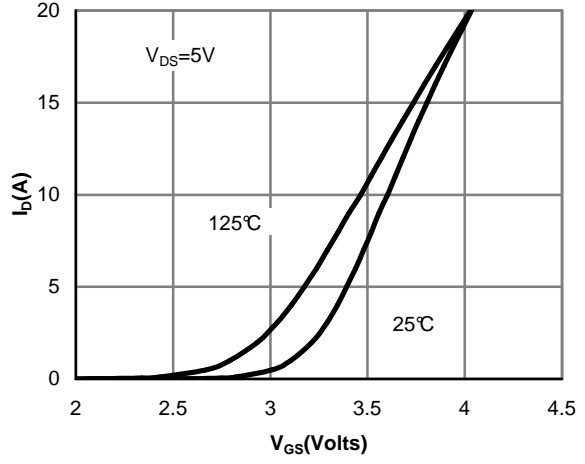


Figure 2: Transfer Characteristics

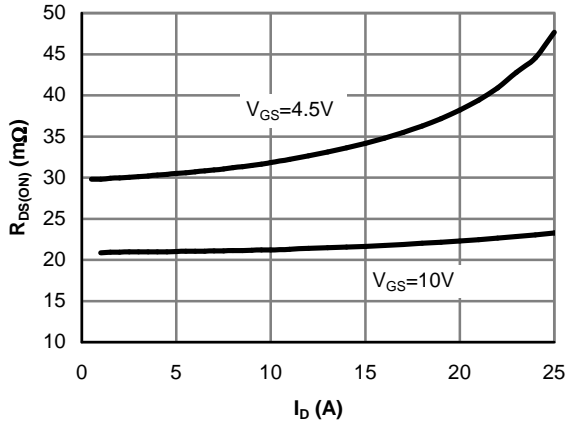


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

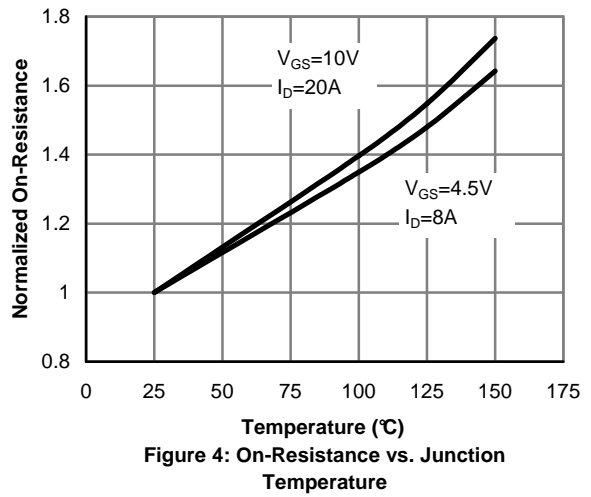


Figure 4: On-Resistance vs. Junction Temperature

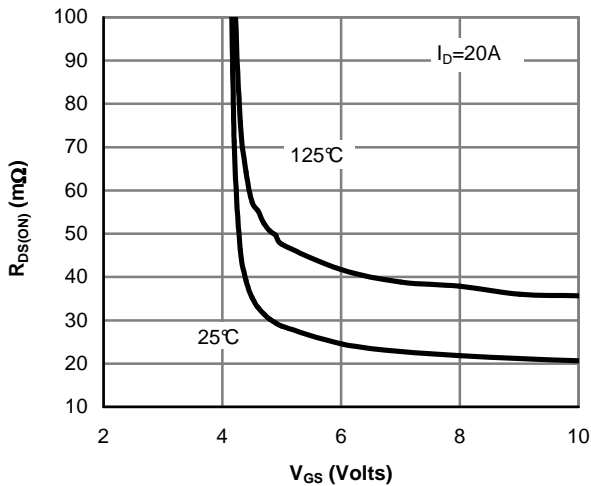


Figure 5: On-Resistance vs. Gate-Source Voltage

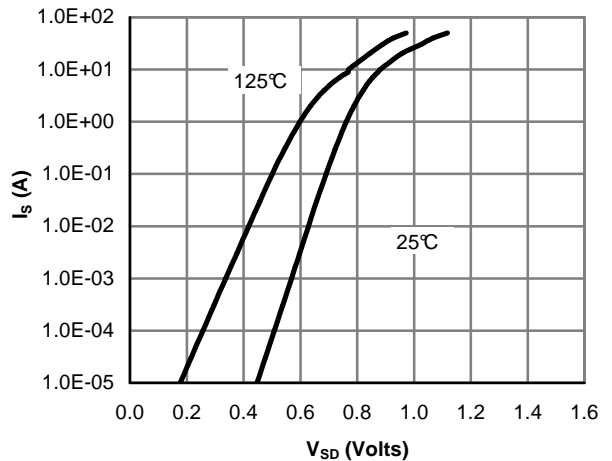


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

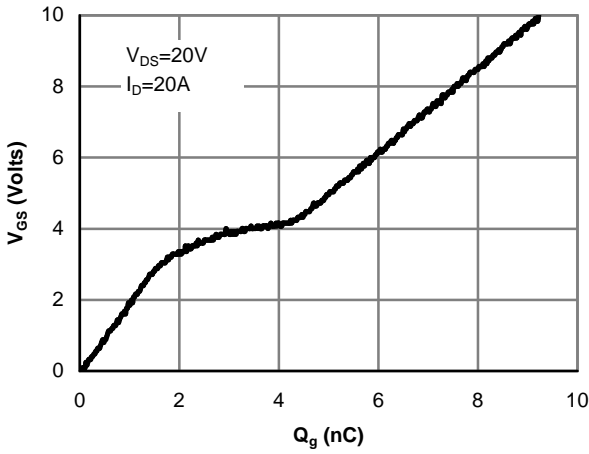


Figure 7: Gate-Charge Characteristics

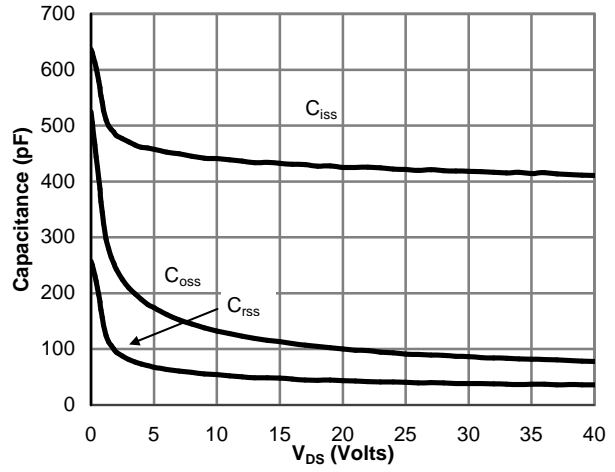


Figure 8: Capacitance Characteristics

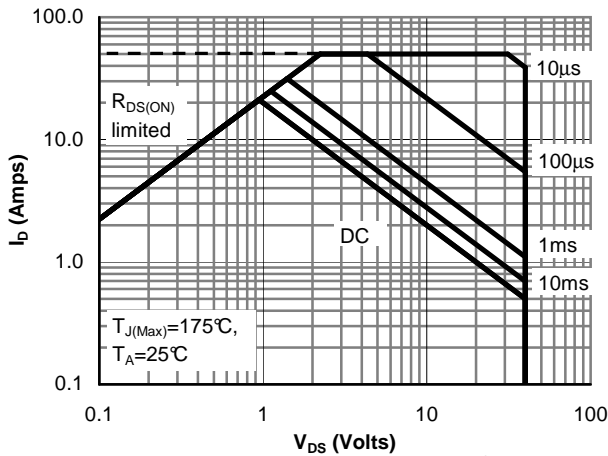


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

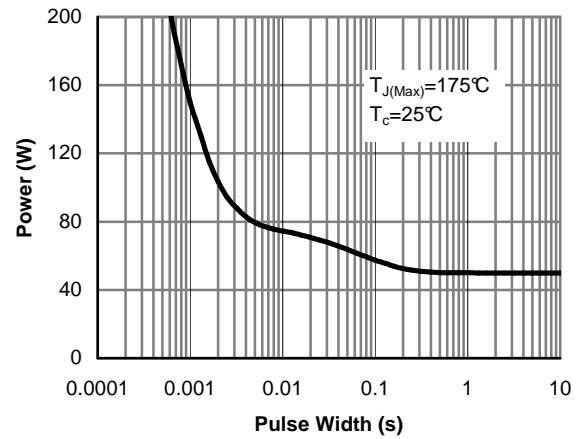


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

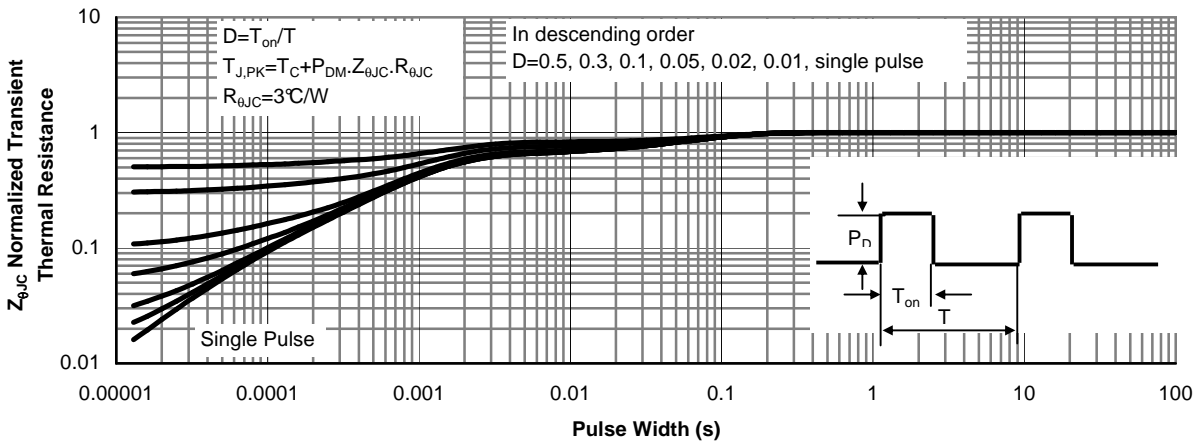


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

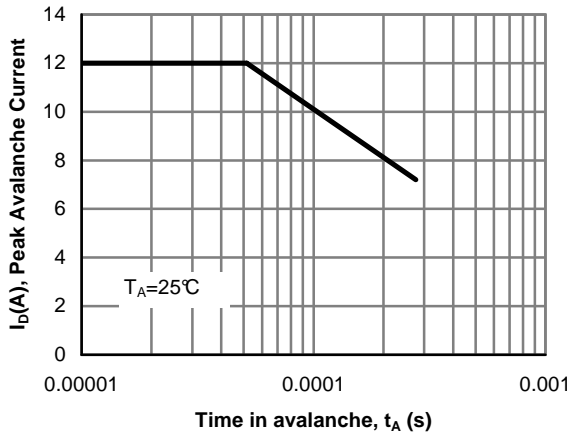


Figure 12: Single Pulse Avalanche capability

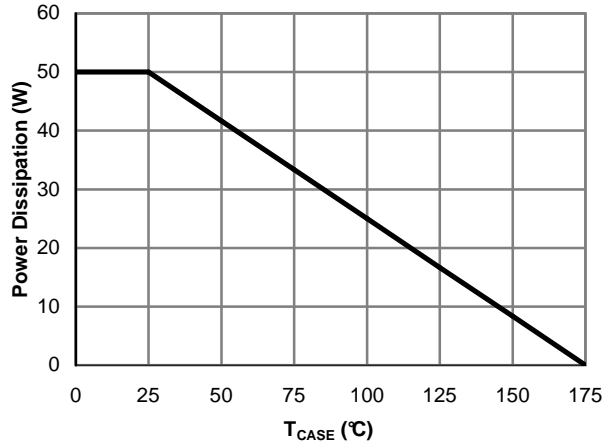


Figure 13: Power De-rating (Note B)

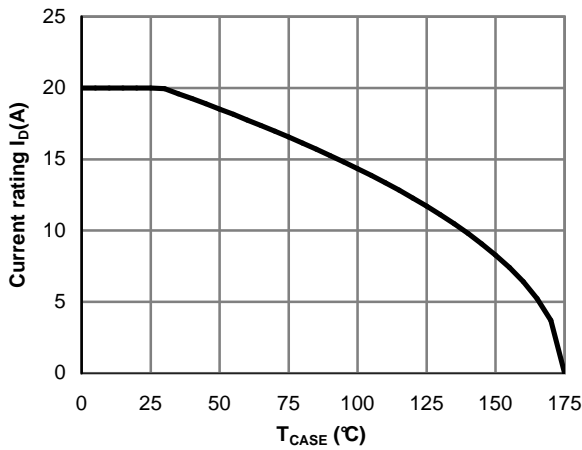


Figure 14: Current De-rating (Note B)

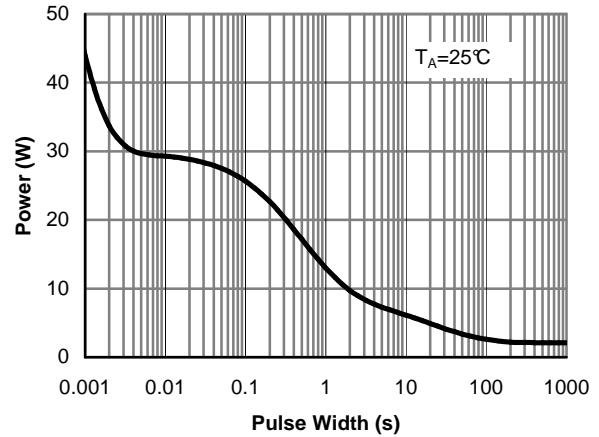


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

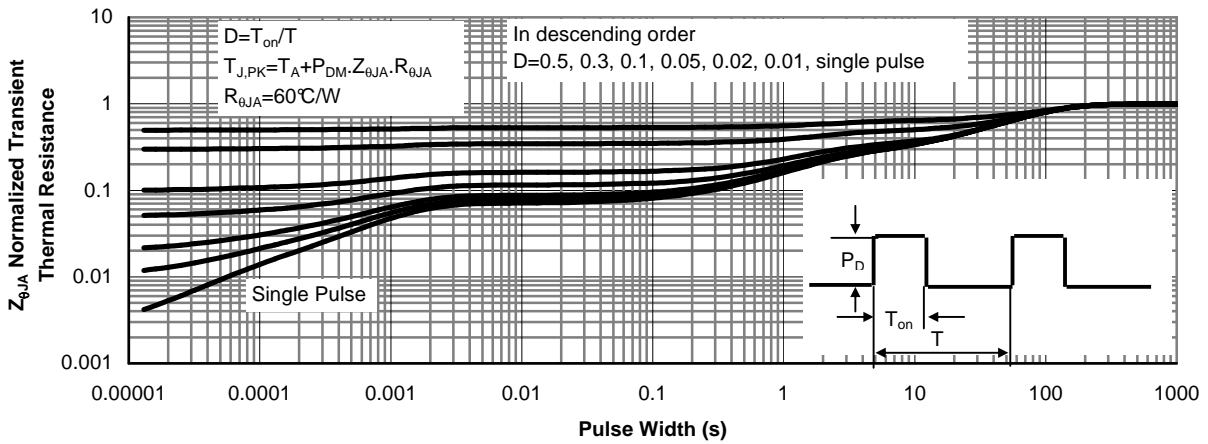
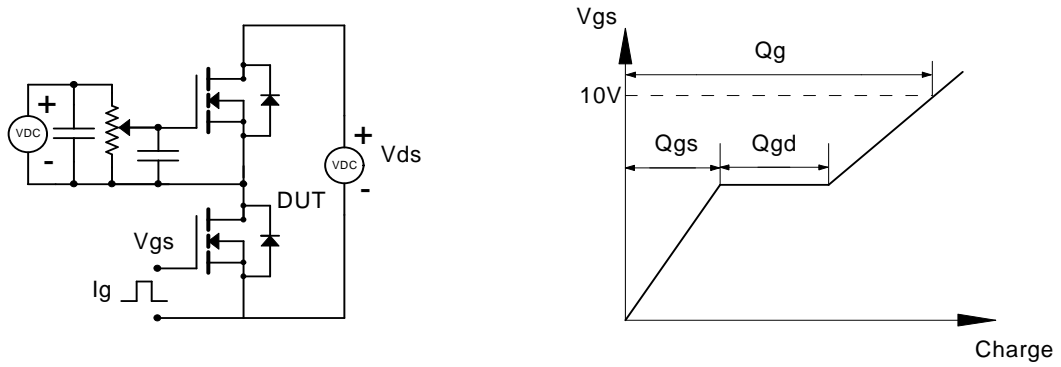
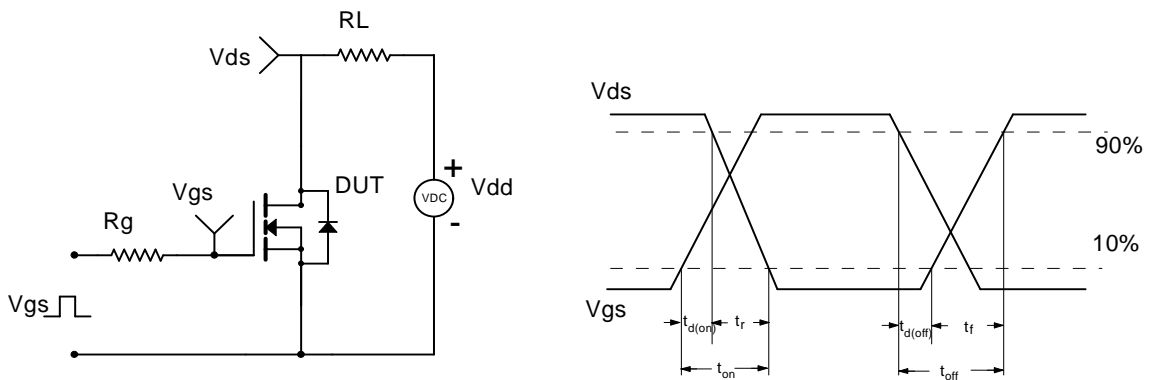


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

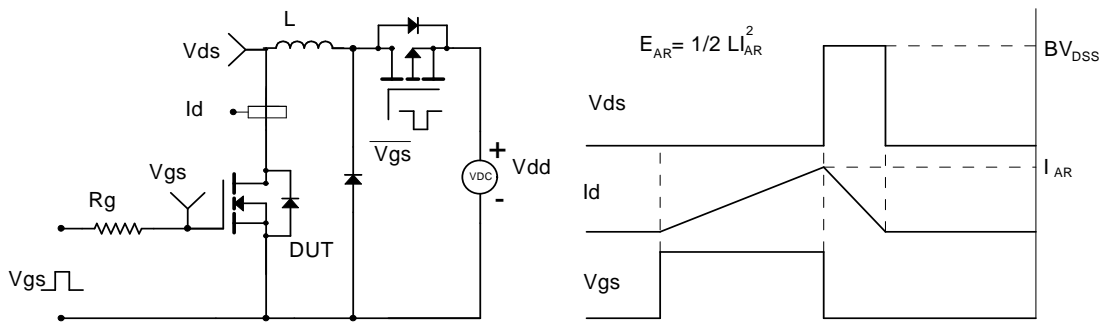
Gate Charge Test Circuit & Waveform



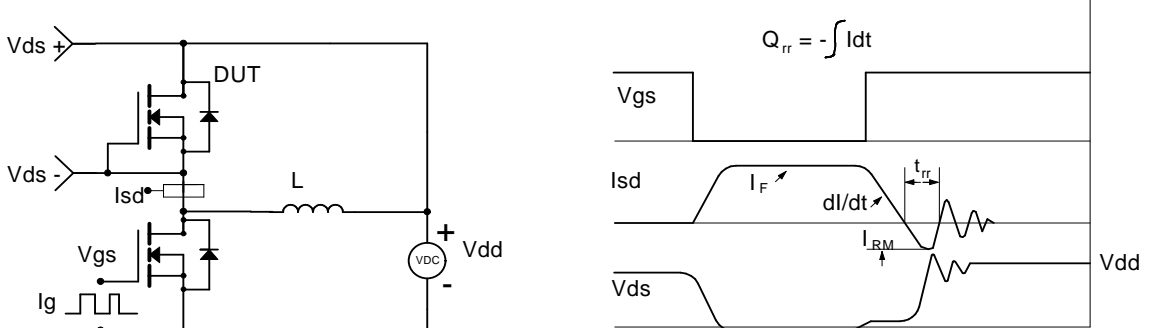
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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