

### General Description

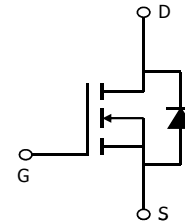
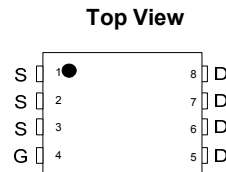
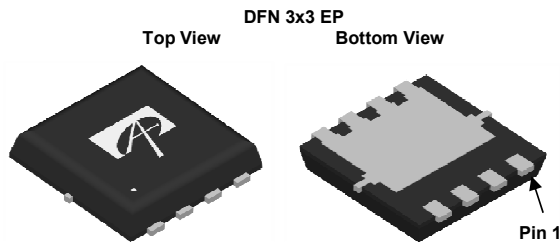
The AON7410 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in DC - DC converters and Load Switch applications.

RoHS and Halogen-Free Compliant

### Features

$V_{DS}$  (V) = 30V  
 $I_D$  = 24A ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 20m\Omega$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 26m\Omega$  ( $V_{GS} = 4.5V$ )

100% UIS Tested  
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON7410	DFN 3x3 EP	Tape & Reel	5000

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	50	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	17	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	14	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	30	$^\circ\text{C/W}$
		Steady-State	60	
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	5	6	$^\circ\text{C/W}$

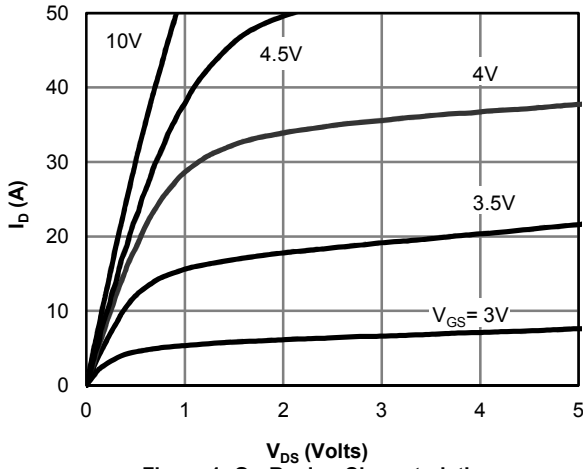
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.4	1.8	2.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	50			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =8A T <sub>J</sub> =125°C		16 24	20 29	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =7A		21	26	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A		30		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	440	550	660	pF
C <sub>oss</sub>	Output Capacitance		77	110	143	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		33	55	77	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	3	4	4.9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =8A	7.8	9.8	12	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		3.6	4.6	5.5	nC
Q <sub>gs</sub>	Gate Source Charge		1.4	1.8	2.2	nC
Q <sub>gd</sub>	Gate Drain Charge		1.3	2.2	3	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =2Ω, R <sub>GEN</sub> =3Ω		5		ns
t <sub>r</sub>	Turn-On Rise Time			3.2		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			24		ns
t <sub>f</sub>	Turn-Off Fall Time			6		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =8A, di/dt=500A/μs	7	9	11	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =8A, di/dt=500A/μs	12	15	18	nC

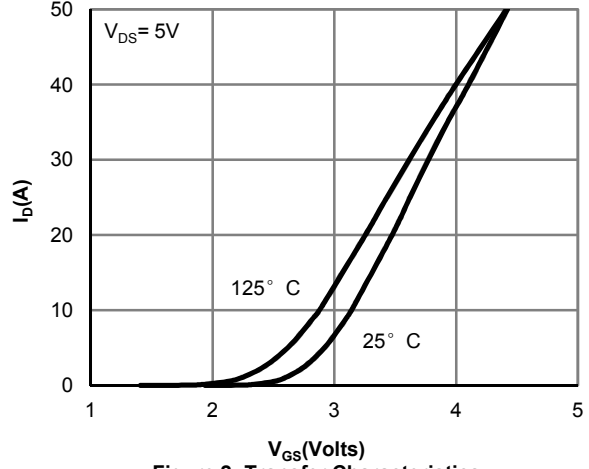
- A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E: The static characteristics in Figures 1 to 6 are obtained using <300ms pulses, duty cycle 0.5% max.
- F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.
- G: The maximum current rating is limited by bond-wires.
- H: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The SOA curve provides a single pulse rating.
- Rev12: Jul-2011

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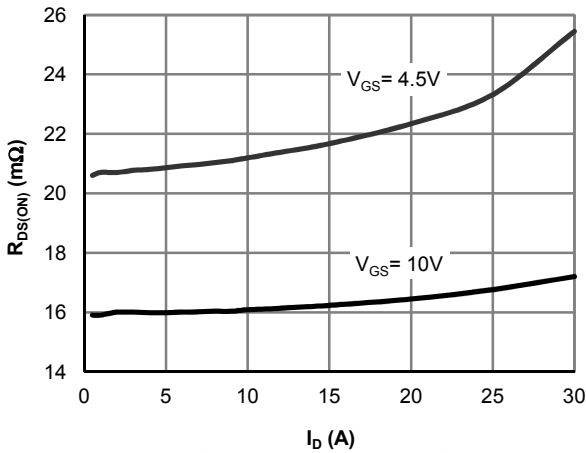
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



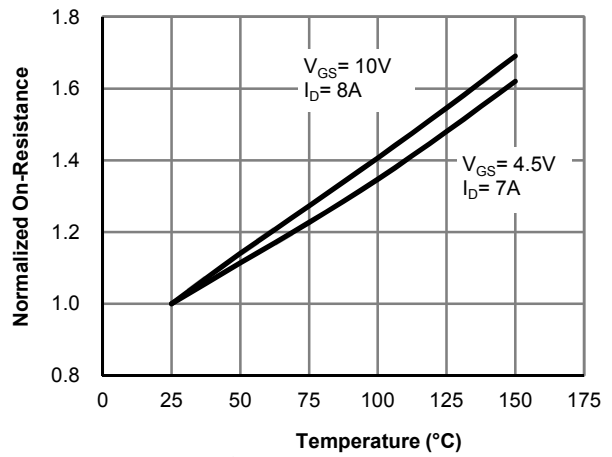
**Figure 1: On-Region Characteristics**



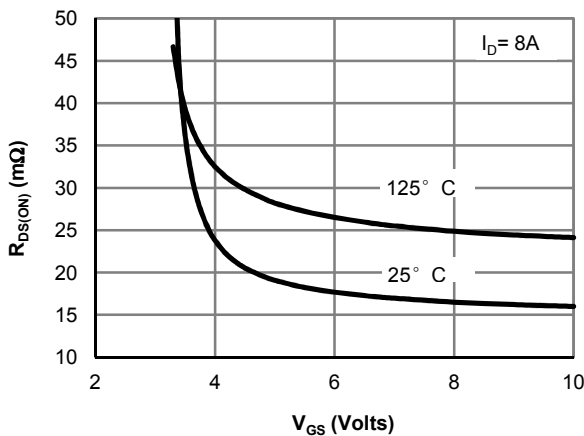
**Figure 2: Transfer Characteristics**



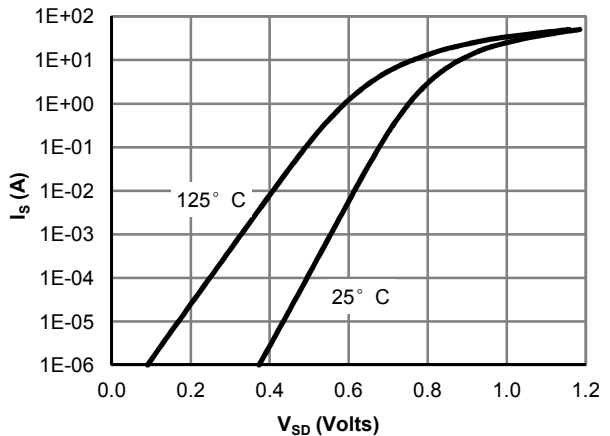
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

**TYPICAL ELECTRICAL AND THERMAL CHARACTER**

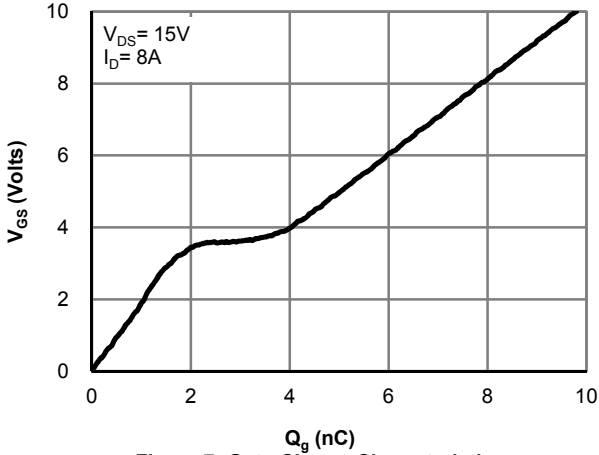


Figure 7: Gate-Charge Characteristics

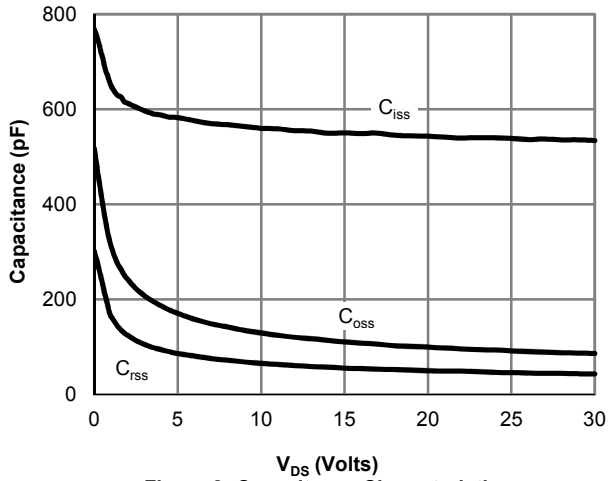


Figure 8: Capacitance Characteristics

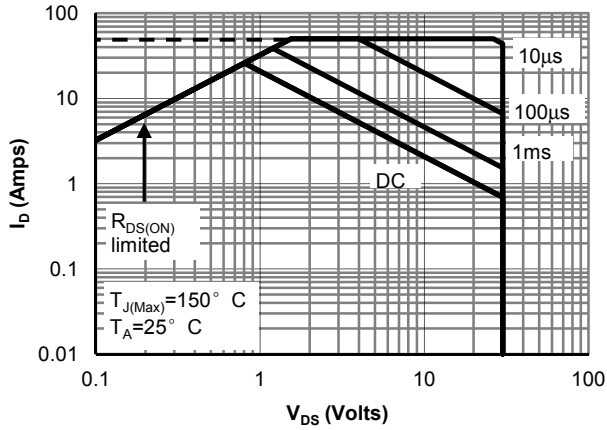


Figure 9: Maximum Forward Biased Safe Operating Area (Note H)

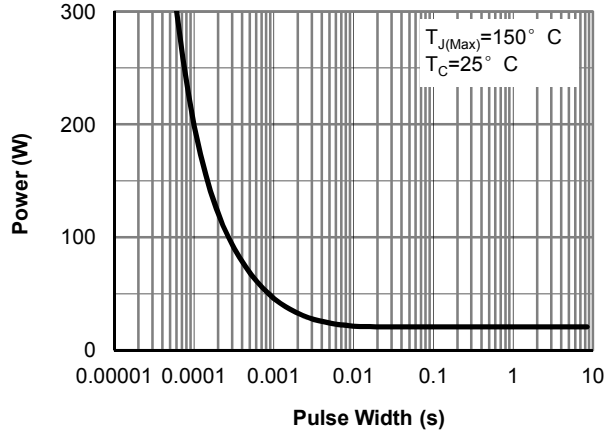


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

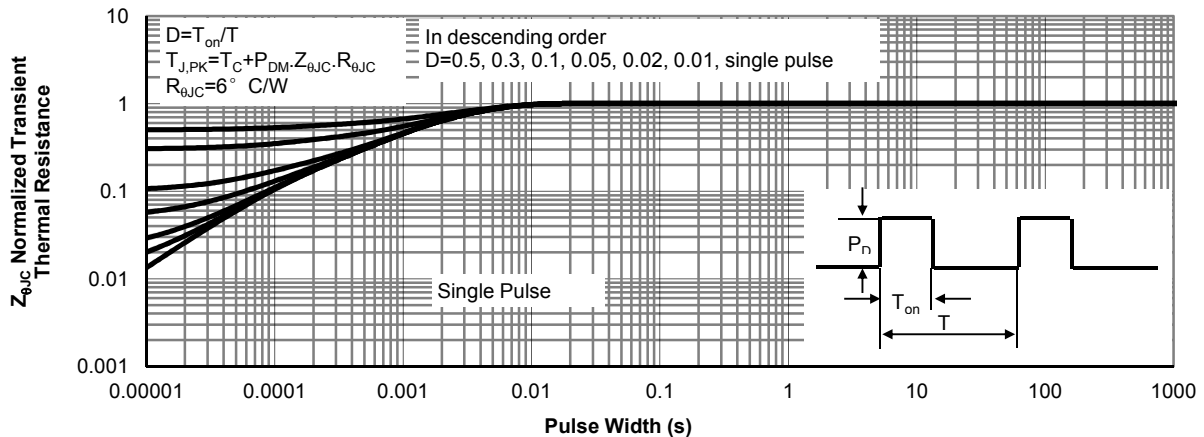


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

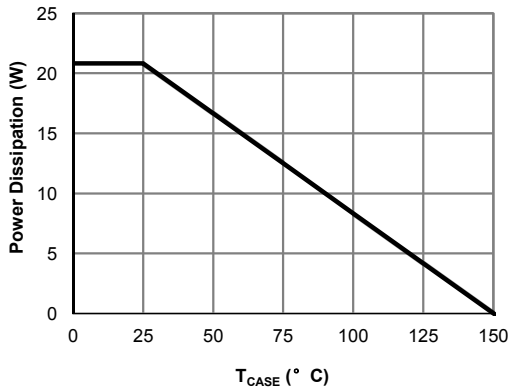


Figure 12: Power De-rating (Note F)

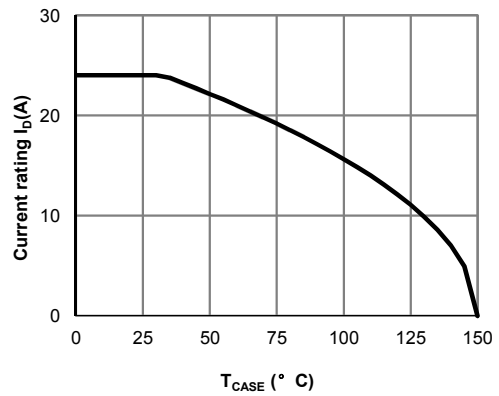


Figure 13: Current De-rating (Note F)

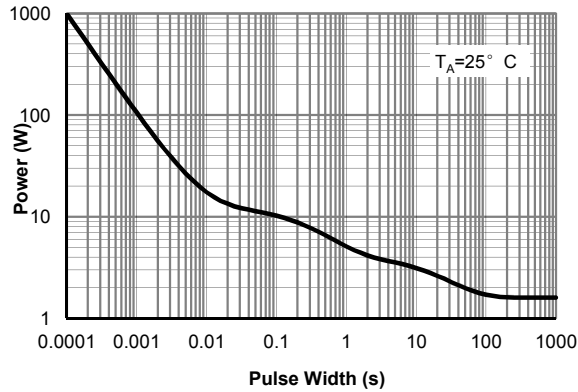


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

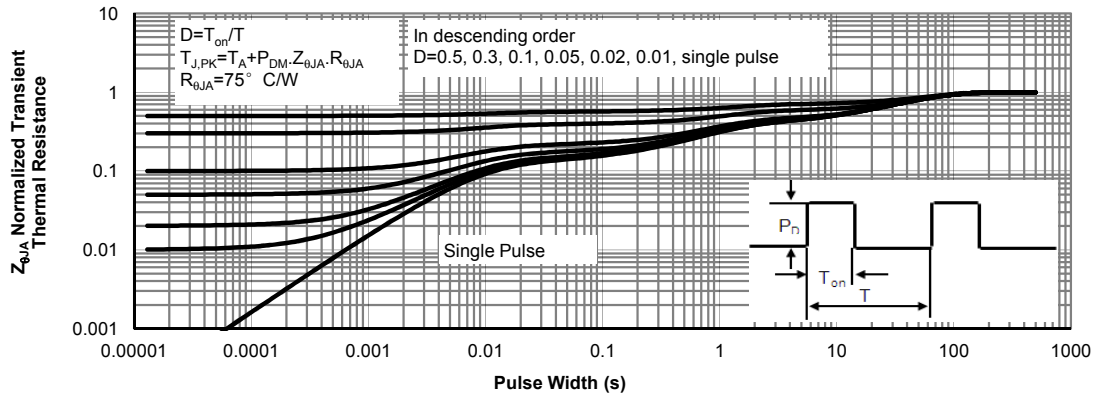
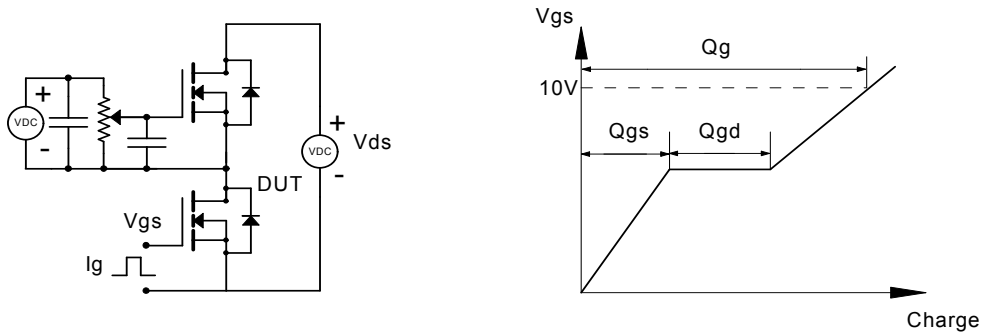
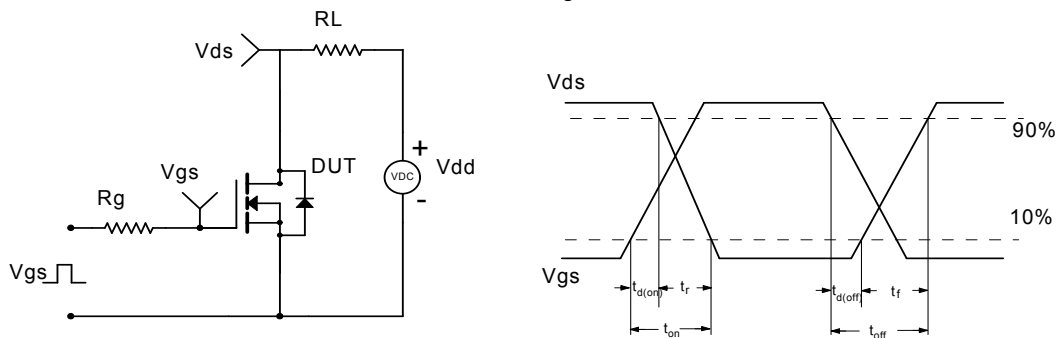


Figure 15: Normalized Maximum Transient Thermal Impedance(Note H)

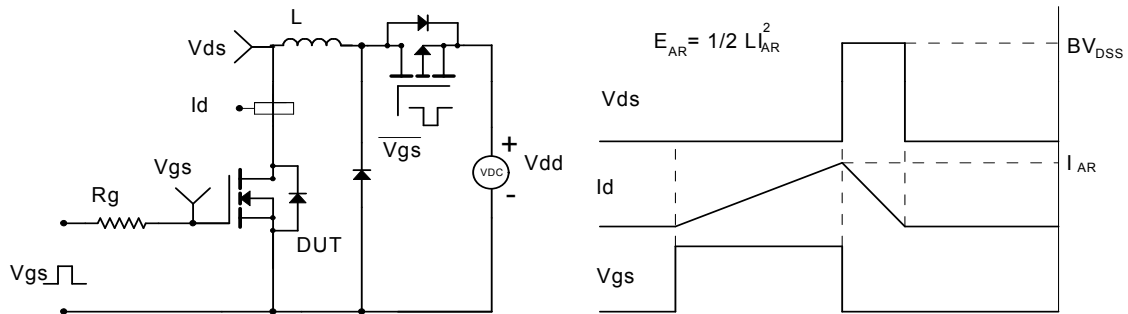
### Gate Charge Test Circuit & Waveform



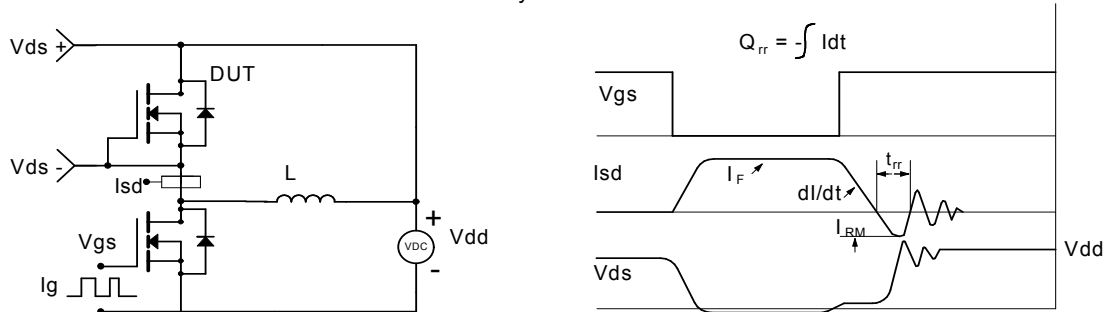
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms



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